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The PE42524 40 GHz SPDT Substrate Carrier Assembly Guide

Introduction

The PE42524 is the first microwave switch to be offered by Peregrine Semiconductor. It harnesses the high frequency performance of UltraCMOS® with monolithic microwave integrated circuit (MMIC) design techniques to yield unprecedented performance in the K and Ka microwave bands. Achieving 2 dB of insertion loss and greater than 45 dB of isolation at 30 GHz, the PE42524 reflective single pole double throw (SPDT) also brings to this frequency range the same high power and high linearity performance for which Peregrine's UltraCMOS technology is historically known.

To achieve this performance level, nothing can be taken for granted in the assembly of the PE42524 into higher-level assemblies. This application note provides design details related to the recommended landing pattern and the assembly process for obtaining the peak performance of PE42524.

Summary

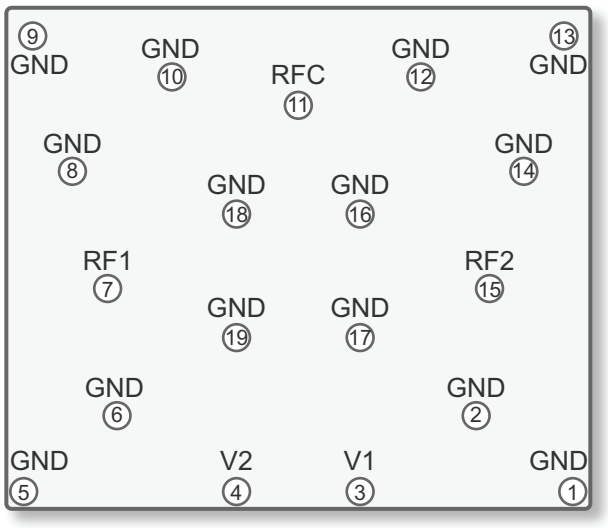
- Enables 2 dB insertion loss and >45 dB isolation @ 30 GHz
- Recommended landing patterns
- Assembly details
- Measurement summary

Product Overview

The PE42524 is a flip-chip SPDT that utilizes lead-free solder ball technology to provide the signal and ground interconnect. Solder reflow profiles common to lead-free surface-mount device (SMD) assembly can readily be used to achieve uniform and reliable attachment. Since the material composition of sapphire is identical to alumina, Al_2O_3 aluminum oxide, the coefficients of thermal expansion for the two materials is a nearly identical 5–7 ppm / °C (or 5–7 × 10^{-6} / °K) resulting in a mechanically reliable and robust interconnect.

The pin configuration for the PE42524 is shown in *Figure 1* while the detailed pin descriptions are listed in *Table 1*. The pin configuration is such that a minimum of 500 µm (0.5 mm) pitch is maintained between all unique signal pads to permit ease of routing and manufacturing.

Figure 1. Pin Configuration* (Bumps Up)



Note: * Drawing is not drawn to scale.

Table 1. Pin Descriptions

Pin #	Pin Name	Description
1, 2, 4, 5, 8–10, 12–14, 16–19	GND	Ground.
7	RF1	RF port 1.
11	RFC	RF common port.
15	RF2	RF port 2.
3	V1	Control logic input 1.
4	V2	Control logic input 2.

Landing Patterns

The PE42524 is configured with a 0.5 mm, or 500 µm, minimum ball pitch. Thin film technologies can readily meet the line width and spacing critical dimensions (CD) of 100 µm or less, but other thick film and PCB processes generally require far less stringent CDs to reach reasonable and consistent manufacturing yields. The comparatively wide 500 µm ball pitch is intended to support the larger CD requirements and enable assembly of the die directly to RF PCB boards.

To obtain the best microwave performance, specific metallization and via patterns have been defined and implemented to provide measured results for the PE42524. These recommended layouts can be downloaded from the Peregrine Semiconductor website.

Alumina Substrate

Figure 2 depicts two recommended metallization patterns and via placements for alumina substrate carriers on which the PE42524 is assembled. The first substrate carrier, shown in *Figure 2a,* uses an alumina thickness of 10 mil with 8 mil diameter vias. Important parameters for the coplanar waveguide with ground (CPWG) transmission lines are as follows: The RF common port (RFC) transitions from a 50 ohm input to a 45 ohm line of length and width of 42 mil and 6 mil, respectively, and then transitions to a 65 ohm line of length and width 17.5 mil and 2.8 mil, respectively. The RF1 and RF2 ports transition from 50 ohm transmission lines (width and spacing of 5.13 mil and 3.54 mil, respectively) to 61 ohm lines of length and width of 8.3 mil and 3.5 mil, respectively.

This substrate carrier is referenced as PRT58123 and is used for the sampling and the characterization of the PE42524 SPDT. A second substrate carrier also uses 10 mil alumina but has an increased number of filled vias. The PRT60965, shown in *Figure 2b*, has 28 vias compared to 18 vias in the PRT58123 version.

In general, should the end application need to use a different thickness alumina between 5–10 mil, the critical dimensions of line width and spacing and via diameter can be readily scaled to accommodate the specific thickness requirements.

Figure 2a. PRT58123 10 mil Alumina Substrate Metallization and Via Pattern Used for Characterization and Sample Units

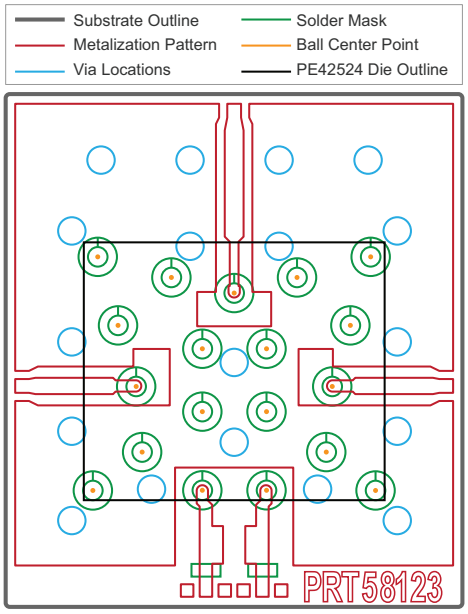
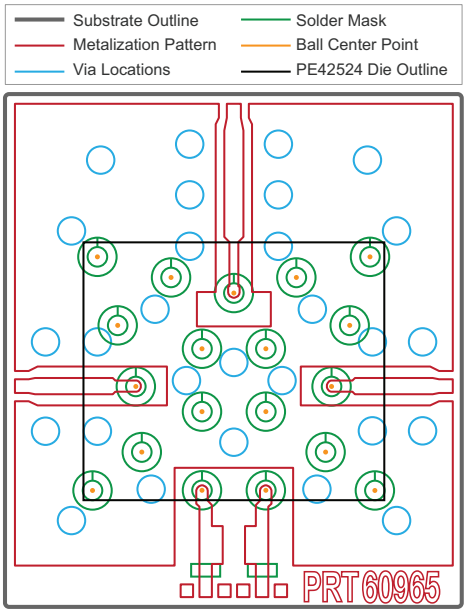


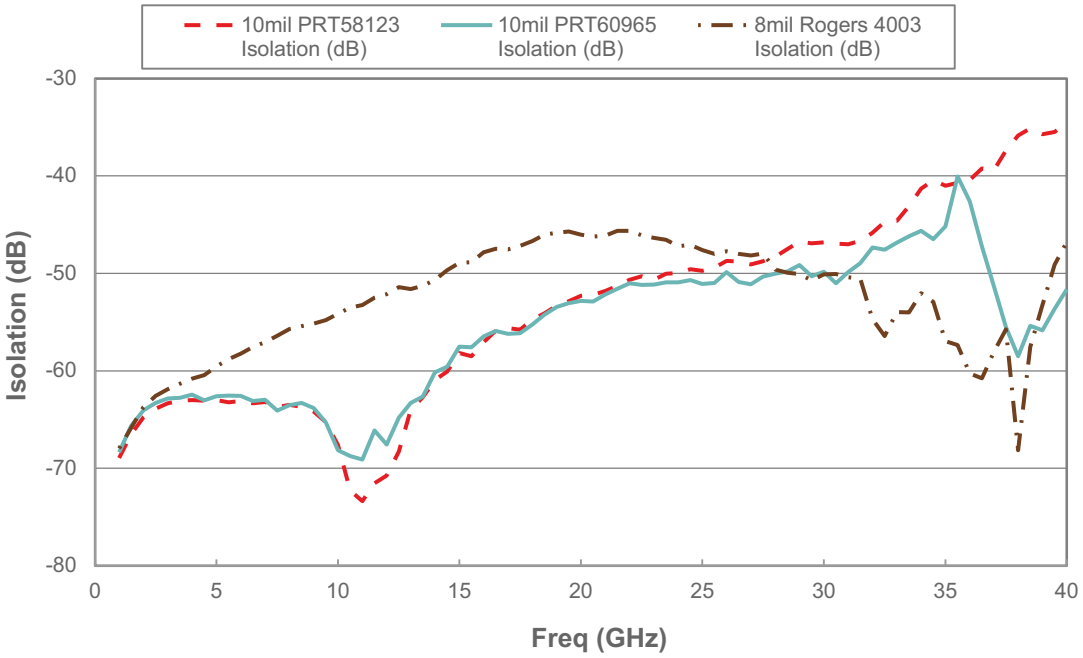
Figure 2b. PRT60965 10 mil Alumina Substrate Metallization and Via Pattern Recommended for Maximum Isolation



As mentioned earlier, RF performance can be affected by the specifics of the metallization and via patterns. This is shown in *Figure 3*, which depicts the changes in isolation levels due to differences in the number of vias and minor changes in the metal pattern. The best isolation is achieved using the PRT60965 design. In comparison, the substrate used for sampling and characterizing the PE42524, PRT58123, is also shown.

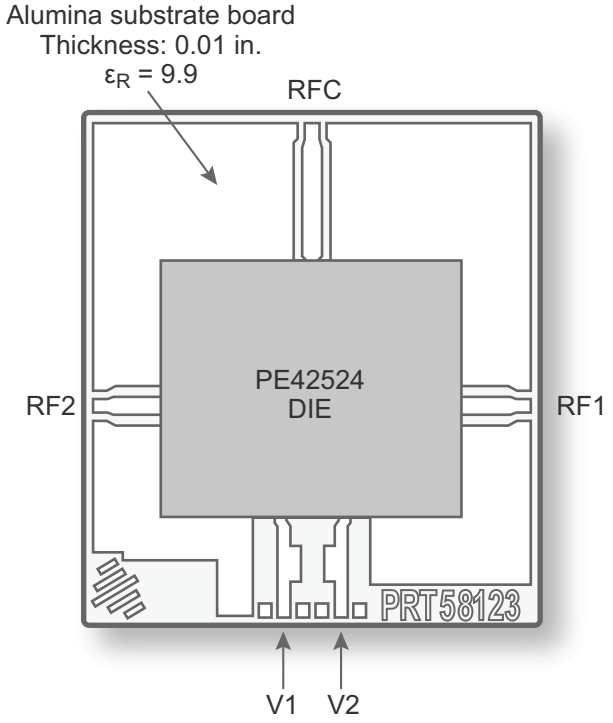
The isolation of the PRT58123 substrate carrier at 40 GHz degrades to 35 dB while the PRT60965 version has greater than 40 dB across the entire range. Isolation performance for the Rogers 4003 PCB substrate (PRT44405) is also shown in *Figure 3*. The PCB vias are located on entirely different coordinates, since the substrate material gives different trace patterns compared to the alumina versions.

Figure 3. Isolation Performance Comparison Between 10 mil Alumina Substrate Carriers PRT58123 and PRT60965 Metallization and Via Patterns*



Note: * The PRT60965 is the recommended pattern for maximum isolation. Isolation for the 8 mil Rogers 4003 (PRT44405) substrate carrier is also shown.

Figure 4. Assembled PE42524 on Alumina Substrate PRT58123



To minimize unwanted wicking of individual solder balls from the local connection point, some form of solder stop is strongly recommended. This could be a marking or protective polymer layer, or some other material that the substrate manufacturer may recommend. The thickness of the solder stop is suggested to be in the 15–25 µm range to assure its effectiveness in stopping solder wicking while not touching the face of the PE42524 die.

Finally, the line width and spacing at the edge of the RF lines in the landing pattern is configured for 150 µm pitch Ground-Signal-Ground (G-S-G) RF probes to facilitate accurate measurements. The user should feel free to modify and integrate the landing pattern anywhere outside the die outline to align with the higher level assembly and substrate design requirements.

Rogers 4003 Printed Circuit Board

A metallization and via pattern PRT44405 has also been generated for a Rogers 4003 substrate. *Figure 5* shows the pattern that is designed for an 8 mil board thickness. This board layout is configured to work with high frequency SMA connectors, but the basic pattern can be used to create an RF-probable PCB. Such a PCB is shown in *Figure 6*. The measured performance of the PE42524, when assembled to the PCB and properly de-embedded, results in performance that is comparable to that achieved using the alumina-based design.

Important dimensions, in addition to the 50Ω transmission line width and spacing, include the dimensions of the thinner lines right at the PE42524 SPDT RF ports. The RF common port (RFC) transitions from a 50 ohm line to a line length and width of 21 mil and 6 mil (Z = 75 ohm), respectively, and the two RF ports RF1 and RF2 transition from a 50 ohm line to a line length and width of 16.5 mil and 6 mil (Z = 75 ohm), respectively. Note that these parameters serve as alternate matching impedances that can yield similar results if the transmission line impedances used for the alumina substrate are used for the PCB. Via diameters are 8 mil except in the region under the die, which uses 5 mil diameter.

Figure 5. PCB Rogers 4003 PRT44405 Metallization and Via Patterns

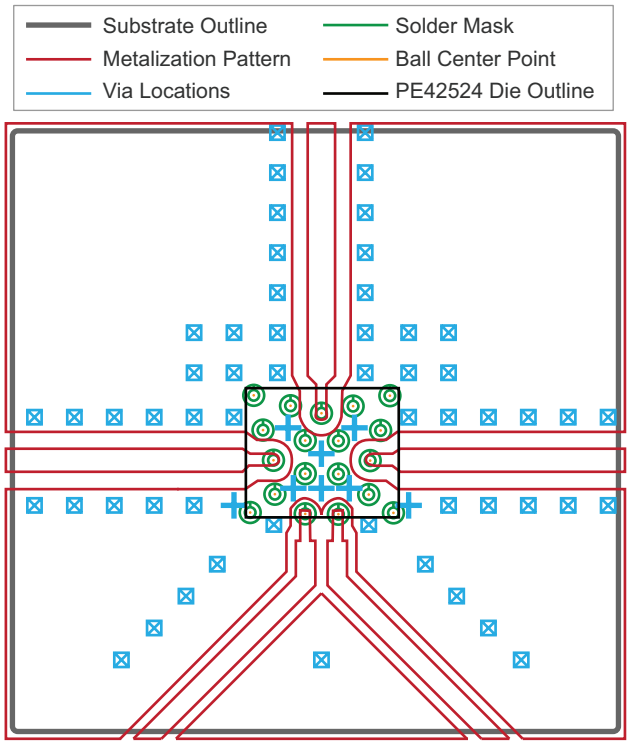
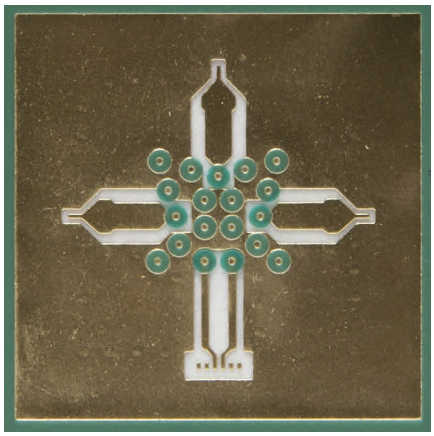


Figure 6. PCB Rogers 4003 Evaluation Board Based Upon the PRT44405 Metallization and Via Patterns



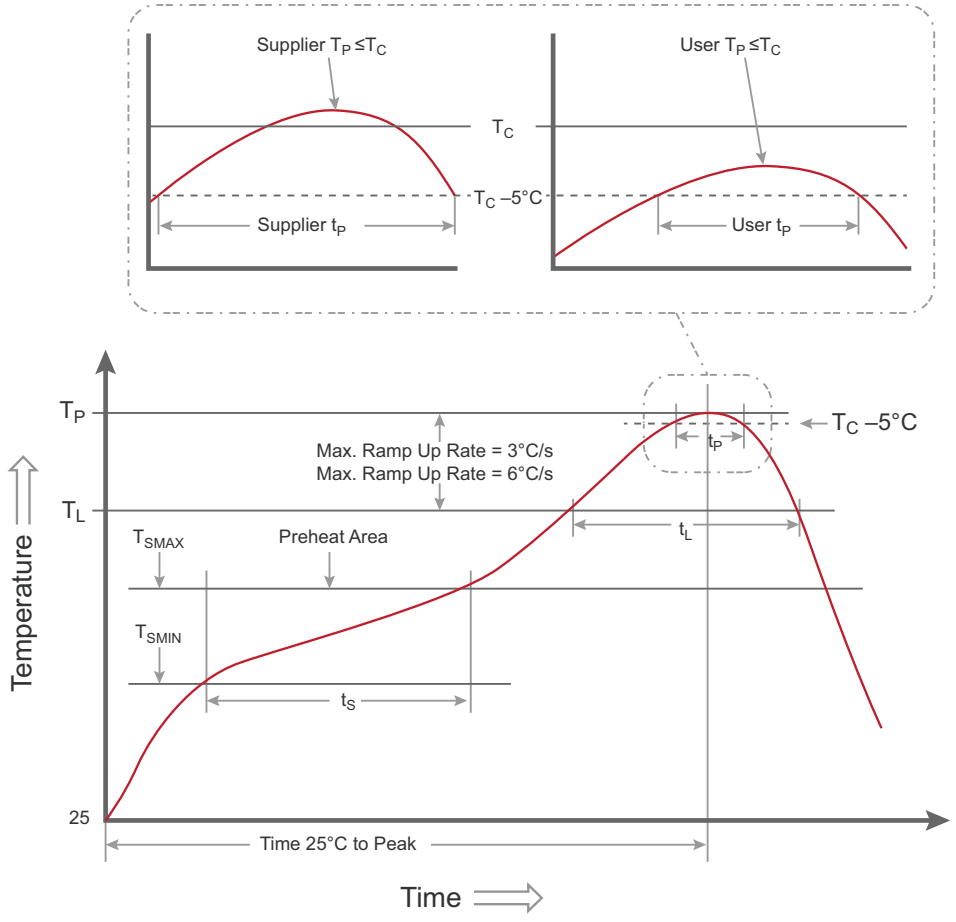
Assembly Process

The means of assembly for the PE42524 leverages common SMD solder reflow techniques. A reflow profile suitable for use with an alumina substrate is depicted in *Figure 7* and follows a recognized JEDEC profile. The following recommendations apply to properly attaching the PE42524.

- No solder paste needs to be printed.
- Apply a thin layer of flux by stencil printing.
- Pick and place the die and align it on the Substrate.
- Conduct reflow using a controlled reflow Profile.
  - Refer to JSTD020D–01, *Table 4–1*, *Table 4–2*, Section 5.6 and *Figure 5–1*:
    * Lead-based reflow: *Table 4–1*
    * Lead-free reflow: *Table 4–2*
    * Reflow definition: Section 5.6 and *Figure 5–1*
- Check for alignment and voids in joints using X-ray inspection after reflow.

The above assembly guidance is targeted for attaching the PE42524 to an alumina-based substrate. If a PCB is being used, careful attention to the substrate material, its glassivation temperature (T_g) and the material coefficient thermal expansion (CTE) must be given while defining a reliable reflow profile. Excessive soak times and temperatures can each cause significant assembly yield issues.

Figure 7. Generalized Reflow Profile*



Note: * Reference JEDECJ–STD–020D.1 *Figure 5–1* and *Table 5–2*.

Assembly Recommendations for Attaching the PE42524 on a PCB

Careful attention must be given to the PCB substrate material, its glassivation temperature, Tg, and the various CTEs while defining a reliable reflow profile. Excessive soak times and temperatures can each cause significant assembly yield issues and potentially laminate delamination.

Table 1–Table 3 of assembly related process parameters are provided to help the user define an assembly flow that works for some specific high frequency PCB substrates. Details concerning other components on the same PCB, the PCB substrate temperatures limitations and the PCB board design and its thermal properties will all need to be considered in refining a suitable reflow profile and assembly process.

Table 1. PE42524 Assembly Related Parameters

Parameter	PE42524	Unit	Comments
Max reflow temp, T_P	≥ 260	°C	JEDEC J-STD-020D.1 Table 4-2
Max dwell at T_P	10	sec	JEDEC J-STD-020D.1 Table 5.2
Recommended flux			
Pb-free solder ball	Tin-95.5/Ag-3.5/ Cu-1 (%)		SAC 351 solder definition
Min landing size	90	um	
Solder stop max thickness	25	um	
Solder stop diameter	190	um	
Solder paste particle size	Type 5		15–25 um particle size
Stencil thickness	60	um	
Stencil aperature diameter	180	um	
CTE (worst case, X, Y, Z)	6–7	ppm/°C	
Underfill	Not recommended		If deemed necessary, a low loss, low dielectric constant underfill is recommended.

Table 2. Assembly Related Parameters for Common High Frequency PCB Substrates

Parameter		Panasonic Megtron 6	Rogers 4350	Rogers 4003	Unit
Max reflow temp, T_P		≥ 260	≥ 260	≥ 260	°C
Max dwell at T_P		10	10	10	Sec
Glassivation temp, T_G		180–210	>280	>280	°C
CTE (worst case X, Y, Z)	X		10	11	ppm/°C
	Y		12	14	
	Z	45	32	46	

Figure 8. Suggested Starting Definition for PCB Reflow Profile

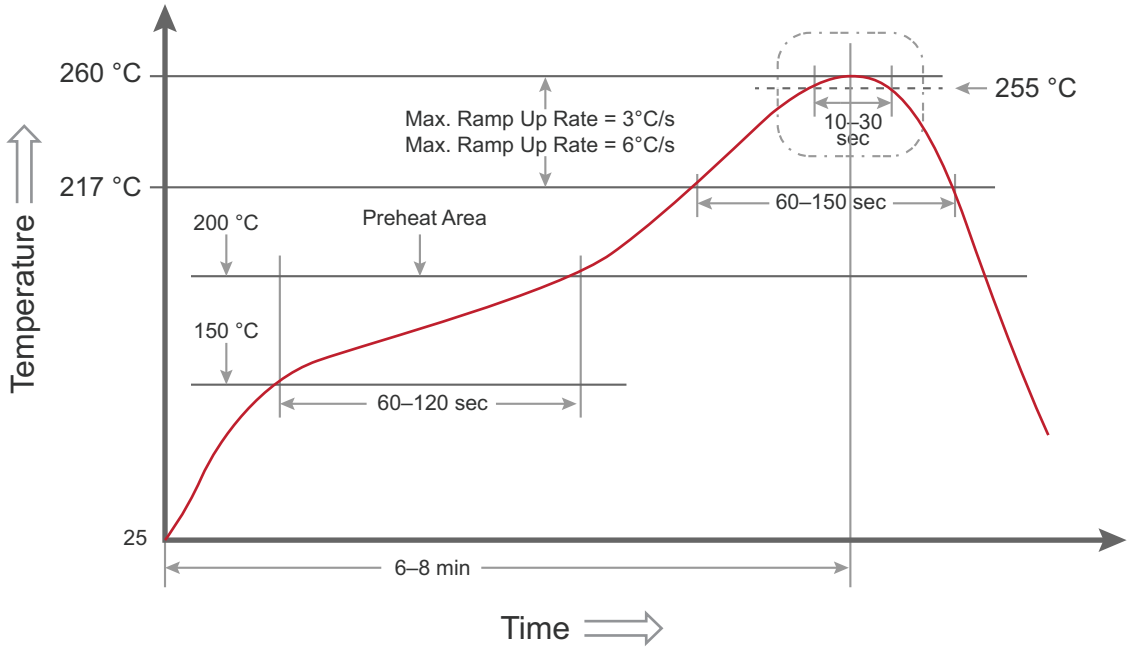


Table 3. Reflow Profile Parameter Recommendations (source: JEDEC J-STD-020D.01)

Profile Parameter	Pb-free Assembly	Unit	Comments
Preheat temperature	150–200	°C	
Preheat time	60–120	sec	
Ramp up rate	3	°C/sec	
Liquidous temperature, T_L	217	°C	SAC 351 melting point
Time above T_L	60–150	Sec	
Peak temperature, T_P	260	°C	
Time within 5 °C of T_P	10–30	sec	
Time 25 °C to T_P	6–8	min	
Ramp down rate	3–6	°C/sec	

The use of underfill may be needed to address the mechanical stresses that arise primarily from differences in the coefficients of thermal expansion (CTE). The laminate PCB substrates listed have CTEs above 32 ppm/°C, or more than 4xthat of the PE42524. Underfill materials will have an impact on the peak RF performance, and therefore, when underfill is deemed necessary, Peregrine suggests using a low loss, low dielectric constant underfill that is compatible with the entire assembly process.

Measured Performance

Figure 9 shows the insertion loss behavior to 40 GHz of the PE42524 when mounted to the PRT58123 alumina substrate carrier and measured in an RF probe configuration. *Figure 10* shows the >45 dB of isolation at 30 GHz and the RFC and RF1 active port return losses.

Figure 9. Insertion Loss of PE42524 on 10 mil Alumina Substrate Carrier

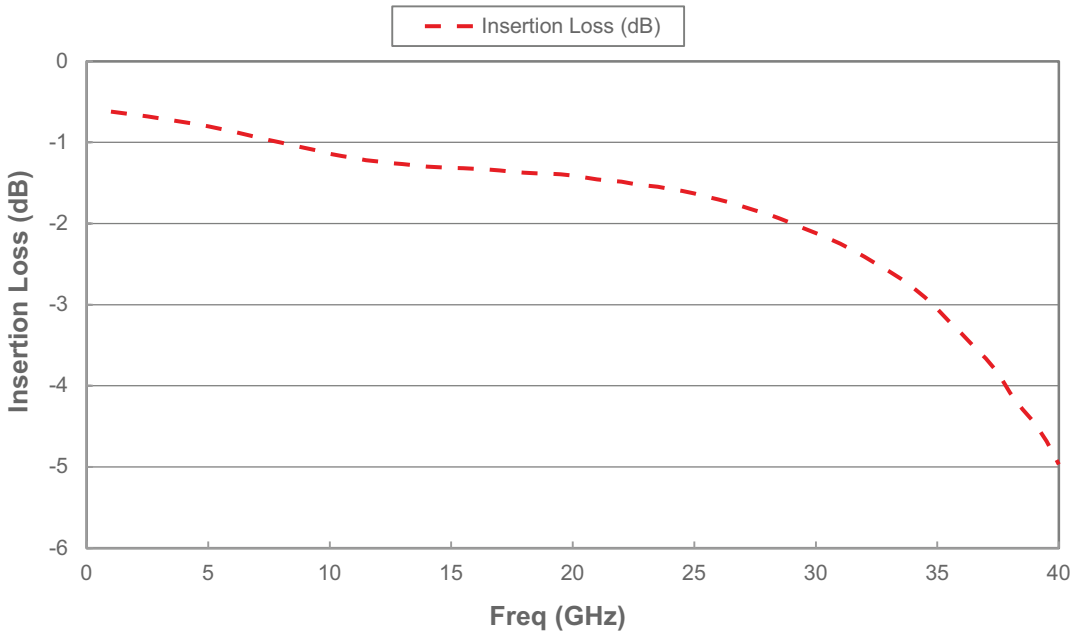
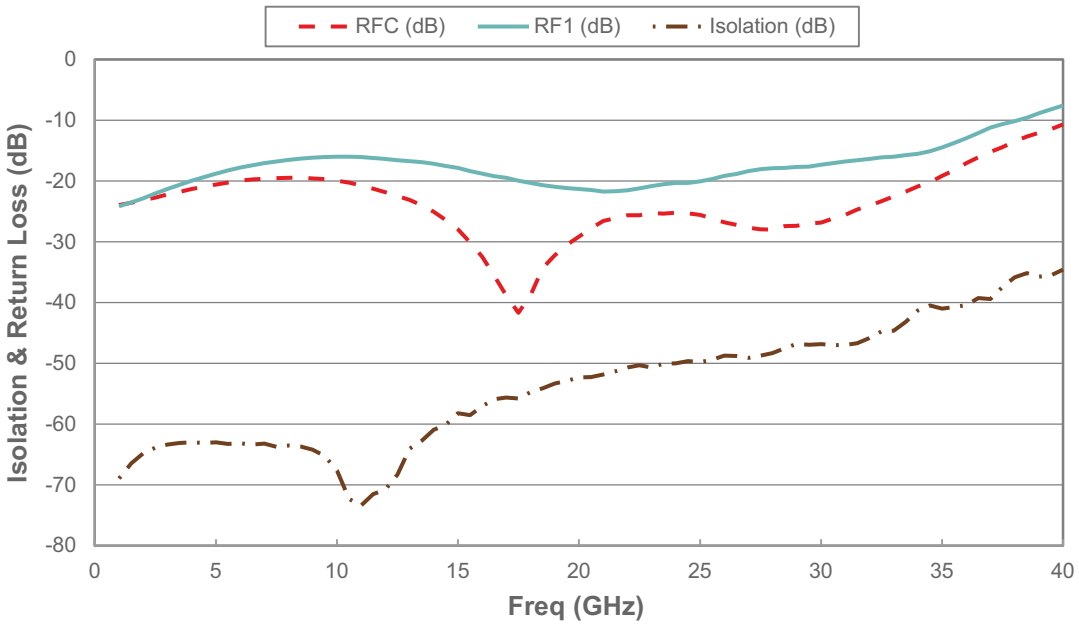


Figure 10. Isolation and Return Loss of PE42524 on 10 mil Alumina Substrate Carrier



Similarly, for the Rogers 4003 PRT44405 substrate, *Figure 11* shows the insertion loss response to 40 GHz while *Figure 12* contains the isolation and the RFC and RF1 active port return losses.

Figure 11. Insertion Loss of PE42524 on 8 mil Rogers 4003 PRT44405 Substrate Carrier

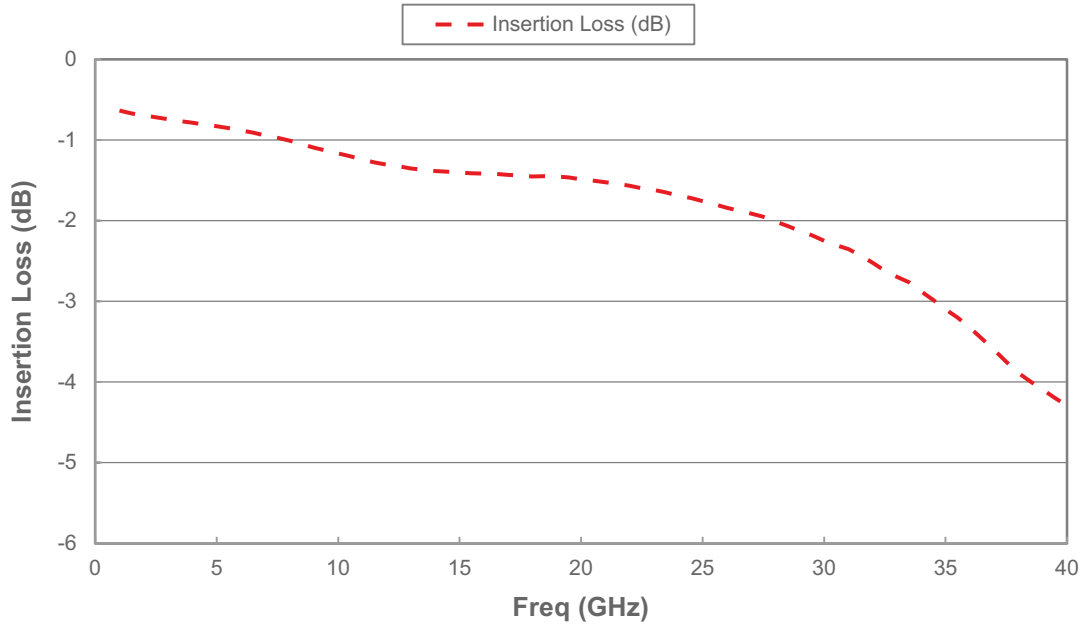
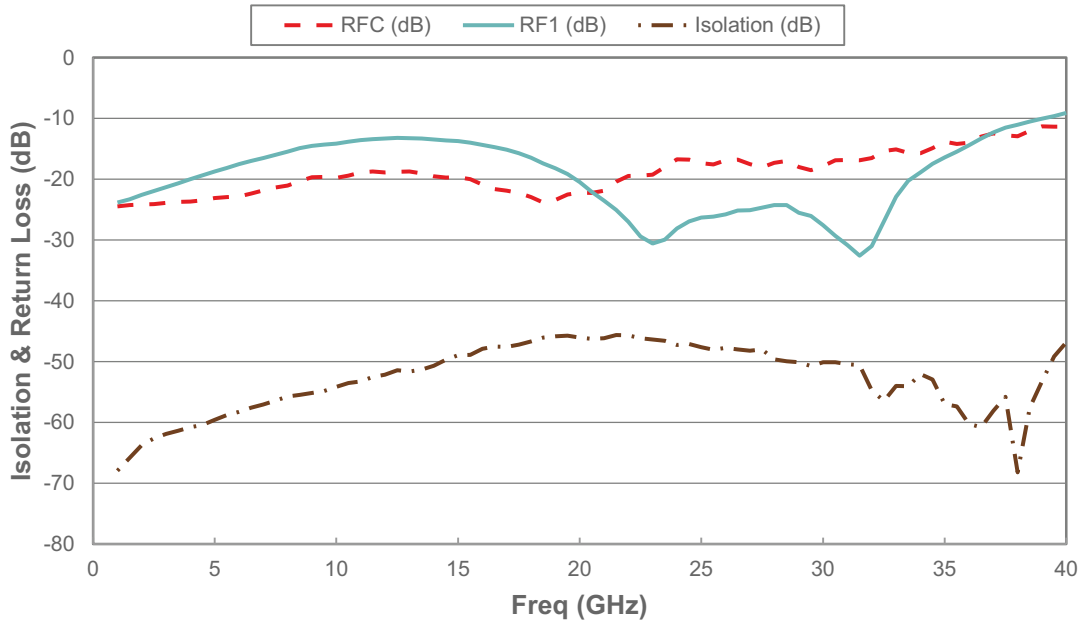


Figure 12. Isolation and Return Loss of PE42524 on 8 mil Rogers 4003 PRT44405 Substrate Carrier



Conclusion

The PE42524 is the first microwave switch to be offered by Peregrine Semiconductor. The PE42524 brings competitive insertion loss, exceptional isolation and the usual high linearity and power handling Peregrine is known for to a market that can benefit from the uniformity and availability that UltraCMOS affords to every market it enters. To achieve high performance at these frequencies, extreme care must be taken to eliminate any stray parasitics affecting the RF channel.

This application note provides guidance necessary for achieving the optimum performance from the PE42524. Landing patterns in different substrate technologies have been described, all of which have shown comparable performance up to 40 GHz. Complete CAD files of the physical layouts are available from Peregrine's website to help facilitate the integration of the PE42524 into higher-level assemblies and systems.