PE46130 and PE46140 Insertion Loss Stabilizer

Application Note 49

Summary

The insertion loss stabilizer (ILS) can be used in conjunction with the digital step attenuator (DSA) to emulate a 7-bit DSA with finer resolution. RF_{OUT2} insertion loss variation over 5-bit phase range can be reduced by using the 3-bit ILS feature. A programming lookup table is used by the controller to select the ILS bit value based on the 5-bit phase setting key. No additional programming steps are required to use the ILS bits.

Introduction

The PE46130 and PE46140 monolithic phase and amplitude controllers (MPAC)–Doherty offer excellent binary selectable phase and amplitude accuracy over the entire 5-bit phase shift and 4-bit attenuation range. These devices also feature a 3-bit ILS, which is an attenuator providing a minimum step size as low as 0.05 dB.

The 3-bit ILS can be combined with the 4-bit digital step attenuator to emulate a 7-bit DSA with a 0.05 dB and 0.06 dB resolution for the PE46130 and PE46140, respectively.

The ILS feature can also be used to improve the insertion loss variation versus phase setting on the RF_{OUT2} path over the range of the 5-bit phase control states by combining the 3-bit ILS with a programming lookup table containing the 5-bit phase state (key) and 3-bit ILS state (value).

This application note will demonstrate the performance of the emulated 7-bit DSA that can be used in applications that would benefit from a finer attenuator resolution. Also covered is the improvement in insertion loss variation over phase state achievable through the use of ILS and a lookup table based on measurement data.

Figure 1 • *PE46130 and PE46140 Functional Diagram*

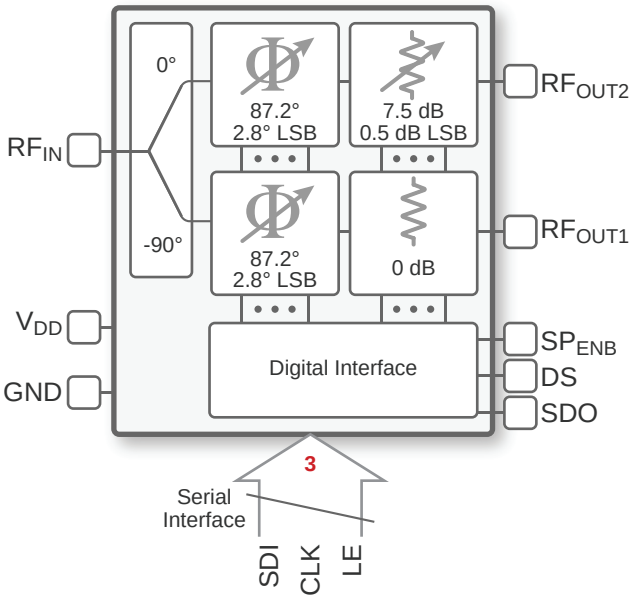
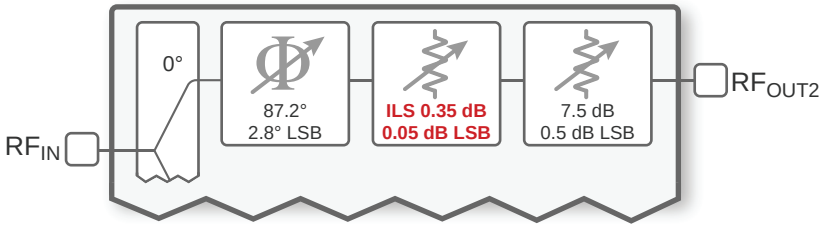


Figure 2 • *PE46130 and PE46140 Insertion Loss Stabilizer*



Using ILS to Create an Emulated 7-bit Attenuator

The PE46130 and PE46140 DSAs can be used in conjunction with the ILS bits to emulate a 7-bit DSA with a resolution of 0.05 dB and 0.06 dB for the PE46130 and PE46140, respectively. This enables the device to be used in applications that require a resolution finer than 0.5 dB or where a finer resolution could improve performance without increasing the overall insertion loss that is typically found in traditional 7-bit DSA architectures.

The bandwidth or return loss of the device is not negatively affected by the use of the ILS bits.

Programming Considerations

Programming the ILS bits is accomplished using the same 14-bit programming word used in programming the RF_{OUT2} attenuation and phase settings shown in Table 1. Table 2 and Table 3 show the location of each of the emulated seven attenuation bits in the serial programming word.

Table 1 • *PE46130 and PE46140 14-bit Programming Word*

Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	
C0	S3	S2	M3	M2	M1	M0	P4	P3	P2	P1	P0	S1	S0	
–	–	ILS2	–	–	–	–	–	–	–	–	–	ILS1	ILS0	
–	–	0.2	–	–	–	–	–	–	–	–	–	0.1	0.05	PE46130
–	–	0.25	–	–	–	–	–	–	–	–	–	0.125	0.063	PE46140

Table 2 • *PE46130 7-bit Digital Step Attenuator Bit Definition*

Programming Word Bit Location[1]	Q11	Q10	Q9	Q8	Q7	Q1	Q0	
Bit weight	M2[2]	M6	M5	M4	M3[2]	M1	M0	
Attenuation value (dB)	0.2	4.0	2.0	1.0	0.5	0.1	0.05	Attenuation setting (dB)
	L	L	L	L	L	L	L	0.0
	L	L	L	L	L	L	H	0.05[3]
	L	L	L	L	L	H	L	0.1[3]
	H	L	L	L	L	L	L	0.2[3]
	L	L	L	L	H	L	L	0.5
	L	L	L	H	L	L	L	1.0
	L	L	H	L	L	L	L	2.0
	L	H	L	L	L	L	L	4.0
	H	H	H	H	H	H	H	7.85

Table 2 • *PE46130 7-bit Digital Step Attenuator Bit Definition (Cont.)*

Programming Word Bit Location[1]	Q11	Q10	Q9	Q8	Q7	Q1	Q0	

Notes:
1) Channel and phase bits have been omitted from this table for clarity.
2) M2/M3 bits are out of traditional binary order in the serial programming word when used as a 7-bit attenuator.
3) The PE46130 ILS bits are not strictly binary weighted in relation to the attenuator.

Table 3 • *PE46140 7-bit Digital Step Attenuator Bit Definition*

Programming Word Bit Location[1]	Q11	Q10	Q9	Q8	Q7	Q1	Q0	
Bit weight	M2[2]	M6	M5	M4	M3[2]	M1	M0	
Attenuation value (dB)	0.25	4.0	2.0	1.0	0.5	0.12	0.06	Attenuation setting (dB)
	L	L	L	L	L	L	L	0.0
	L	L	L	L	L	L	H	0.06
	L	L	L	L	L	H	L	0.12
	H	L	L	L	L	L	L	0.25
	L	L	L	L	H	L	L	0.5
	L	L	L	H	L	L	L	1.0
	L	L	H	L	L	L	L	2.0
	L	H	L	L	L	L	L	4.0
	H	H	H	H	H	H	H	7.93

Notes:
1) Channel and phase bits have been omitted from this table for clarity.
2) M2/M3 bits are out of traditional binary order in the serial programming word when used as a 7-bit attenuator.

Figure 3 and Figure 4 illustrate the PE46130 and PE46140 relative insertion loss versus frequency for all states of the 7-bit emulated attenuator.

Figure 3 • *PE46130 7-bit Attenuator States Relative Insertion Loss RF_{IN} to RF_{OUT2} vs Frequency*

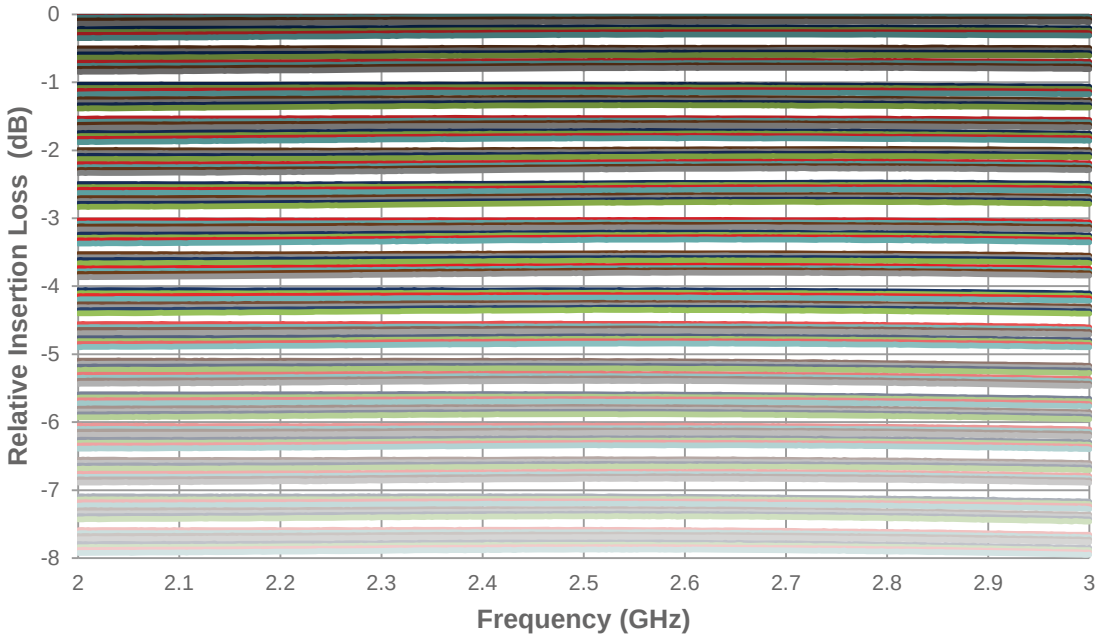


Figure 4 • *PE46140 7-bit Attenuator States Relative Insertion Loss RF_{IN} to RF_{OUT2} vs Frequency*

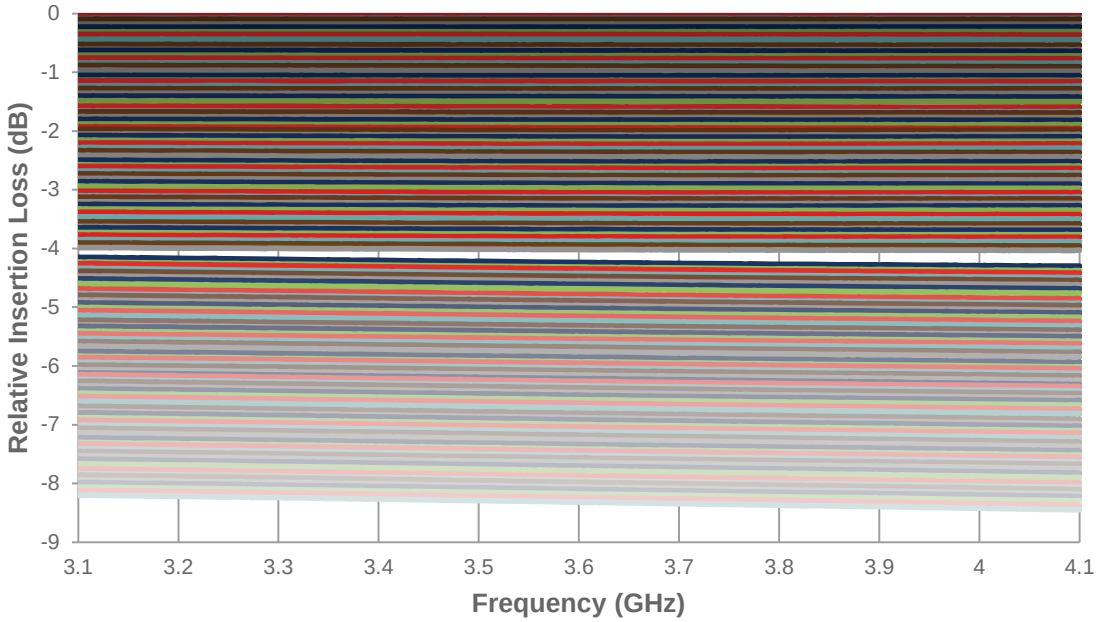


Figure 5 and Figure 6 illustrate the PE46130 and PE46140 insertion loss error versus frequency (desired attenuation subtracted from the relative insertion loss measurement) for all states of the 7-bit emulated attenuator.

Figure 5 • *PE46130 RF_{OUT2} 7-bit Attenuator Relative Insertion Loss Across Frequency*

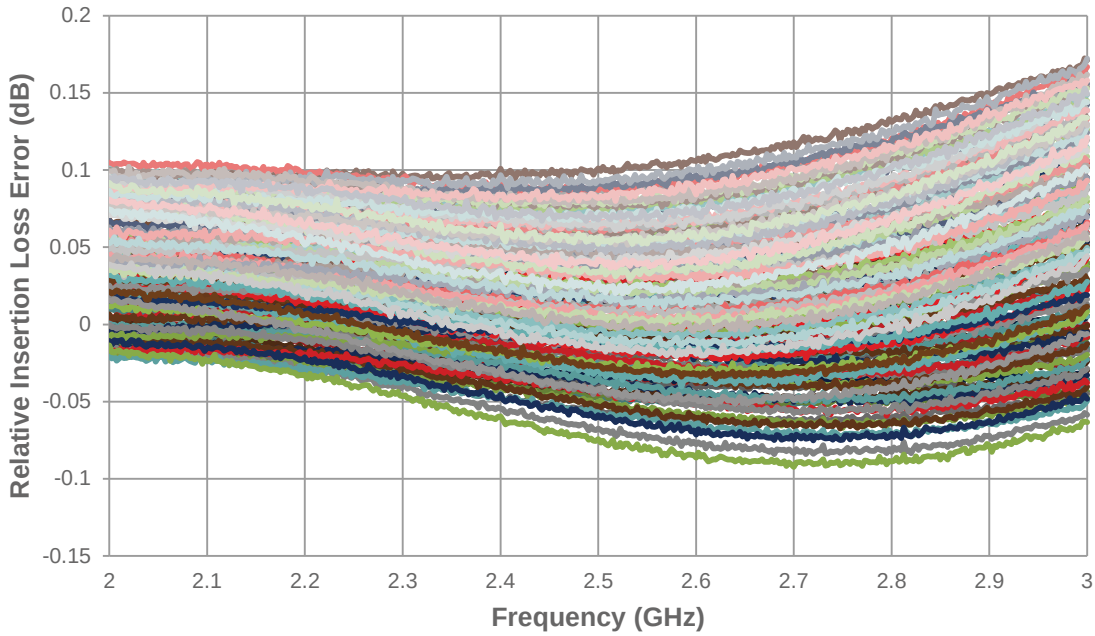


Figure 6 • *PE46140 RF_{OUT2} 7-bit Attenuator Relative Insertion Loss Across Frequency*

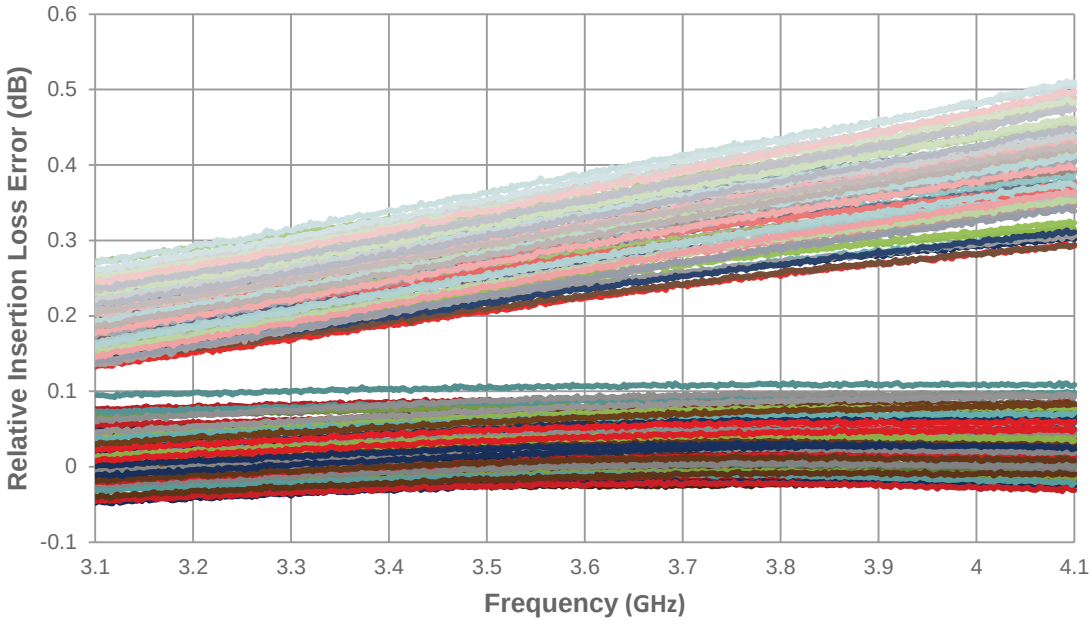


Figure 7 and Figure 8 illustrate the PE46130 and PE46140 relative insertion loss at low, mid and high frequency when the 4-bit attenuator is combined with the 3-bit ILS creating an emulated 7-bit attenuator.

Figure 7 • *PE46130 RF_{OUT2} 7-bit Attenuator Relative Insertion Loss Across Attenuation*

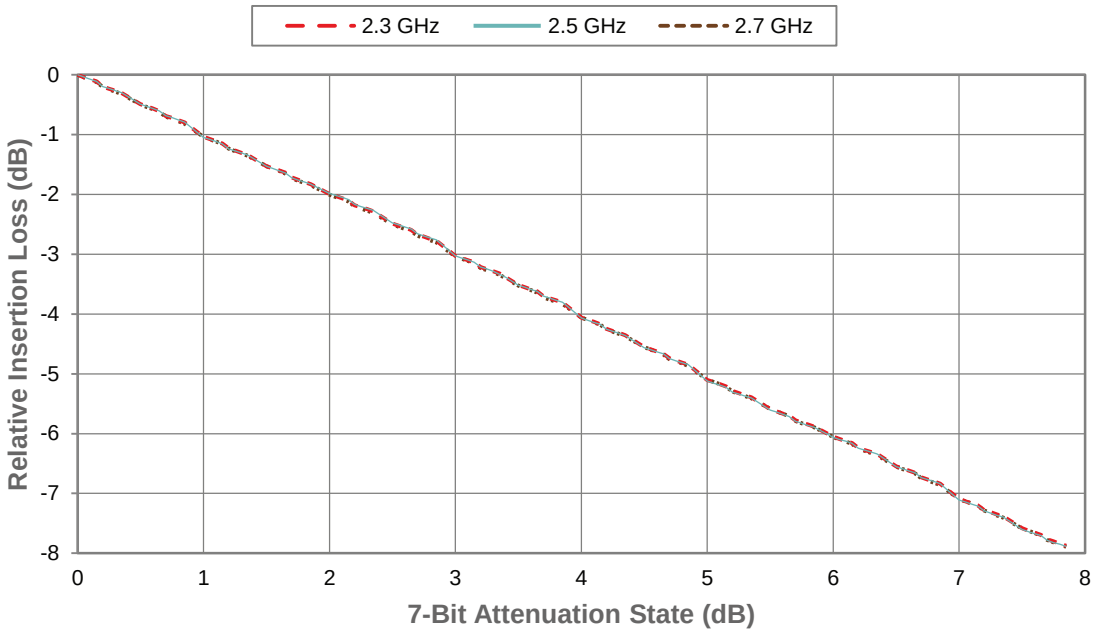
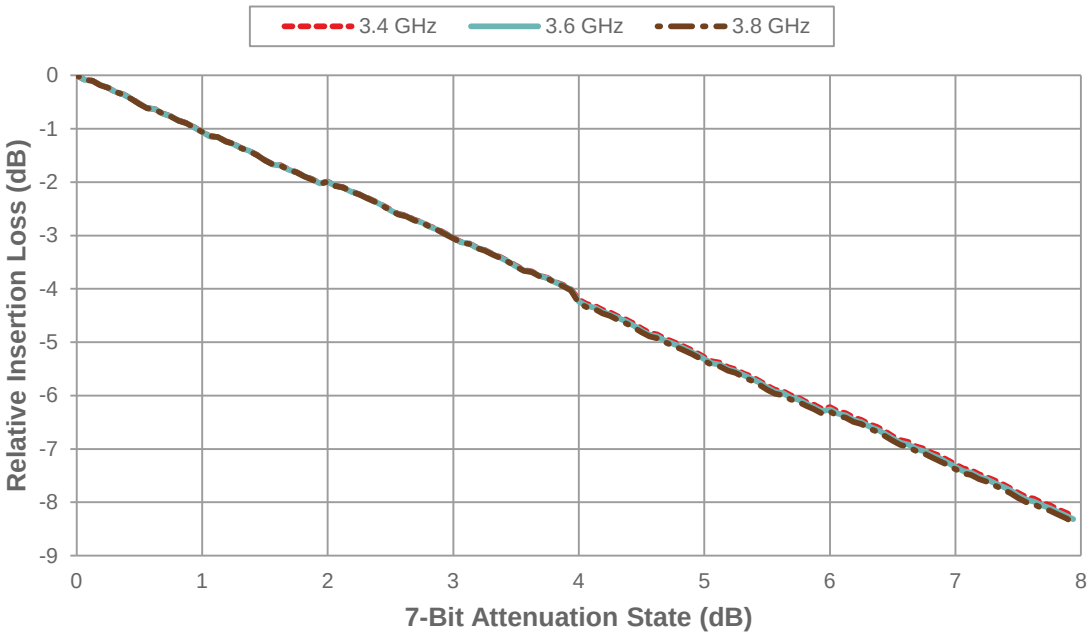


Figure 8 • *PE46140 RF_{OUT2} 7-bit Attenuator Relative Insertion Loss Across Attenuation*

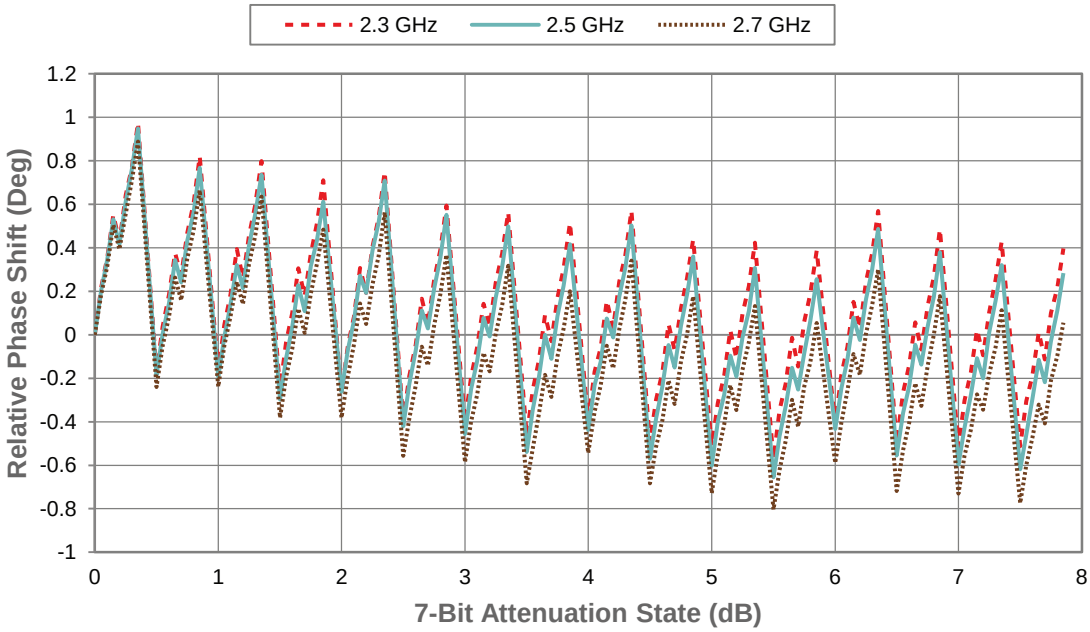


Phase Measurements

Before relative phase states can be compared to another, the measured phase data must be unwrapped and normalized. The raw phase states are measured with the vector network analyzer, which returns phase data that wraps each time the phase crosses a ±180 degree threshold. The reference state phase trace versus frequency must be unwrapped using a MOD function (integer division). Each subsequent measured phase state is then unwrapped in the same manner. All traces are normalized to the reference state by subtracting the reference state phase from the measured phase.

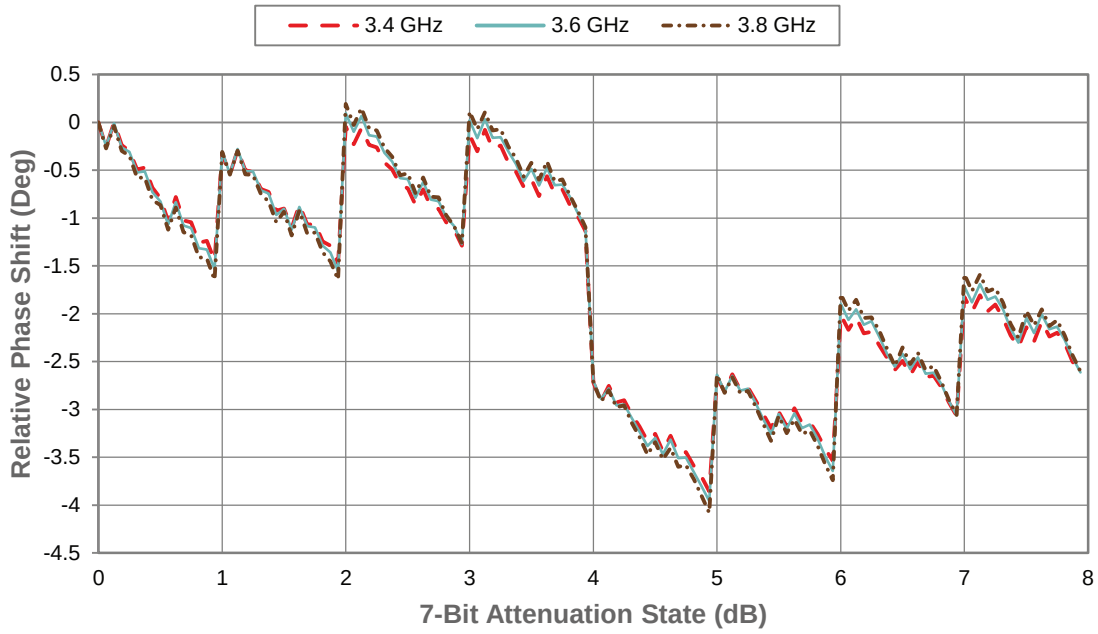
Figure 9 and Figure 10 illustrate the PE46130 and PE46140 relative phase variation at low, mid and high frequency versus the 7-bit emulated attenuator state. The phase setting is held at the reference phase state.

Figure 9 • *PE46130 RF_{IN}–RF_{OUT2} Phase Variation Across RF_{OUT2} 7-bit Attenuation State*(*)



Note: * Phase set to reference phase.

Figure 10 • *PE46140 RF_{IN}–RF_{OUT2} Phase Variation Across RF_{OUT2} 7-bit Attenuation State*(*)



Note: * Phase set to reference phase.

Figure 11 and Figure 12 illustrate the PE46130 and PE46140 relative phase variation at low, mid and high frequency versus the 3-bit ILS state. The phase setting is held at the reference state.

Figure 11 • *PE46130 Relative Phase RF_{IN}–RF_{OUT2} vs All Insertion Loss Stabilizer States*

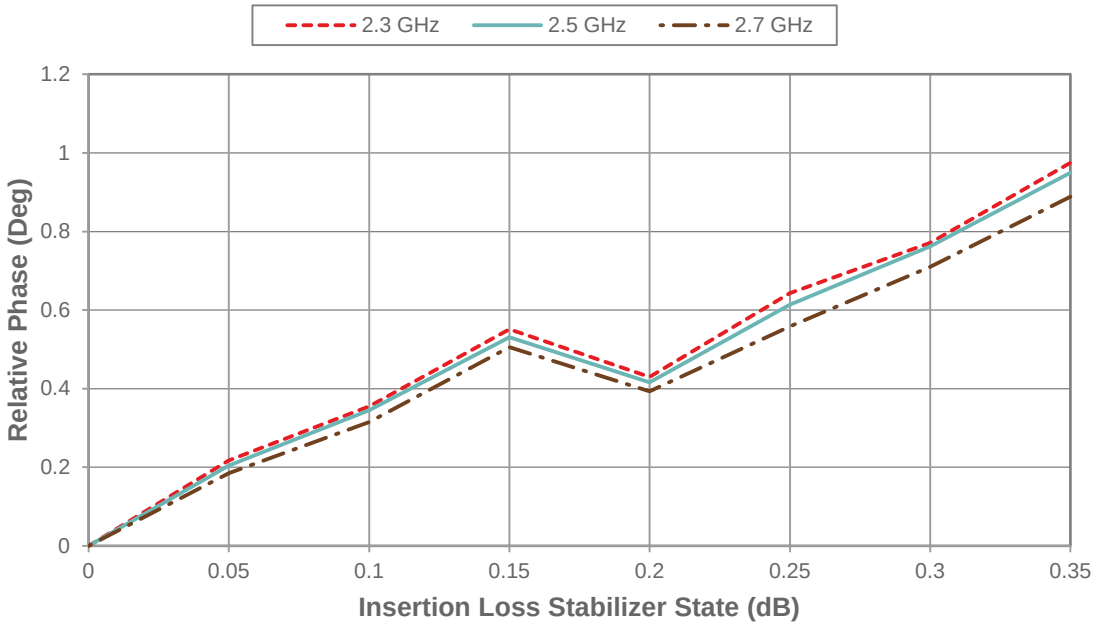


Figure 12 • *PE46140 Relative Phase RF_{IN}–RF_{OUT2} vs All Insertion Loss Stabilizer States*

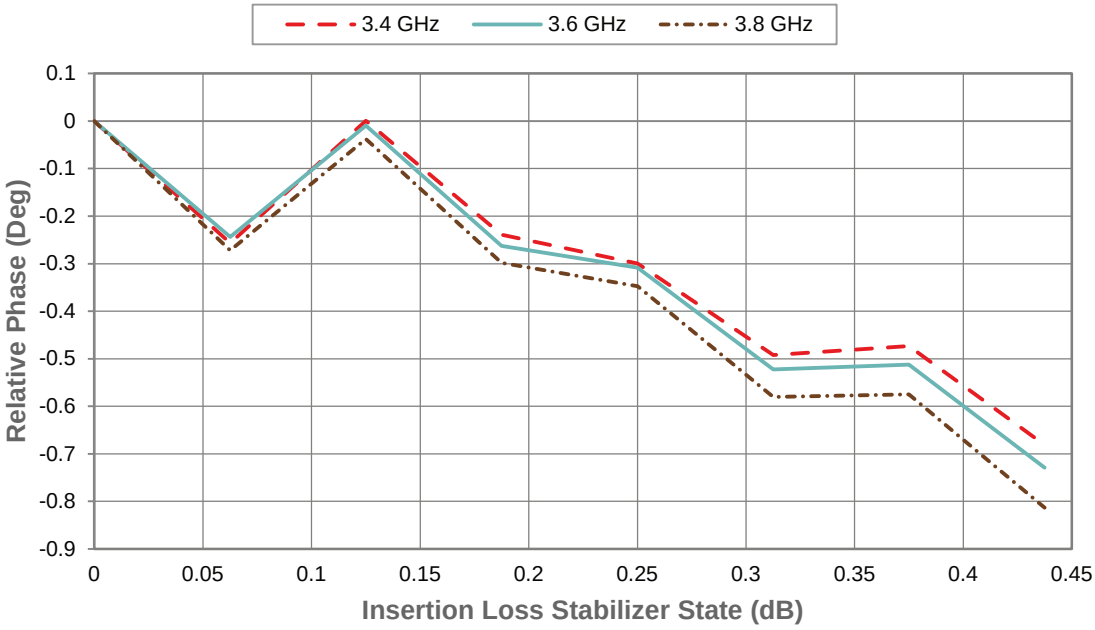


Figure 13 and Figure 14 illustrate the PE46130 RF_{IN} and RF_{OUT2} return loss at low, mid and high frequency versus the 7-bit emulated attenuator state. The phase setting is held at the reference state.

Figure 13 • *PE46130 RF_{IN} Input Return Loss vs RF_{OUT2} 7-bit Attenuation State*

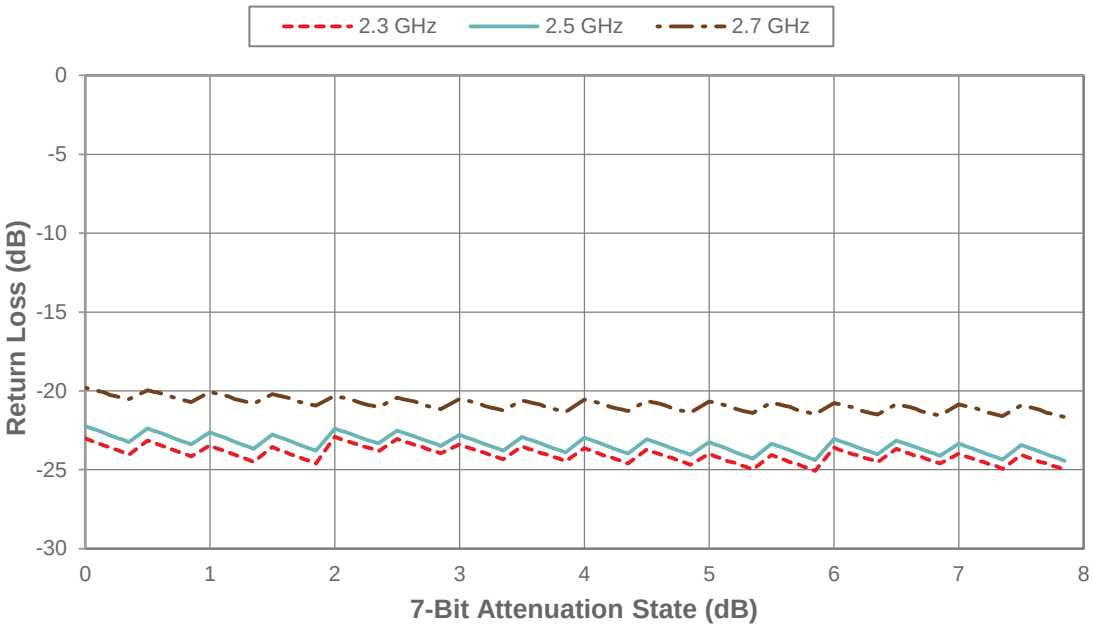
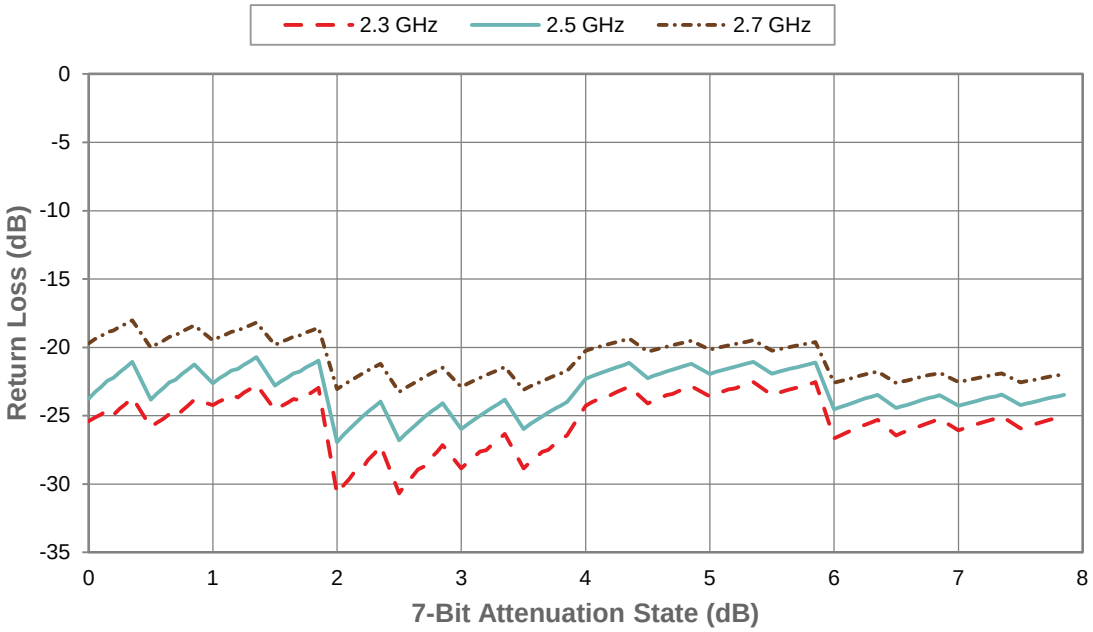


Figure 14 • *PE46130 RF_{OUT2} Output Return Loss vs RF_{OUT2} 7-bit Attenuation State*



RF_{OUT2} Insertion Loss Variation versus Phase Setting Optimization

The PE46130 and PE46140 digital phase shifters can be used in conjunction with the ILS bits to reduce the insertion loss variation when changing phase states. This is accomplished by characterizing the device 5-bit phase shifter states combined with the 3-bit ILS attenuation bits. The total number of states becomes 2^8, or 256 unique combinations, which are easily manageable. Creating a single lookup table with the 5-bit phase state as the key and the 3-bit ILS setting as the value can improve the insertion loss variation over the operating bandwidth of 2.3–2.7 GHz and 3.4–3.8 GHz for the PE46130 and PE16140, respectively. Creating multiple lookup tables covering partial bandwidth within the overall operating bandwidth can further reduce insertion loss variation.

Table 4 • *Insertion Loss Stabilizer Lookup Table (Partial)*

Lookup Key	Return Value	0.2	0.1	0.05	Total
Phase state	Opt ILS state	ILS2	ILS1	ILS0	ILS value (dB)
0	7	1	1	1	0.35
1	6	1	1	0	0.30
2	7	1	1	1	0.35
3	6	1	1	0	0.30
4	7	1	1	1	0.35
5	7	1	1	1	0.35
6	6	1	1	0	0.3
7	5	1	0	1	0.25
8	5	1	0	1	0.25
...	...	...	...	...	...
31	3	0	1	1	0.15

Programming Considerations

Programming the ILS bits is accomplished using the same 14-bit programming word used to program the attenuation and phase. **Table 5** and **Table 6** show the location of each of the ILS bits in the serial programming word. **Note:** These tables are a subset of the complete programming word and are presented for reference only.

Table 5 • *PE46130 Insertion Loss Stabilizer Bit Definition*

Programming Word Bit Location	Q11	Q1	Q0	
Bit definition	ILS2	ILS1	ILS0	
Attenuation value (dB)	0.2	0.1	0.05	ILS attenuation setting (dB)
	L	L	L	0.0
	L	L	H	0.05
	L	H	L	0.1
	H	L	L	0.2
	H	H	H	0.35

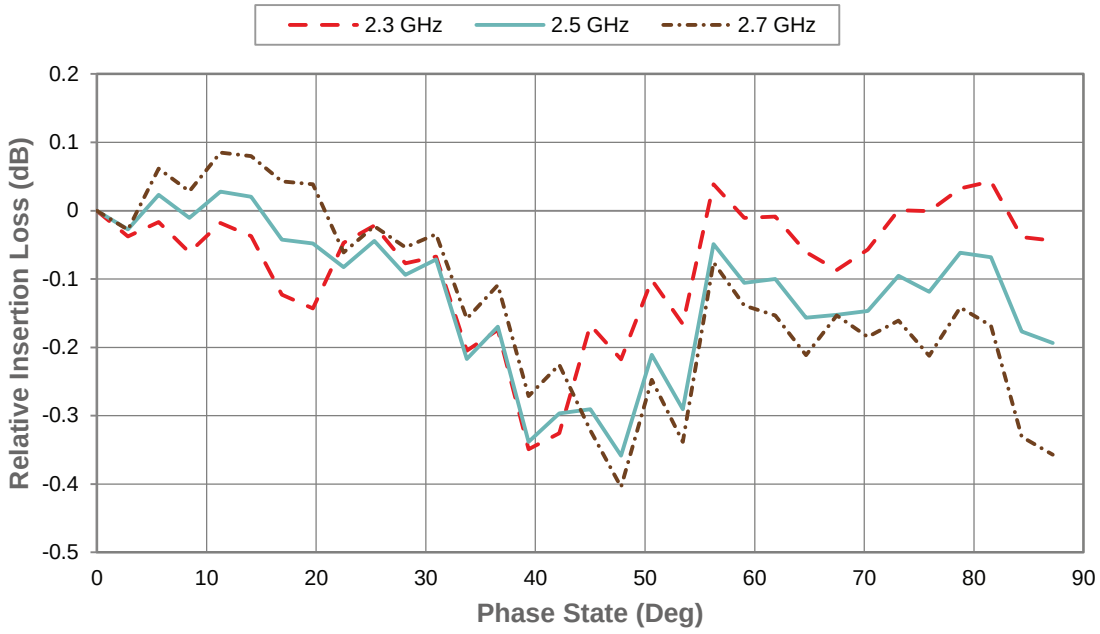
Table 6 • *PE46140 Insertion Loss Stabilizer Bit Definition*

Programming Word Bit Location	Q11	Q1	Q0	
Bit definition	ILS2	ILS1	ILS0	
Attenuation value (dB)	0.25	0.12	0.06	ILS attenuation setting (dB)
	L	L	L	0.0
	L	L	H	0.06
	L	H	L	0.12
	H	L	L	0.25
	H	H	H	0.44

Insertion Loss Flatness

Figure 15 illustrates the PE46130 insertion loss variation over the entire 5-bit phase state range (without the use of ILS bits). All ILS bits are programmed LOW, or at reference state. Three frequencies are presented: 2.3 GHz, 2.5 GHz and 2.7 GHz.

Figure 15 • *PE46130 RF_{IN}–RF_{OUT2} Attenuation Variation vs RF_{OUT2} 5-bit Phase State*



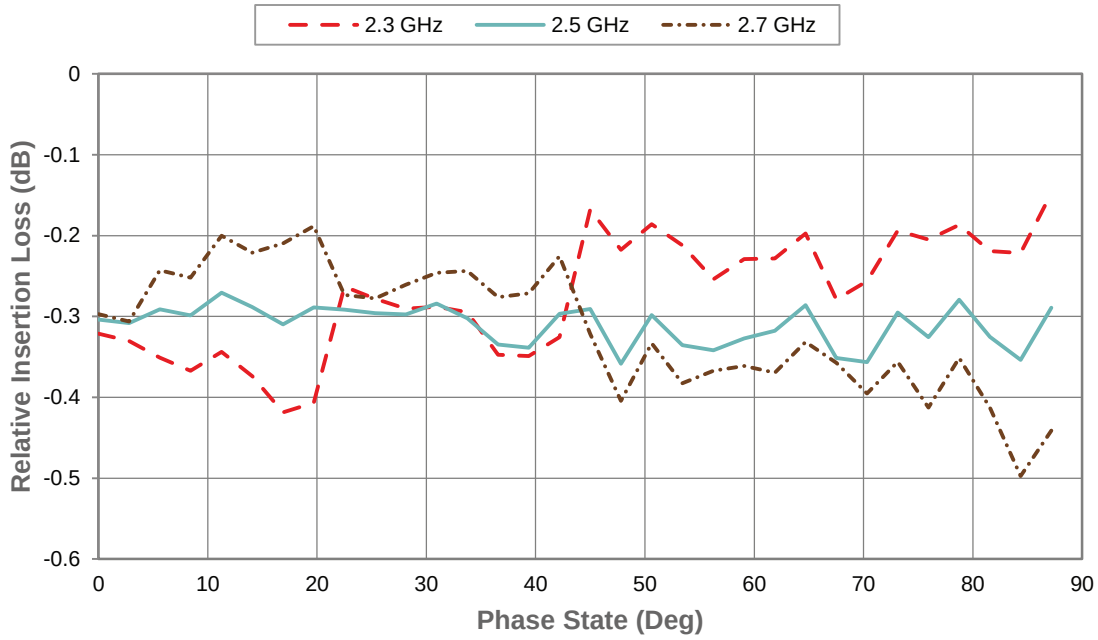
Insertion Loss Flatness with Single Lookup Table

By adding a single software-based lookup table to control the device ILS bits as a function of phase state, the attenuation variation of the phase shifter can be reduced. ILS changes the overall insertion loss when this approach is used. Given that typical MPAC circuit implementations perform a small amount of attenuation in the MPAC to compensate for board and other component gain or loss variation, the ILS insertion loss becomes part of the system amplitude calibration and does not present any additional issues.

Relative insertion loss is plotted versus the minimum (reference) state of the phase shifter, attenuator and ILS. Figure 16 demonstrates a single lookup table that has been optimized at 2.5 GHz and applied also at 2.3 GHz and 2.7 GHz using the lookup table shown in Table 5.

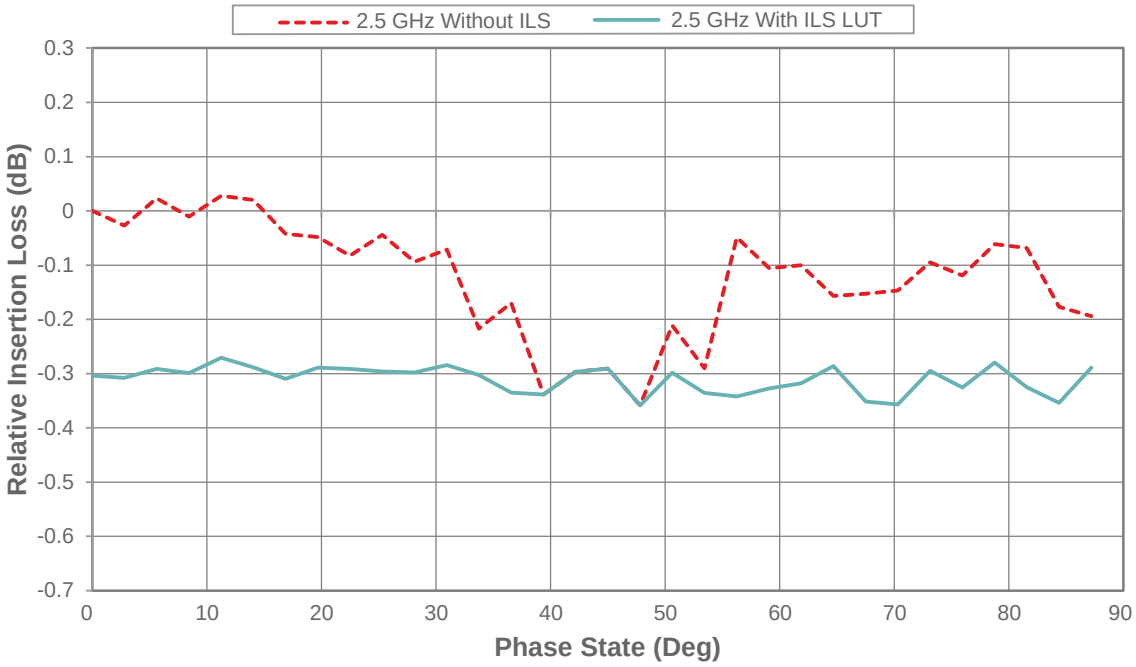
As demonstrated in Figure 16 and Figure 17, the ILS lookup table increases the overall insertion loss while reducing the excursions. The average insertion loss in Figure 16 and Figure 17 is approximately 0.3 dB. This increased relative insertion loss value (0.3 dB) is determined by the phase state setting with the highest insertion loss. Figure 15 (without ILS) illustrates the relative insertion loss between 39.375 and 47.8125 degrees is approximately 0.3 dB. The ILS lookup table shown in Table 4 applied in Figure 16 at 2.5 GHz activates additional ILS attenuation in phase states 0.0 to 36.5625 degrees and 50.625 to 87.125 degrees, which yields improved insertion loss flatness.

Figure 16 • *RF_{IN}–RF_{OUT2} Atten Variation vs RF_{OUT2} 5-bit Phase State—Single ILS Lookup Table*(*)



Note: * Optimized at 2.5 GHz.

Figure 17 • *RF_{IN}–RF_{OUT2} Atten Variation vs RF_{OUT2} 5-bit Phase State—2.5 GHz With and Without ILS Lookup Table*

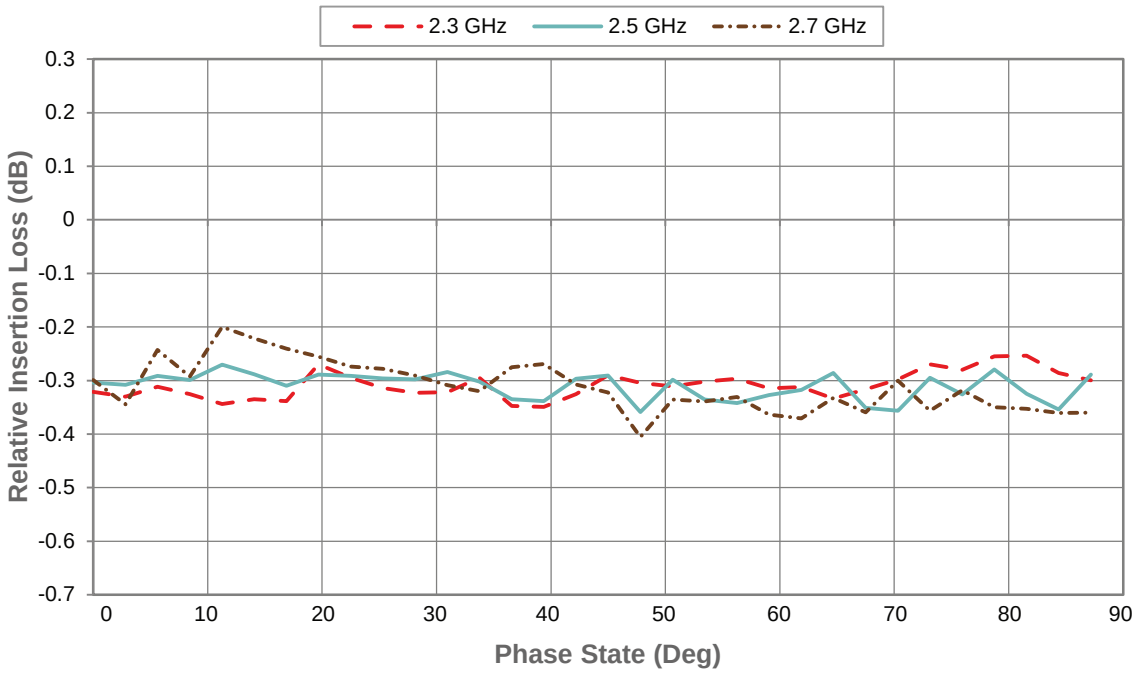


Insertion Loss Flatness with Multiple Lookup Tables

For applications that may benefit from minimizing the insertion loss variation over frequency, the system designer may choose to implement multiple software lookup tables to optimize the flatness with all the circuit loading effects.

Figure 18 demonstrates three individual lookup tables that have been optimized for 2.3 GHz, 2.5 GHz and 2.7 GHz and applied to the respective measurement frequency.

Figure 18 • *RF_{IN}–RF_{OUT2} Atten Variation vs RF_{OUT2} 5-bit Phase State—Multiple ILS Lookup Table*



Phase Accuracy with ILS Lookup Tables

ILS lookup tables have minimal effect on the phase accuracy. Figure 19 illustrates the relative phase accuracy with no lookup table (all ILS bits set to LOW or reference state). Figure 20 illustrates the PE46130 phase accuracy with a single ILS lookup table that has been optimized at 2.5 GHz and applied also at 2.3 GHz and 2.7 GHz using the lookup table shown in Table 7.

Figure 19 • *PE46130 RF_{IN}–RF_{OUT2} Relative Phase Error vs RF_{OUT2} 5-bit Phase State*

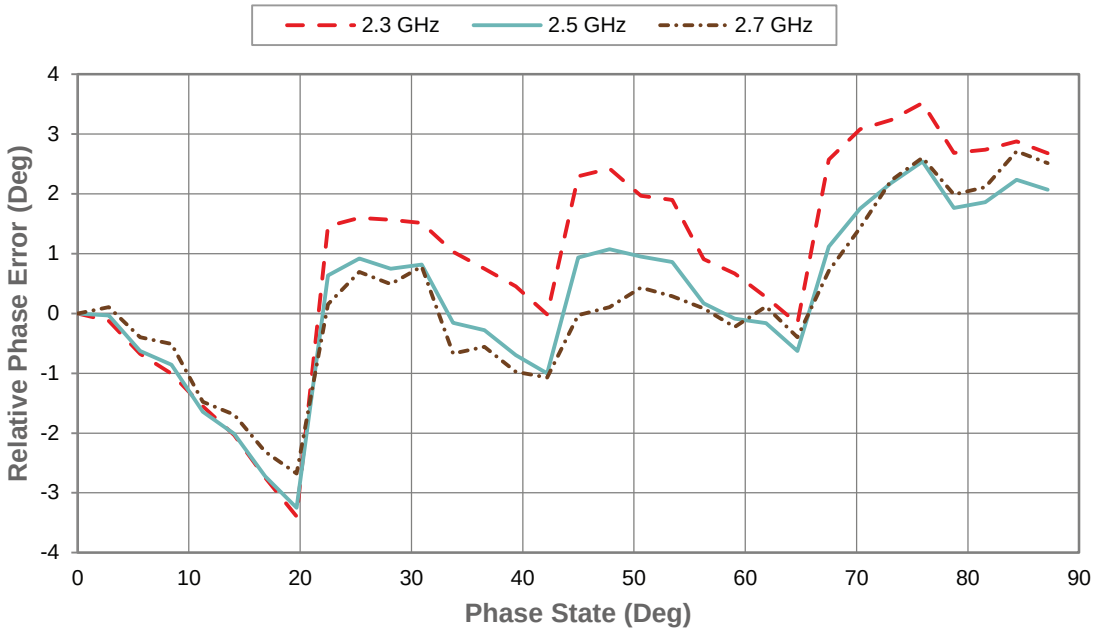
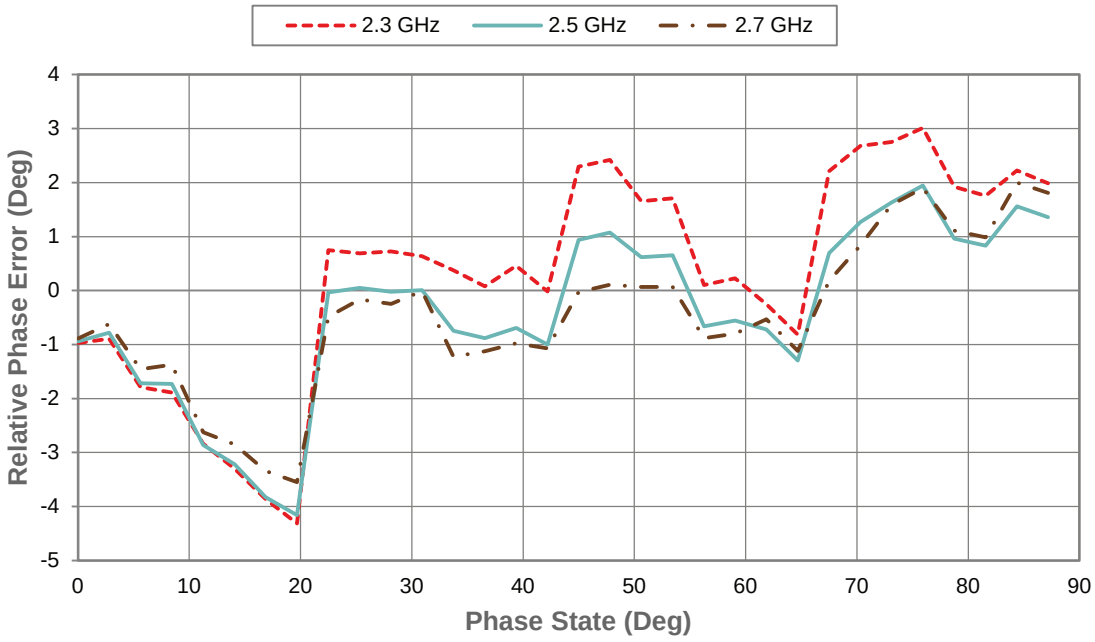


Figure 20 • *PE46130 RF_{IN}–RF_{OUT2} Relative Phase Error vs RF_{OUT2} 5-bit Phase State*(*)



Note: * Single lookup table optimized at 2.5 GHz.

Creating Lookup Tables

Lookup table creation can be accomplished by systematically comparing the insertion loss for each of the ILS states at the desired table frequency for each phase state. The starting insertion loss target is typically the highest insertion loss phase state at the target lookup table frequency. Optimization is accomplished by choosing the best ILS state that results in the lowest insertion loss variation to compensate for slight differences per phase bit and bit-to-bit impedance variations. The program or script searches the data matrix of S21 values versus phase state to find the closest ILS value that creates the flattest insertion loss response. The target insertion loss value may need to be reiterated during the search to evaluate results across several insertion loss solutions to find the flattest overall response. The resulting set of ILS attenuation values are organized into the lookup table.

Table 7 contains the lookup tables used in Figure 16 and Figure 18.

Table 7 • *PE46130 Multiple ILS Lookup Tables* (*)

Phase State (deg)	Phase State (int)	2.3 GHz ILS State	2.5 GHz ILS State	2.7 GHz ILS State
0	0	7	7	7
2.8125	1	6	6	7
5.625	2	6	7	7
8.4375	3	5	6	7
11.25	4	7	7	7
14.063	5	6	7	7
16.875	6	4	6	7
19.688	7	3	5	7
22.5	8	6	5	5
25.313	9	7	6	6
28.125	10	6	5	6
30.938	11	6	5	7
33.75	12	3	3	4
36.563	13	4	4	4
39.375	14	0	0	0
42.188	15	0	0	3
45	16	3	0	0
47.813	17	2	0	0
50.625	18	4	2	2
53.438	19	3	1	0
56.25	20	7	6	5
59.063	21	6	4	4

Table 7 • *PE46130 Multiple ILS Lookup Tables (Cont.)*[*]

Phase State (deg)	Phase State (int)	2.3 GHz ILS State	2.5 GHz ILS State	2.7 GHz ILS State
61.875	22	6	4	4
64.688	23	5	3	3
67.5	24	5	4	4
70.313	25	5	4	3
73.125	26	6	4	4
75.938	27	6	4	3
78.75	28	7	5	5
81.563	29	7	6	4
84.375	30	6	4	1
87.188	31	6	3	0

Note: * Optimized for 2.3 GHz, 2.5 GHz and 2.7 GHz on the evaluation board.

Memory Considerations

Each lookup table consists of a 5-bit index (the phase state) with the 3-bit ILS value stored in a 4-bit nibble. This 32-entry lookup table can be implemented in a byte array with length of 16, with the even lookup table index being stored in the lower 4-bit nibble and odd index in the upper 4-bit nibble of a single byte.

In the case of 32-bit memory layout, each 4-byte entry can be divided into nibbles to store 8 indexes. This would require a DWORD array with a length of 4.

Conclusion

The ILS feature can be used to emulate 7-bit attenuation control with resolution as low as 0.05 dB with no additional programming steps required. ILS can also be used to reduce the insertion loss across the RF_{OUT2} phase step range. A lookup table approach is shown to reduce the variation using a single table in wideband applications. A narrowband approach with multiple lookup tables is shown to further decrease the variation. Peregrine Semiconductor application support can supply custom lookup tables that are compatible with the evaluation kit software upon request.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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