UltraCMOS® Power Limiter Modes and Applications

Application Note 54

Summary

Peregrine Semiconductor's UltraCMOS® power limiters provide a monolithic alternative to discrete, PIN-diode limiters. They reduce design complexity by offering a drop-in solution with no external bias components. Peregrine's power limiters have two operating modes—power limiting and power reflecting. They feature adjustable P1dB threshold, high linearity performance, fast response and recovery time and superior ESD protection. Application examples include test and measurement (T&M) equipment, communication radio frequency front-end (RFFE) modules and weather radar protection.

Introduction

Excessive RF power, intentional jamming and ESD events can wreak havoc on an electronic device. As a result, RF designers for applications such as T&M equipment, RFFE modules, land mobile radios (LMRs) and radar systems must take steps to ensure the power reliability of their devices. These types of applications require repeatable and reliable power protection.

To protect circuitry, power-limiting devices are used to reduce the extra signal strength that might damage the rest of a design's components. Below a threshold (P1dB) level, the limiter passes the input signal to the output without attenuation. At the threshold, the limiter "limits" the amount of input power that is passed to the output, up to the maximum power.

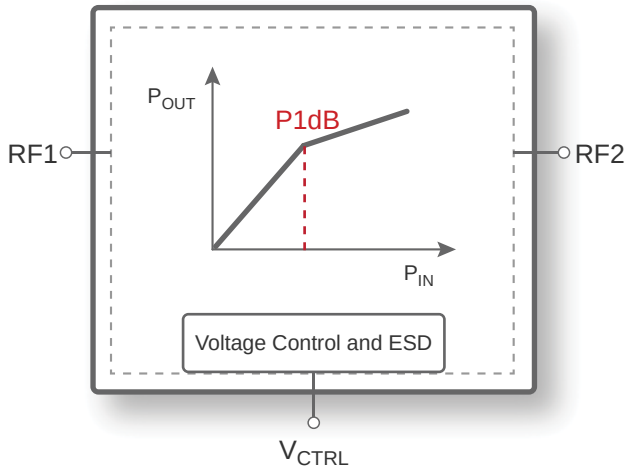
Traditionally, the industry has relied on PIN-diode power limiter circuits and multiple external components to deliver power protection. With a PIN diode, the input signal is shunted to ground. PIN diodes are known for their high maximum power handling and low insertion loss. But PIN diodes are also plagued with slow response and recovery time, poor linearity, low ESD ratings and require DC blocking capacitors. Additionally, PIN diodes take a significant amount of time to design and validate and cannot be easily integrated into a system.

Peregrine's UltraCMOS power limiters provide an all-in-one solution and are a simple and reliable alternative to discrete, PIN-diode limiters. Compared to PIN diodes, UltraCMOS power limiters provide a 10–100x improvement in response and recovery time, deliver a greater than 10–30 dB linearity (IIP3) improvement and offer a 20x improvement in ESD protection. In addition, UltraCMOS power limiters are 8x smaller than the board space required by PIN-diode solutions. Finally, the limiting threshold can be adjusted through a high impedance voltage control pin (V_{CTRL}), eliminating the need for external components such as DC blocking capacitors, RF choke inductors and bias resistors.

Operating Modes

UltraCMOS power limiters have symmetric RF ports that limit incident power in both biased and unbiased conditions (Figure 1). The devices feature two operating modes—power limiting and power reflecting—to maximize performance and flexibility. The operating mode can be selected through the V_{CTRL} pin.

*Figure 1 • **Product Symbol***

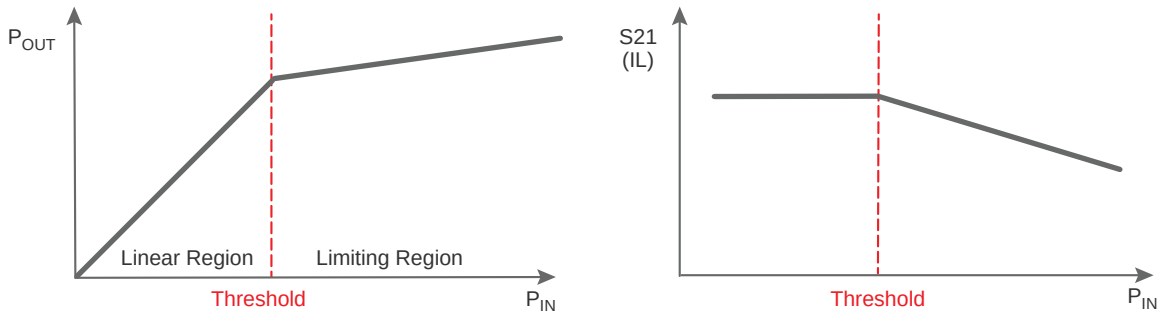


For effective power limiter operation, certain parameters and capabilities must be considered. These considerations include insertion loss, power threshold, ESD protection, power transfer curves and transient characteristics.

Power Limiting Mode

In power limiting mode, the UltraCMOS power limiter is operated within two regions as shown in Figure 2—the linear region and the limiting region. The threshold is adjusted through the V_{CTRL} pin that provides flexibility in the limiting behavior compared to PIN-diode limiters. Peregrine's power limiters act as a diode limiter without an external sensor or loop control requirement.

*Figure 2 • **Power Limiting Mode Operation***



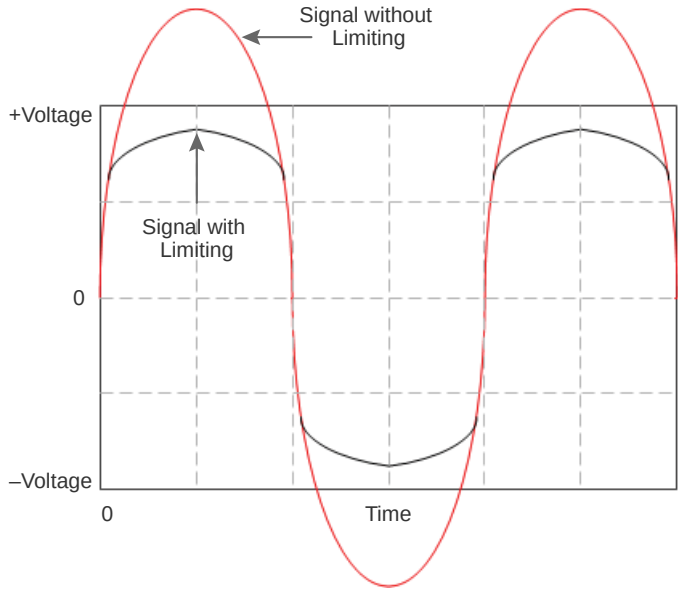
Linear Region

In the linear region (Figure 2), the UltraCMOS power limiter is invisible to the load, and it features very low insertion loss and high linearity. Insertion loss defines the small signal throughput loss (S21) of the limiter. The Peregrine power limiter demonstrates excellent linearity with HaRP™ technology, and delivers 10–30 dB higher IIP3 than PIN diodes at the same P1dB level. These monolithic power limiters also have fast response and recovery times that are typically one nanosecond (1 ns).

Limiting Region

Regarding limiting region operation (Figure 2), when the incoming RF signal power exceeds the limiting threshold set through the V_{CTRL} pin, the device limits the input power. Large signal amplitude results in higher gate voltage and the saturation or breakdown of transistors. The limiting effect occurs at both the positive and negative peak of the signal and is symmetrical on both peaks (Figure 3).

*Figure 3 • **Limiting Region Operation***

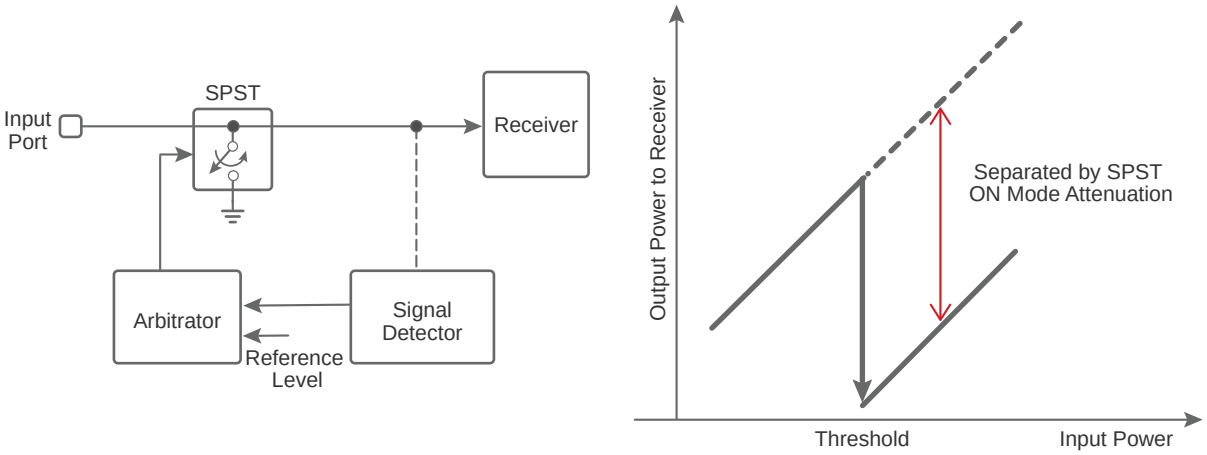


Power Reflecting Mode

In power reflecting mode, the UltraCMOS power limiter is used for power protection in extreme conditions, and the device reflects most of the incident power back to the source. In this mode, the power limiter is acting as a shunt SPST.

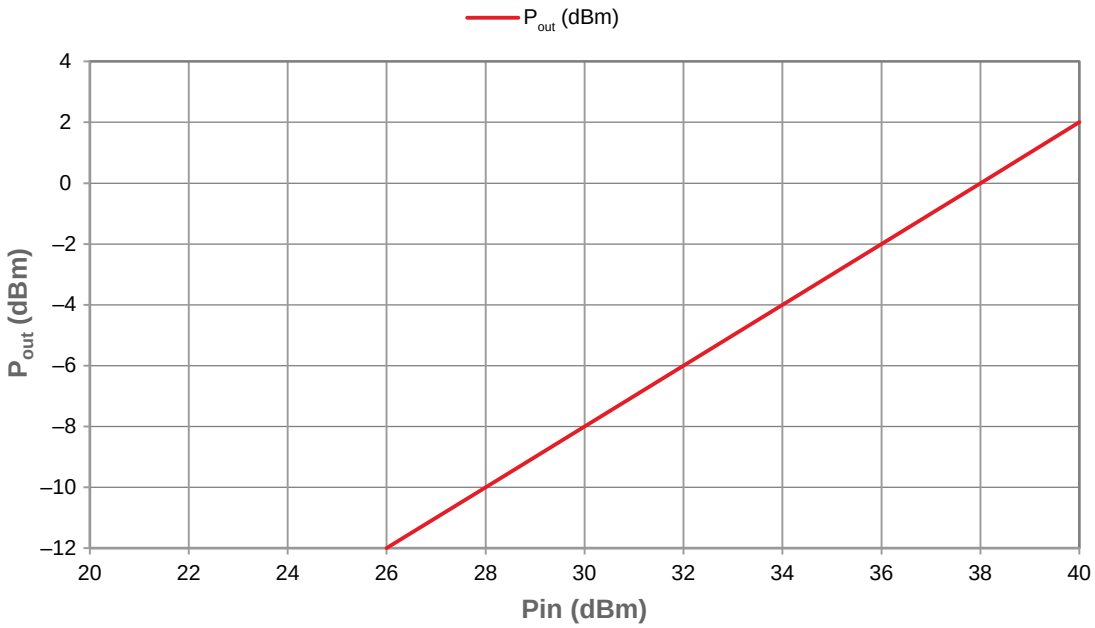
When using a shunt SPST switch for protection, the SPST switch is off (**Figure 4**) during normal receive operation. The system monitors the input power level and compares it with a preset reference level. When input power reaches that level, the system instructs the SPST switch to turn on, shorting the input to ground. When the SPST switch is on and shorting the signal to ground, the system loses its ability to monitor input power. It must periodically turn off the SPST switch to check the input level condition.

Figure 4 • Using a Shunt SPST Switch for Protection



When an UltraCMOS power limiter is used as a shunt SPST switch (Figure 5), V_{CTRL} is set to 2.5–3.3V to turn the switch ON and V_{CTRL} is set to –2.5 to –3.3V to turn the switch OFF. IIP3 is greater than 60 dBm in the OFF state and the ON mode attenuation is approximately 40 dB. Switching time is 0.1–1 ms.

*Figure 5 • **SPST Switch Mode***



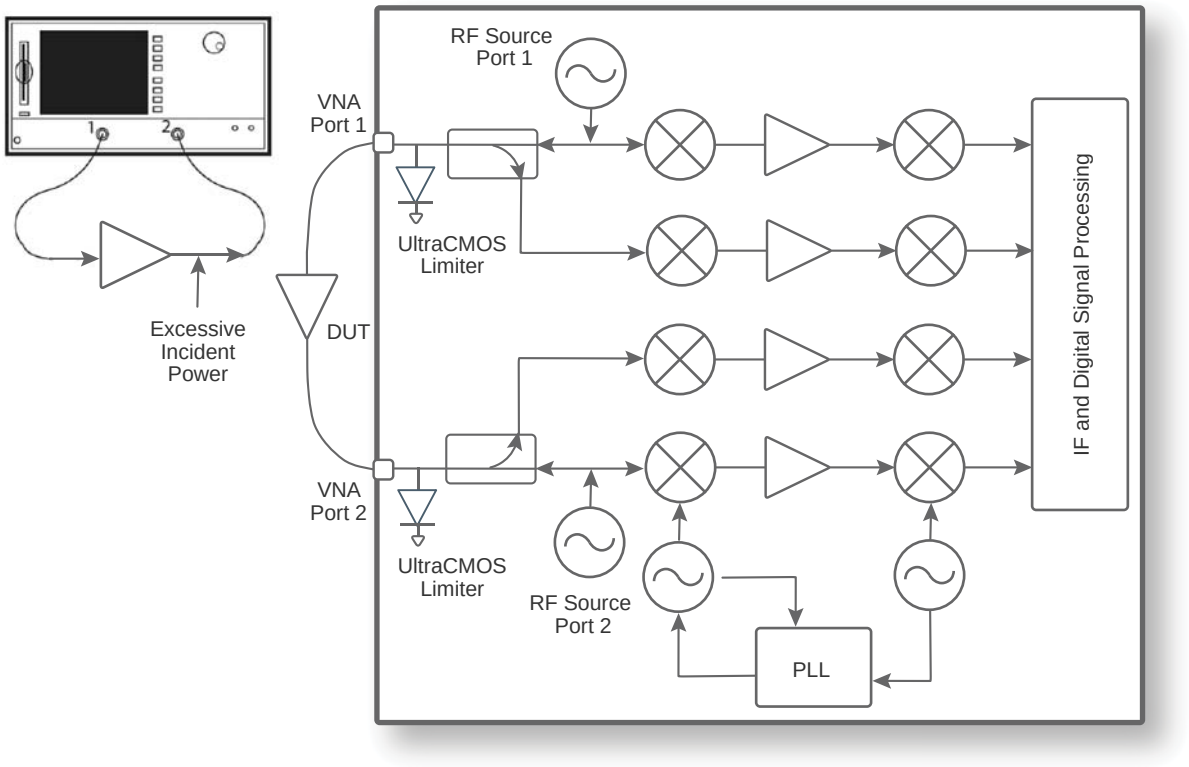
Applications

Power limiters offer repeatable and reliable power protection to applications such as T&M equipment, communication RFFE modules and weather radar protection.

Application 1: Test and Measurement

Measurement equipment needs a power limiter to protect RF ports from unexpected power surges (Figure 6). Peregrine's power limiters feature a high threshold (P1dB greater than 25 dBm) and high linearity in the linear region. UltraCMOS power limiters are effective in the case of unpredictable continuous wave stress duration, and the limiter's ESD capability is also valuable to a T&M system.

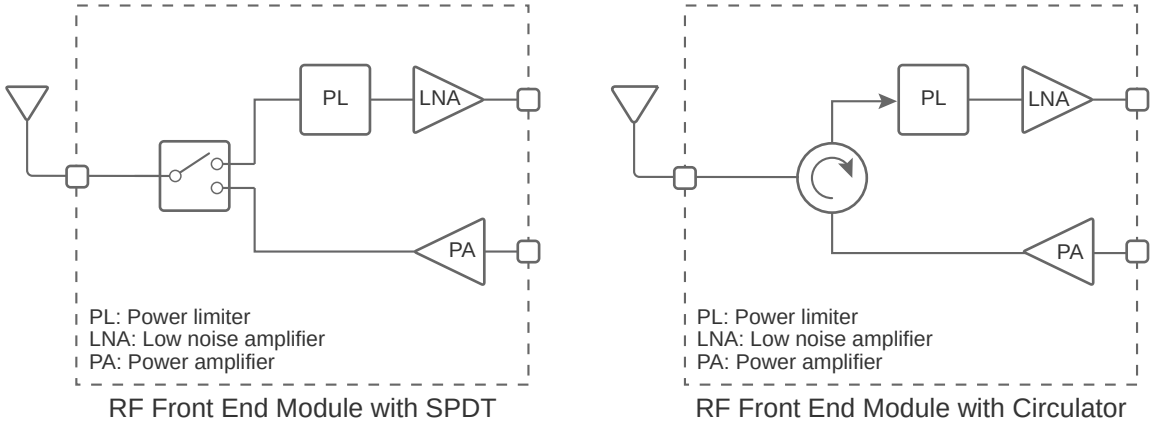
*Figure 6 • **Test and Measurement***



Application 2: Communication RFFE Module

In a communication RFFE module, the maximum power is defined by the power amplifier (PA) output power level (Figure 7). To protect the low noise amplifier (LNA) input as well as provide some isolation of the receive (RX) to transmit (TX) paths, either an SPDT switch or a circulator is used to establish the isolation level. However, the TX leakage signal level can put a strain on LNA devices, especially when reflected power upsets the steady state isolation level. With Peregrine's power limiters, flat leakage for the LNA can be assured to be typically 15 dBm or lower. While in steady state the IIP3 is 45 dBm or higher with greater than 60 dBm being possible.

*Figure 7 • **Communication RFFE Module***



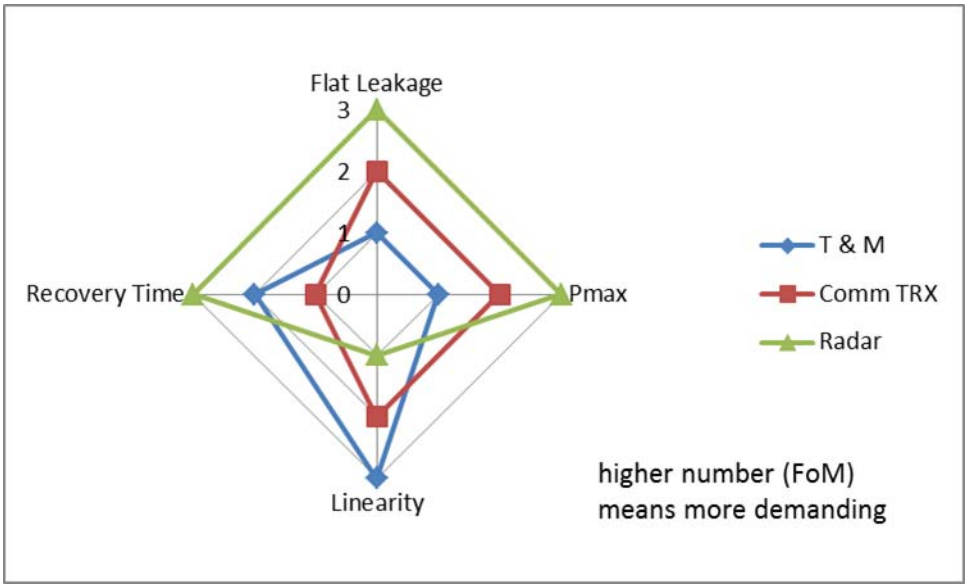
Application 3: Weather Radar Protection

Weather radar applications require a limiter to handle varying high power stress, particularly in the case of pulsed jamming. Additionally, weather radar applications require fast response and recovery times, and the 1 ns response time supports this.

Additional Application Requirements

Figure 8 depicts the weighting of several limiter performance requirements. Performance requirements have different parameters depending on the application. Common factors are extremely low insertion loss and exceptional return loss. As the limiter is intended to cause minimal impact to the system performance during steady state with low incident power signals, maintaining these levels while providing high IIP3 linearity is critical.

*Figure 8 • **Additional Application Requirements***



Conclusion

UltraCMOS power limiters feature adjustable P1dB threshold, high linearity performance, fast response and recovery time and superior ESD protection. These power limiters have two operating modes—power limiting and power reflecting. Application examples discussed include T&M equipment, communication RFFE modules and weather radar protection.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

Peregrine products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark