PE43508 55 GHz DSA
Substrate Carrier Assembly Guide

Application Note 78

Summary

This application note describes how the PE43508 enables high RF performance and monotonicity to 55 GHz. This document provides recommended landing patterns, describes assembly details, and presents a measurement summary.

Introduction

The PE43508 is a 50Ω, HaRP™ technology-enhanced, 6-bit RF digital step attenuator (DSA) that supports a wide frequency range from 9 kHz to 55 GHz. The PE43508 covers a 31.5 dB attenuation range in 0.5 dB and 1 dB steps. It is capable of maintaining 0.5 dB and 1 dB monotonicity through 55 GHz. The PE43508 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology. pSemi's HaRP technology enhancements deliver high power handling and high linearity performance.

To achieve the attenuation range, accuracy, and monotonicity through 55 GHz, nothing can be taken for granted in the assembly of the PE43508 into higher-level assemblies. This application note provides design details related to the recommended landing pattern and the assembly process for obtaining the peak performance of the PE43508 DSA.

Product Overview

The PE43508 is a flip-chip DSA that utilizes lead-free solder ball technology to provide the signal and ground interconnect. Solder reflow profiles common to lead-free surface-mount device (SMD) assembly can readily be used to achieve uniform and reliable attachment. Since the material composition of the DSA is similar to alumina, Al_2O_3 aluminum oxide, the coefficients of thermal expansion for the two materials are similar, 5–7 ppm / °C (or 5–7 × 10^{-6} / °K), resulting in a mechanically reliable and robust interconnect.

Pin Configuration

The pin configuration for the PE43508 is shown in **Figure 1** while the detailed pin descriptions are listed in **Table 1**. The pin configuration is such that a minimum of 500 µm (0.5 mm) pitch is maintained between all unique signal pads to permit ease of routing and manufacturing. All pin locations originate from the die center and refer to the center of the pin, and are referenced with the bumps facing up.

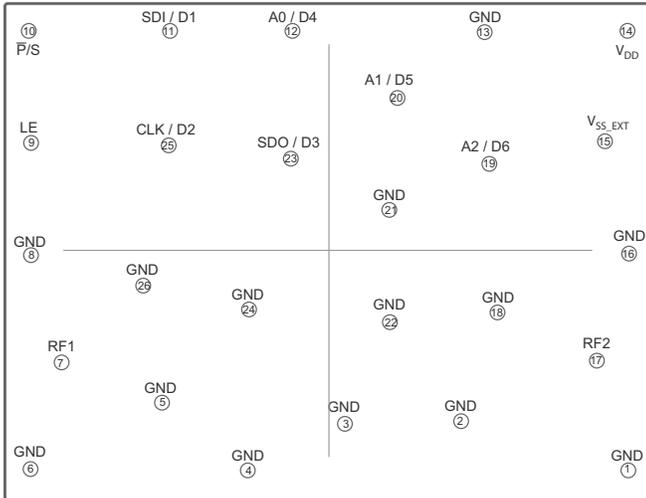*Figure 1* ▪ *Pin Configuration (Bumps Up) for the PE43508*

Table 1 ▪ *Pin Coordinates for the PE43508*

Pin No.	Pin Name	Description	Pin Center (µm)	
			X	Y
1	GND	Ground	1397.760	−985.005
2	GND	Ground	621.680	−767.980
3	GND	Ground	80.290	−782.555
4	GND	Ground	−375.400	−994.535
5	GND	Ground	−776.255	−693.460
6	GND	Ground	−1386.755	−985.005
7	RF1	RF1 port[1]	−1239.910	−504.810
8	GND	Ground	−1386.755	−24.480
9	LE	Serial/parallel interface latch enable input	−1386.985	476.250
10	$\overline{P}$/S	Serial/parallel mode select[2]	−1399.635	977.150
11	SD1/D1	Serial interface data input/parallel control bit, 0.5 dB	−732.120	977.150
12	A0/D4	Address bit A0 connection/parallel control bit, 4 dB[2]	−167.870	977.150
13	GND	Ground	727.870	977.150
14	V_{DD}	Supply voltage	1395.190	977.150

Table 1 ▪ *Pin Coordinates for the PE43508 (Cont.)*

Pin No.	Pin Name	Description	Pin Center (μm)	
			X	Y
15	V_{SS_EXT}	External V_{SS} negative voltage control[3]	1288.820	487.020
16	GND	Ground	1397.760	−24.480
17	RF2	RF2 port[1]	1252.620	−505.905
18	GND	Ground	788.690	−280.620
19	A2/D6	Address bit A2 connection/parallel control bit, 16 dB[2]	753.100	383.070
20	A1/D5	Address bit A1 connection/parallel control bit, 8 dB[2]	323.530	677.170
21	GND	Ground	287.050	178.310
22	GND	Ground	285.870	−326.035
23	SDO/D3	Serial interface data output/parallel control bit, 2 dB	−168.360	404.800
24	GND	Ground	−372.300	−267.810
25	CLK/D2	Serial interface clock input/parallel control bit, 1 dB	−749.140	468.770
26	GND	Ground	−862.865	−169.675

1) RF pins 7 and 17 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC require-ment is met.

2) P/S (pin 10), A0/D4 (pin 12), A2/D6 (pin 19) and A1/D5 (pin 20) have internal 1.5 MΩ pull-up resistor to internal 1.8V V_{DD}. These pins will have an internal logic HIGH on them if they are left floating by the user. In serial mode, the user can leave the P/S pin float-ing and the part will default to serial mode.

3) Use V_{SS_EXT} (pin 15) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 15) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Landing Patterns

The PE43508 is configured with a 0.5 mm, or 500 μm, minimum bump pitch. Thin film technologies can readily meet the line width and spacing critical dimensions (CD) of 100 μm or less, but other thick film and printed circuit board (PCB) processes generally require far less stringent CDs to reach reasonable and consistent manufac-turing yields. The comparatively wide 500 μm bump pitch is intended to support the larger CD requirements and enable assembly of the die directly to RF PCBs.

To obtain the best microwave performance, specific metallization and via patterns have been defined and imple-mented to provide measured results for the PE43508.

Alumina Substrates: PRT-69886 and PRT-69887

The first recommended landing pattern for use with the PE43508 and an alumina substrate is shown in **Figure 2**. The landing pattern is identified as PRT- 69886 and is designed for a 254 µm (10 mil) alumina substrate. The PRT-69886 landing pattern is used in the customer evaluation kit EK43508-01.

Figure 2 ▪ PRT-69886 Landing Pattern for the PE43508 Using 10 mil Alumina Substrate
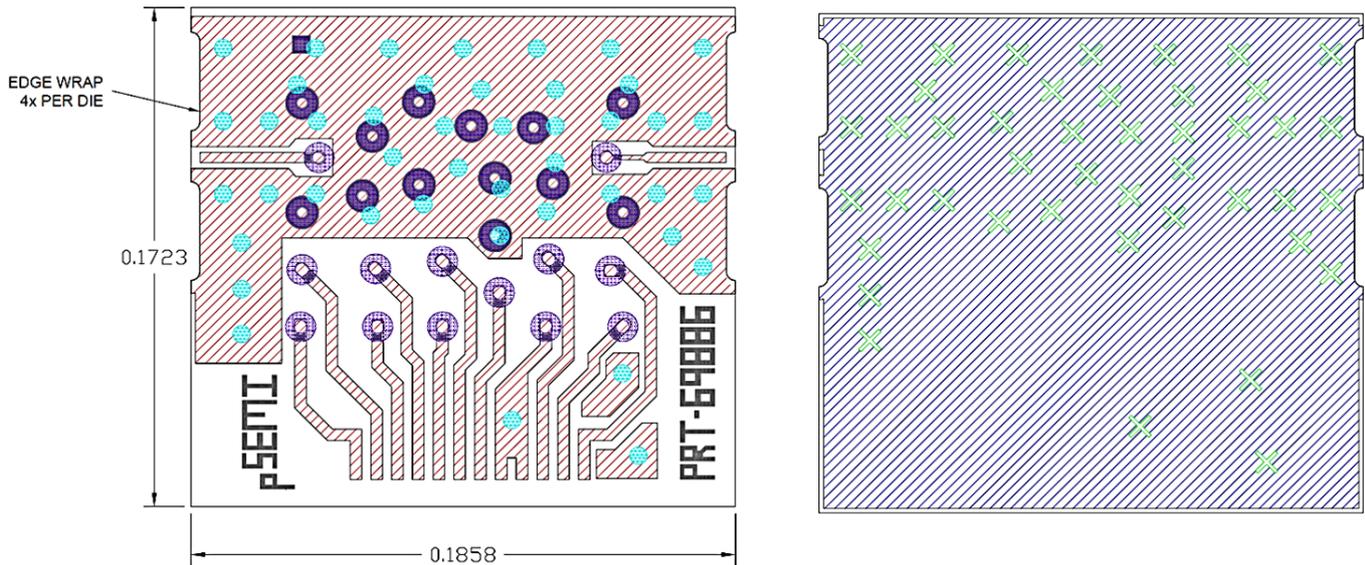

Drawing notes:

- Material is polished alumina 254 µm (0.010") thick.
- Metallization (top side and bottom side): TiW (1000-1500A), Ni(5A), Au(38A)
- Polyimide (solder mask): Small rings with openings in the center of the polyimide. Opening size of 113 µm (4.45 mil) approximately.
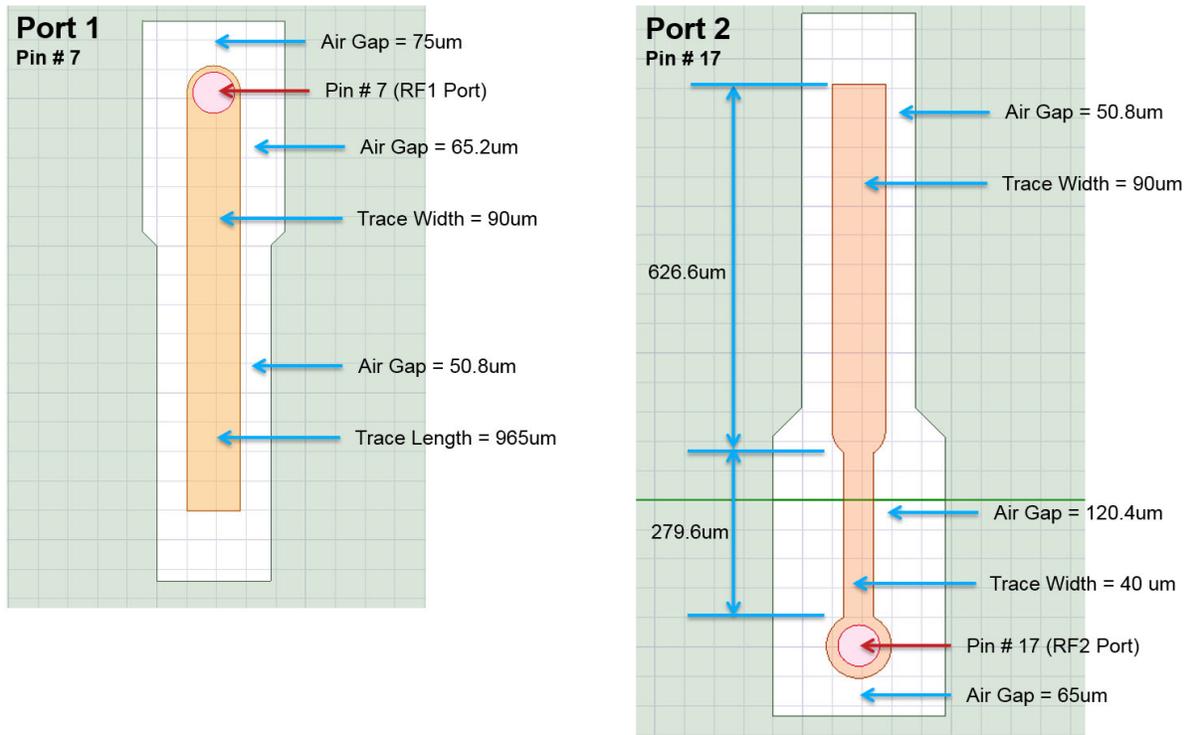- Pin#1 indicator (square) added using solder mask layer.

The corresponding pin out of the PRT-69886 substrate is shown in **Figure 3**.

Figure 3 ▪ *PE43508 Pin Connection Detail Using the PRT-69886 Landing Pattern*
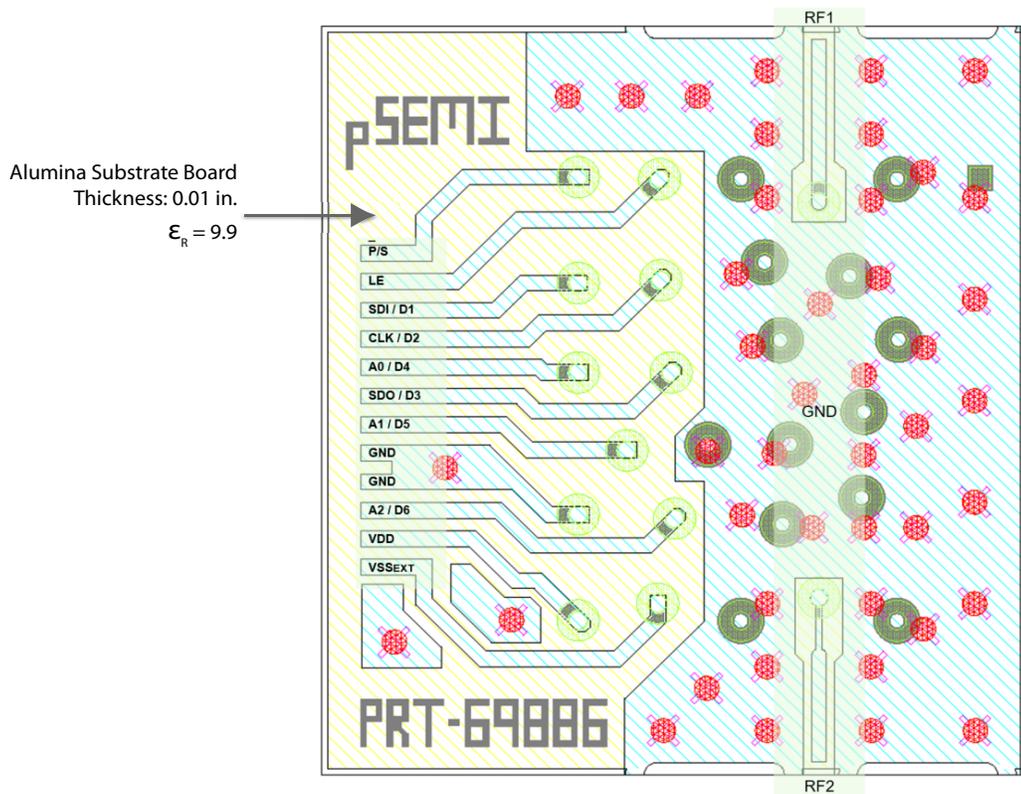
Dimensional detail of the RF ports is shown in **Figure 4**.

Figure 4 ▪ Dimensional Detail of the RF Ports Used in the PRT-69886 Landing Pattern

As shown in **Figure 4**, the RF1 Port (pin 7) uses a CPW trace length of 965 µm (38 mil) with trace width of 90 µm (3.54 mil) and signal-to-ground spacing of 50.8 µm (2 mil). This signal trace width and signal-to-ground spacing should approximately give 50Ω for the defined alumina stack.

The RF2 port (pin 17) uses a 50Ω CPW trace length of 627 µm (24.7 mil) of the same dimension as described above for RF1 port (pin 7). Between the 50Ω trace and the RF2 port pad (pin17), an inductive trace of a width of 40 µm (1.6 mil) and a length of 279 µm (11 mil) is used to provide a broadband match required for this port.

The recommended solder bump opening for the alumina substrate is described in **Figure 5**. The typical diameter of the solder bump of the PE43508 die is 91 µm (3.6 mil). The solder opening for the bumps is approximately 113 µm (4.45 mil) for the alumina substrate.

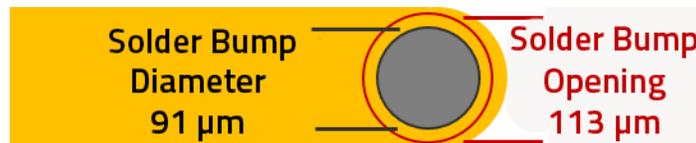*Figure 5 ▪ Solder Bump Opening Detail of the PRT-69886 Landing Pattern*

Figure 6 shows the PRT-69886 alumina substrate unpopulated and populated with the PE43508 DSA flip chip IC. As can be seen in the unpopulated substrate view, a solder stop layer is used to provide control over solder wicking away from the bump pad. The recommended solder stop opening is 113 µm (4.45 mil).

Figure 6 ▪ Unpopulated PRT-69886 Substrate and Populated Assembly with PE43508
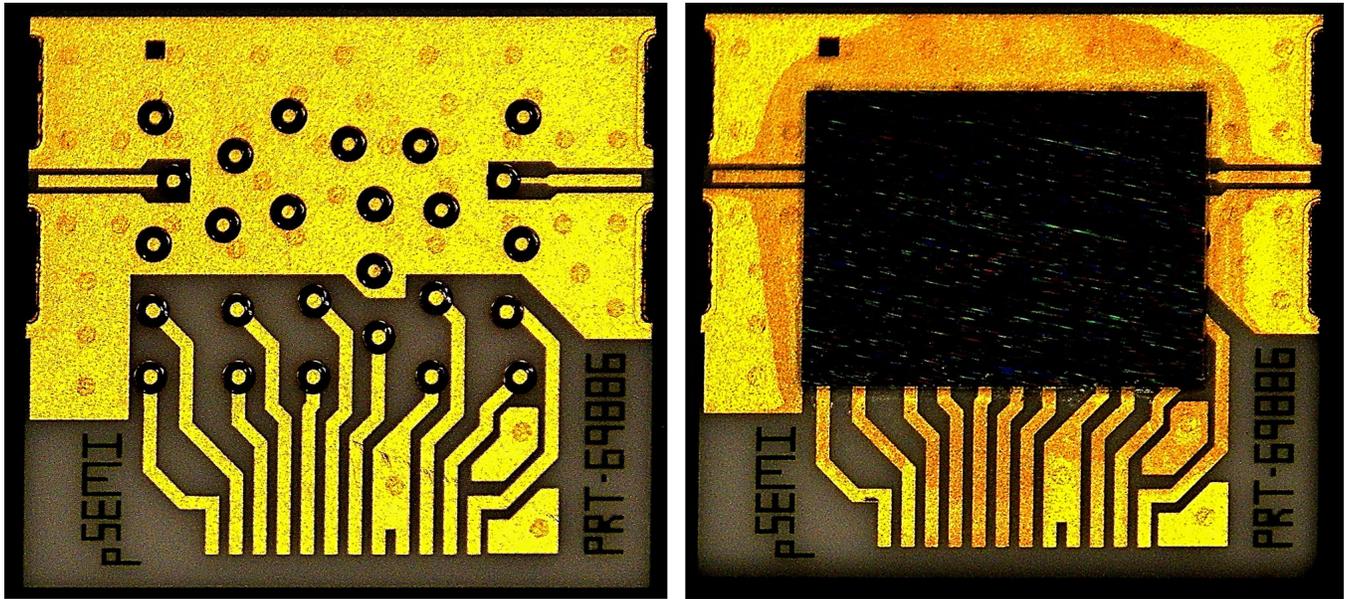
The second recommended landing pattern for use with the PE43508 and an alumina substrate is shown in **Figure 7**. The landing pattern is identified as PRT- 69887, is designed for a 254 μm (10 mil) alumina substrate, and has a modified RF2 port trace to aid performance at the high end of the operating frequency range. The PRT-69887 landing pattern is used in the customer evaluation kit EK43508-02.

Figure 7 ▪ PRT-69887 Landing Pattern for the PE43508 Using 254 μm (10 mil) Alumina Substrate
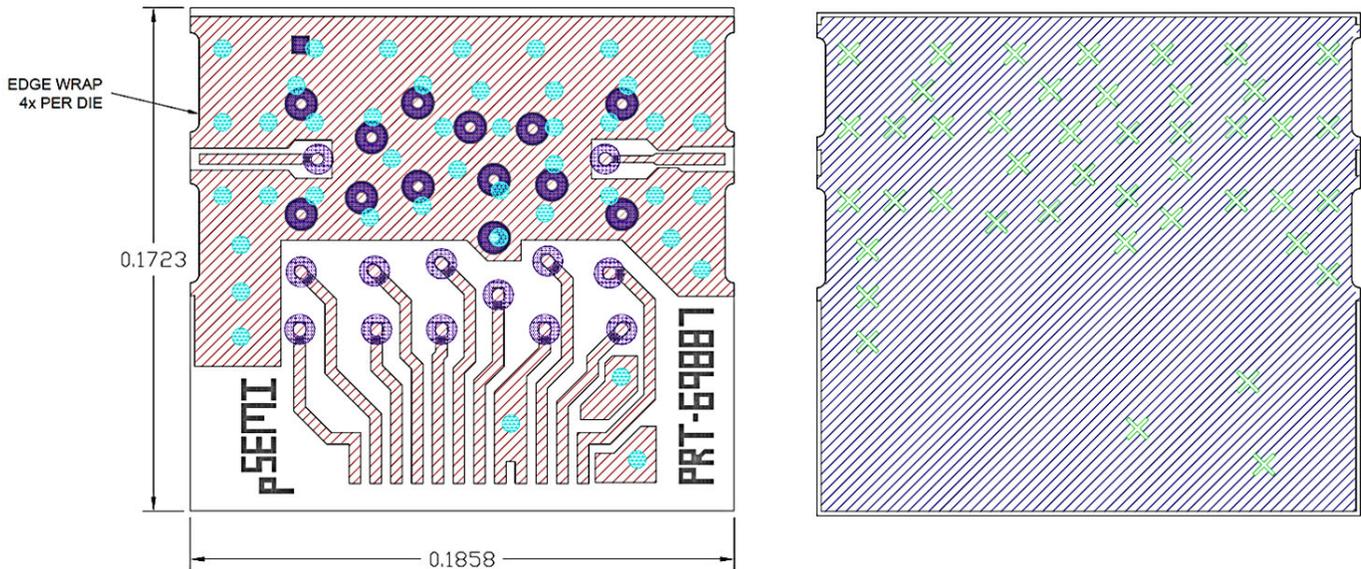

Drawing Notes:

- Material is polished alumina 254 μm (0.010") thick.
- Metallization (top side and bottom side): TiW (1000-1500A), Ni (5A), Au (38A)
- Polyimide (solder mask): Small rings with openings in the center of the polyimide. Opening size of 113 μm (4.45 mil) approximately
- Pin 1 indicator (square) added using solder mask layer
- Modified RF2 port trace compared to PRT-69886

The corresponding pin out of the PRT-69887 substrate is shown in **Figure 8**.

Figure 8 ▪ PE43508 Pin Connection Detail Using the PRT-69887 Landing Pattern

Alumina Substrate Board
Thickness: 0.01 in.
$\varepsilon_R = 9.9$
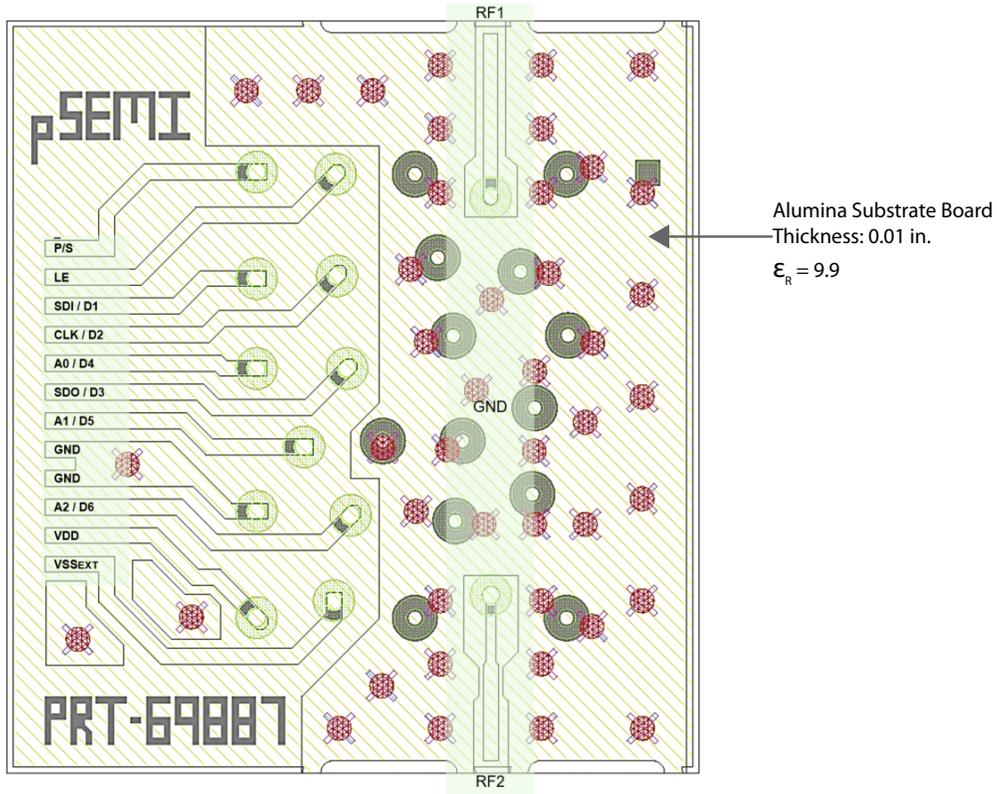
Dimensional detail of the RF ports is shown in **Figure 9** for both RF1 and RF2 ports, pins 7 and 17 of the PRT-69887 landing pattern.

*Figure 9 ▪ Dimensional Detail of the RF Ports used in the PRT-69887 Landing Pattern*
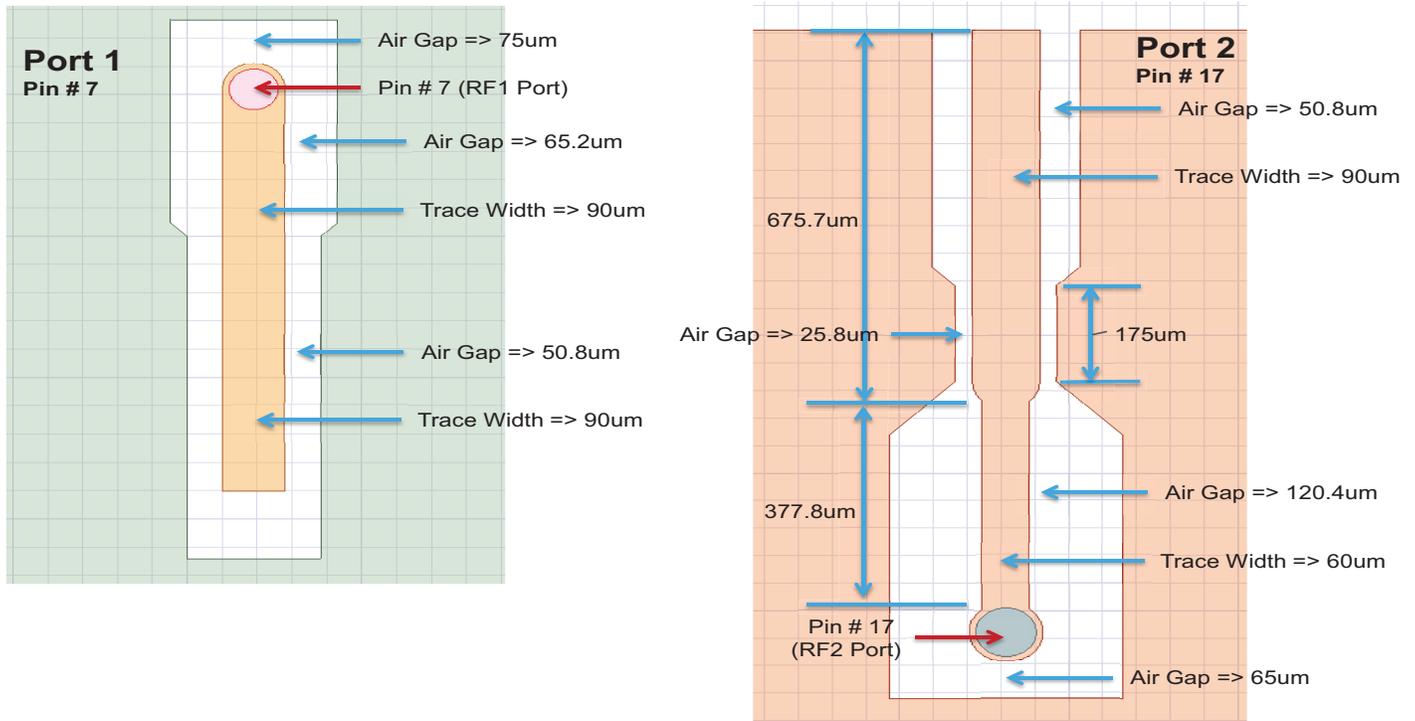
As shown in **Figure 9**, the RF1 port (pin 7) uses a CPW trace length of 965 µm (38 mil) with a trace width of 90 µm (3.54 mil) and signal-to-ground spacing of 50.8 µm (2 mil). This signal trace width and signal-to-ground spacing should approximately give 50Ω for the defined alumina stack.

The RF2 port (pin 17) uses a 50Ω CPW trace length of 452 µm (17.8 mil) of the same dimension as described above for RF1 port (pin 7). Between the 50Ω trace and rest of the RF2 port connection is a capacitive line having a trace width of 90 µm (3.54 mil) and an air gap of 25.8 µm (1.01 mil). Finally, an inductive trace of width of 60 µm (2.36 mil), a length of 378 µm (14.9 mil) and an air gap of 120 µm (4.72 mil) is connected from the previous CPW line to the RF2 port of the PE43508. This interconnection is done to improve the high frequency match of the RF2 port. The PRT-69886 and PRT-69887 layouts in .dxf format can be downloaded from the PE43508 product page on the pSemi website.

## Probe Printed Circuit Board Using Rogers RO4003C™ Substrate

A metallization and via pattern has also been generated for a Rogers 4003 substrate shown in **Figure 10**. This board layout is configured to create an RF-probable PCB. The measured performance of the PE43508, when assembled to the PCB and properly de-embedded, results in performance that is comparable to that achieved using the alumina-based substrate designs.

Figure 10 ▪ PE43508 Pin Connection Detail Using the Probe PCB Landing Pattern
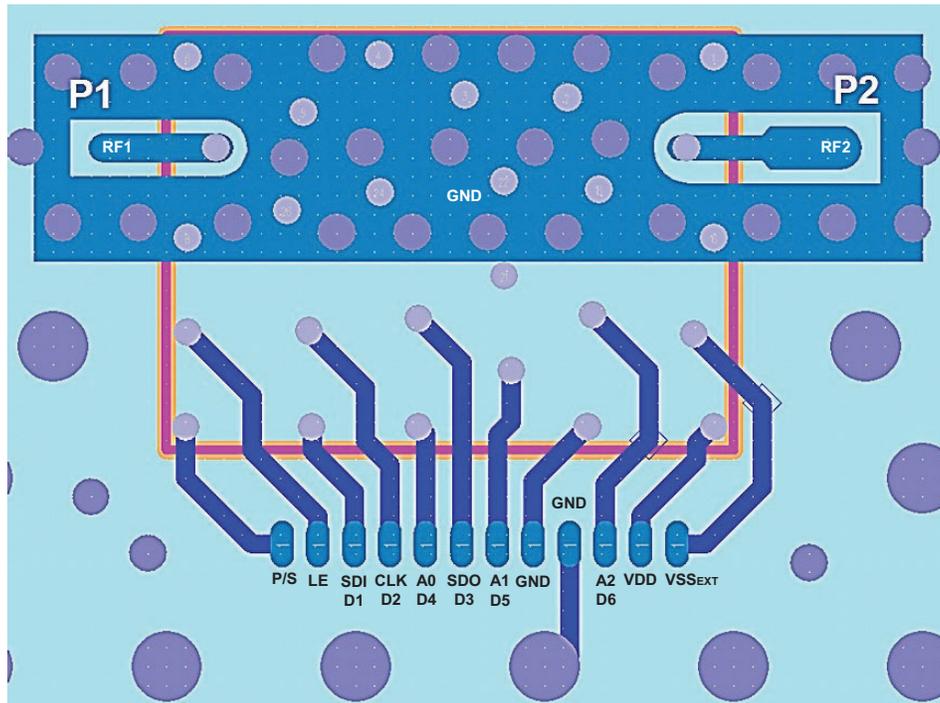

The board layout shown in **Figure 10** has the board stack-up detail as described in **Figure 11**.

Figure 11 ▪ Rogers RO4003C Probe PCB Board Stack-up Detail
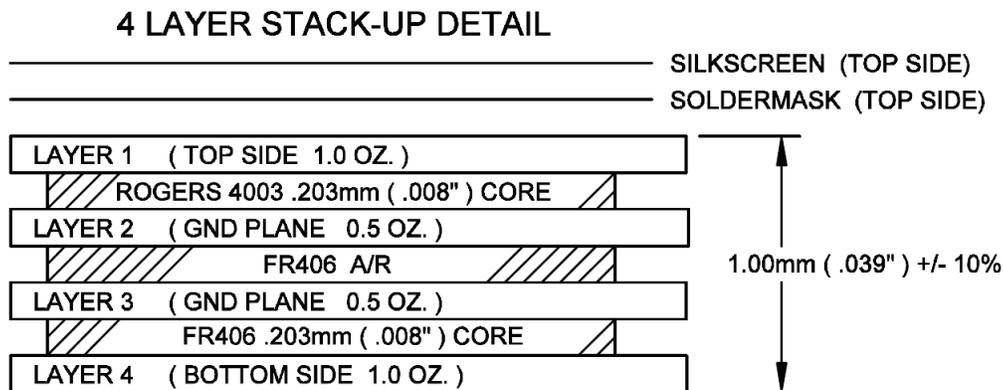
As shown in **Figure 10**, the probe PCB has a unique RF2 port trace designed to aid performance in the high end of the operating frequency range. Dimensional detail of both RF1 and RF2 ports, pins 7 and 17 of the PCB landing pattern, is shown in **Figure 12**.

Figure 12 ▪ Dimensional Detail of the RF Ports Used in the PRT-69885 PCB Landing Pattern
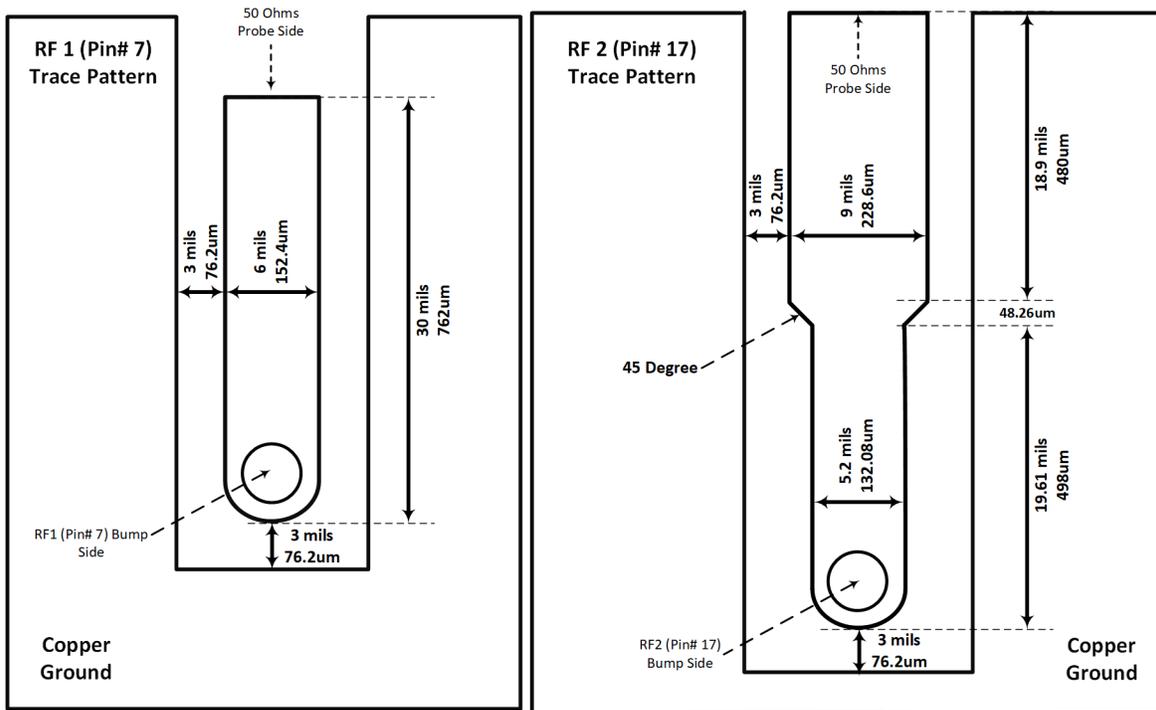
Important dimensions, in addition to the 50Ω transmission line width and spacing, include the dimensions of the thinner lines right at the PE43508 RF ports. As shown in **Figure 12**, the RF1 port (pin 7) uses a CPW trace length of 762 µm (30 mil) with a trace width of 152 µm (6 mil) and signal-to-ground spacing of 76.2 µm (3 mil). This signal trace width and signal-to-ground spacing should approximately give 50Ω for the defined RO4003C stack-up.

The RF2 port transitions from a 50Ω line to a line length, width, and air gap of 480 µm (18.9 mil), 229 µm (9 mil), and 76.2 µm (3 mil), respectively. Then, a second CPW trace length of 498 µm (19.6 mil) with a width of 132 µm (5.2 mil) and an air gap of 124 µm (4.9 mil) connects to the RF2 port of the PE43508. This interconnection scheme improves the high-frequency match of the RF2 port.

Performance Comparison

The three different substrates each have similar yet distinct performance characteristics. **Table 2** and **Figure 13** define the RF1 port maximum return loss for the three substrate options. **Table 3** and **Figure 14** depict the RF2 port maximum return loss. **Table 4** and **Figure 15** show the minimum insertion loss of the three substrate options. Finally, **Figure 16** shows the maximum attenuation behavior of the PE43508 up to 65 GHz. The maximum attenuation is defined as the measured insertion loss at 31.5 dB attenuation setting minus the loss of the reference state at the same frequency.
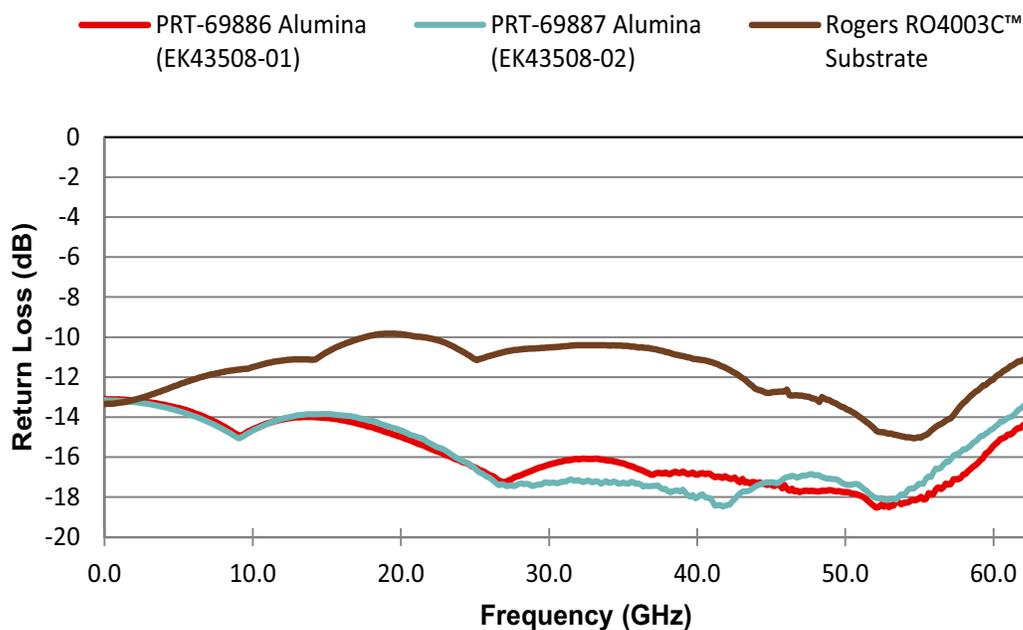
Table 2 ▪ RF1 Maximum Return Loss for the Three Substrate Options

Parameters	Condition	PRT-69886 Alumina (EK43508-01)	PRT-69887 Alumina (EK43508-02)	Rogers RO4003C™ Substrate Probe Data
Port 1 Return Loss (dB)	0.01 – 13.0 GHz	13.1	13.2	11.1
	13.0 – 26.5 GHz	14.0	13.9	10.0
	26.5 – 45.0 GHz	16.1	17.3	10.4
	45.0 – 50.0 GHz	17.4	16.8	13.2
	50.0 – 55.0 GHz	17.7	17.4	13.6
	55.0 – 60.0 GHz	15.4	14.6	12.2
	60.0 – 65.0 GHz	12.0	11.3	10.0

Figure 13 ▪ RF1 Maximum Return Loss vs. Frequency (All States)

Table 3 ▪ RF2 Maximum Return Loss for the Three Substrate Options

Parameters	Condition	PRT-69886 Alumina (EK43508-01)	PRT-69887 Alumina (EK43508-02)	Rogers RO4003C™ SubstrateProbe Data
Port 2 Return Loss (dB)	0.01 – 13.0 GHz	12.3	12.2	12.4
	13.0 – 26.5 GHz	15.0	15.5	14.1
	26.5 – 45.0 GHz	12.3	13.4	11.4
	45.0 – 50.0 GHz	11.8	13.2	12.4
	50.0 – 55.0 GHz	9.8	10.7	12.9
	55.0 – 60.0 GHz	8.6	9.0	11.2
	60.0 – 65.0 GHz	7.7	7.8	11.0

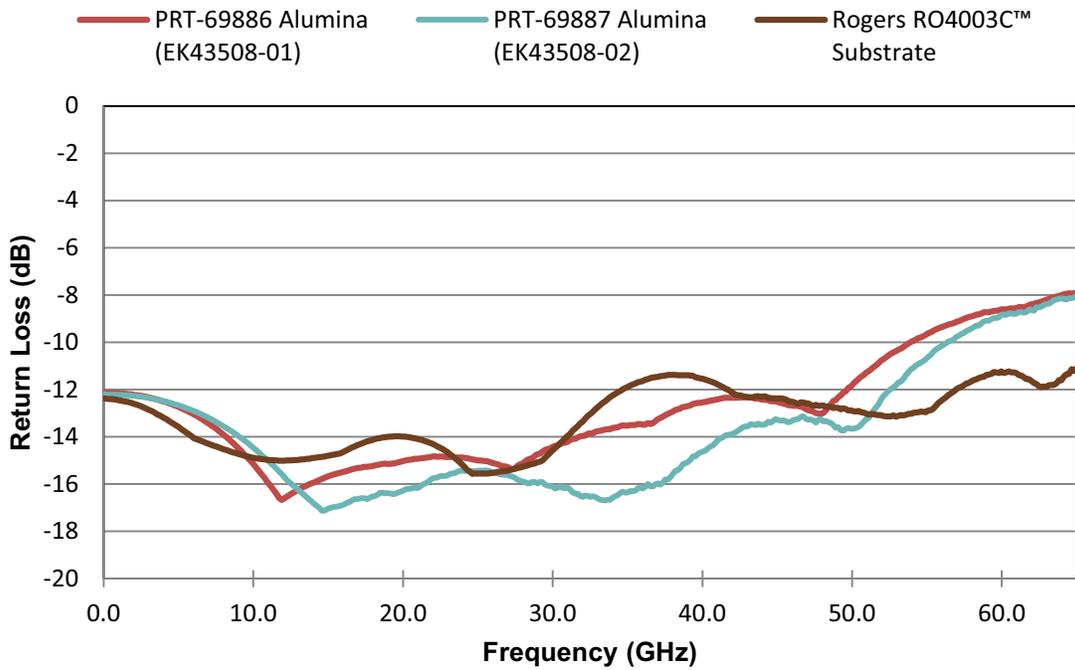*Figure 14 ▪ RF2 Maximum Return Loss vs. Frequency (All States)*

Table 4 ▪ Minimum Insertion Loss for the Three Substrate Options (DSA in 0 dB Attenuation Reference State)

Parameters	Condition	PRT-69886 Alumina (EK43508-01)	PRT-69887 Alumina (EK43508-02)	Rogers RO4003C™ Substrate Probe Data
Minimum Insertion Loss (dB)	0.01 – 13.0 GHz	2.1	2.1	2.1
	13.0 – 26.5 GHz	3.0	3.0	3.5
	26.5 – 45.0 GHz	4.5	4.5	5.1
	45.0 – 50.0 GHz	5.0	4.9	5.3
	50.0 – 55.0 GHz	5.5	5.3	5.7
	55.0 – 60.0 GHz	6.2	6.0	6.2
	60.0 – 65.0 GHz	6.6	6.5	6.8

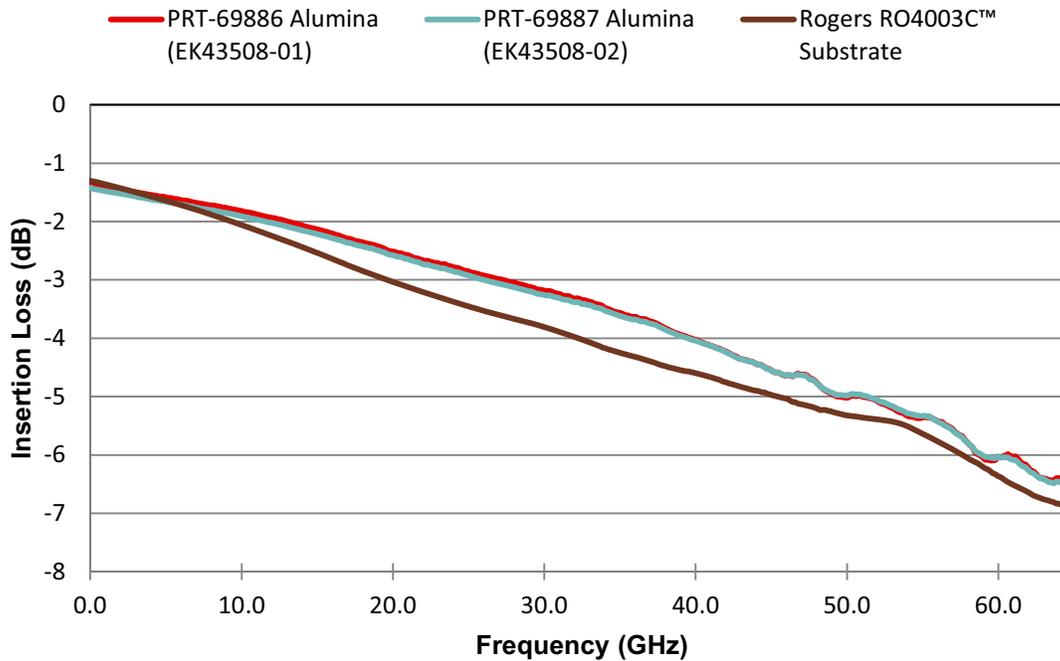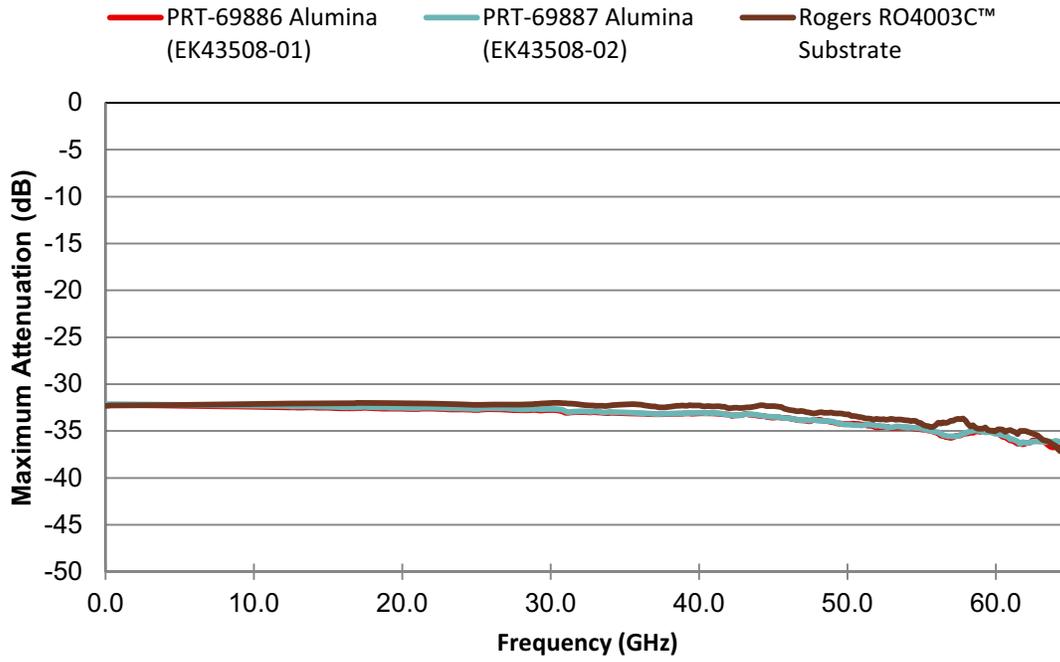Figure 15 ▪ Minimum Insertion Loss vs. Frequency (Reference State)

Figure 16 ▪ Maximum Attenuation(*) vs. Frequency

Note: *   Measured insertion loss at 31.5 dB attenuation setting minus the loss of the reference state at the same frequency.

Assembly Recommendations for Attaching the PE43508 on a PCB

Careful attention must be given to the PCB substrate material, its glassivation temperature (Tg), and the various coefficients of thermal expansion (CTEs) while defining a reliable reflow profile. Excessive soak times and temperatures can each cause significant assembly yield issues and potentially laminate delamination.

Table 5, Table 6, and Table 7 containing assembly-related process parameters are provided to help the user define an assembly flow that works for some specific high-frequency PCB substrates. Specifics concerning other components on the same PCB, the PCB substrate temperature limitations, and the PCB design and its thermal properties, all must be considered in refining a suitable reflow profile and assembly process.

Table 5 ▪ PE43508 Assembly-Related Parameters

Parameter	PE43508	Units	Comments
Max. reflow temp. T_P	≥ 260	°C	JEDEC J-STD-020D.1 Table 4-2
Max dwell at T_P	10	sec	JEDEC J-STD-020D.1 Table 5.2
Recommended flux			
Pb-free solder ball	Tin-95.5/ Ag-3.5/ Cu-1 (%)		SAC 351 Solder Definition
Min. landing size	90	µm	
Solder stop max. thickness	25	µm	
Solder stop diameter	190	µm	
Solder paste particle size	Type 5		15-25 µm particle size
Stencil thickness	60	µm	
Stencil aperture diameter	180	µm	
CTE (worst case X,Y,Z)	6-7	ppm/°C	
Underfill	Not recommended		If deemed necessary, a low-loss, low-dielectric constant underfill can be used.

Table 6 ▪ Assembly-Related Parameters for Common High-Frequency PCB Substrates

Parameter		Panasonic MEGTRON™ 6	Rogers RO4350B™	Rogers RO4003C	Units
Max. reflow temp. T_P		≥ 260	≥ 260	≥ 260	°C
Max dwell at T_P		10	10	10	sec
Glassivation temp. Tg		180-210	> 280	> 280	°C
CTE (w/c X,Y,Z)	X		10	11	ppm/°C
	Y		12	14	
	Z	45	32	46	

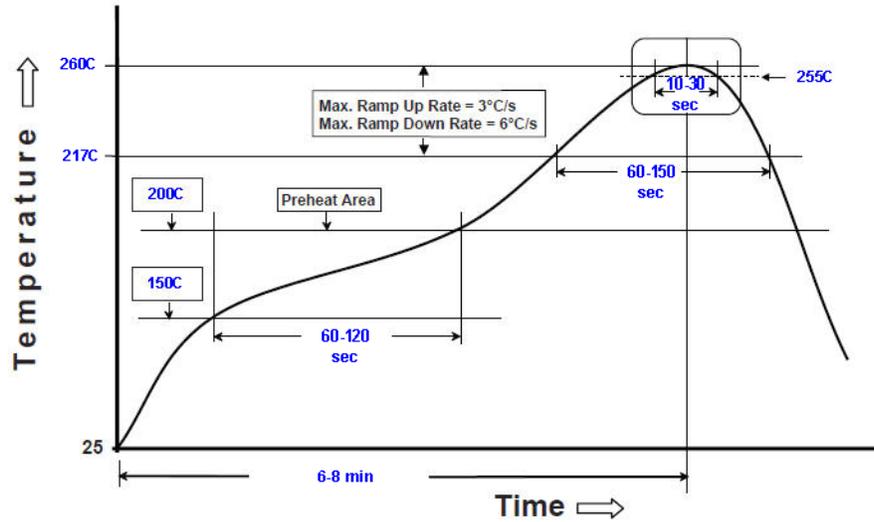*Figure 17 ▪ Suggested Starting Definition for PCB Reflow Profile*

Table 7 ▪ Reflow Profile Parameter Recommendations (source: JEDEC J-STD-020D.01)

Profile Parameter	Pb-Free Assembly	Units	Comments
Preheat temperature	+150–200	°C	
Preheat time	60–120	sec	
Ramp up rate	3	°C/sec	
Liquidous temperature T_L	+217	°C	SAC 351 and Sn/Ag 1.84%
Time above T_L	60–150	sec	
Peak Temperature T_P	+260	°C	
Time within 5°C of T_P	10–30	sec	
Time 25°C to T_P	6–8	min	
Ramp Down Rate	3–6	°C/sec	

The use of underfill may be needed to address the mechanical stresses that arise primarily from differences in the CTEs. The laminate PCB substrates listed have CTEs above 32 ppm/°C, or more than 6x that of the PE43508. Underfill materials will have an impact on the peak RF performance, and therefore, when underfill is deemed necessary, pSemi suggests using a low-loss, low-dielectric constant underfill that is compatible with the entire assembly process.

Conclusion

The PE43508 is the first microwave DSA to be offered by pSemi Corporation. The PE43508 brings competitive minimum insertion loss, 55 GHz monotonicity, and the usual high linearity and power handling pSemi is known for, to a market that can benefit from the uniformity and availability that UltraCMOS affords to every market it enters. To achieve high performance at these frequencies, extreme care must be taken to eliminate any stray parasitics affecting the RF channel.

This application note provides guidance necessary for achieving the optimum performance from the PE43508. Landing patterns in different substrate technologies have been described, all of which have shown comparable performance up to 55 GHz.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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Patent Statement

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