Summary

This application note provides pSemi customers with general guidelines for soldering and assembling wafer-level chip scale packages (WLCSPs) to ensure consistent printed circuit board assembly that meets target yield and reliability. Precise process development and designed experimentation are needed to optimize specific application and performance goals, and to meet the requirements of industry best practices and standards.

Introduction

WLCSP refers to the technology of packaging an integrated circuit at the water level instead of the traditional process of assembling individual units in packages after singulation from a wafer. The device is a solder-bumped array with balls attached at an I/O pitch that is compatible with surface mount assembly processes.

WLCSP technology differs from other ball grid array (BGA) and laminate-based chip scale packages (CSPs) in that no bond wires or interposers are required. The key advantages of WLCSP packaging are that it minimizes die-to-printed circuit board (PCB) inductance, reduces package size, and enables a lighter weight and thinner package profile. WLCSPs are manufactured by extending the wafer fabrication process to form the device interconnects, redistribution layer, and passivation protection. A typical package with RDL is shown in Figure 1.

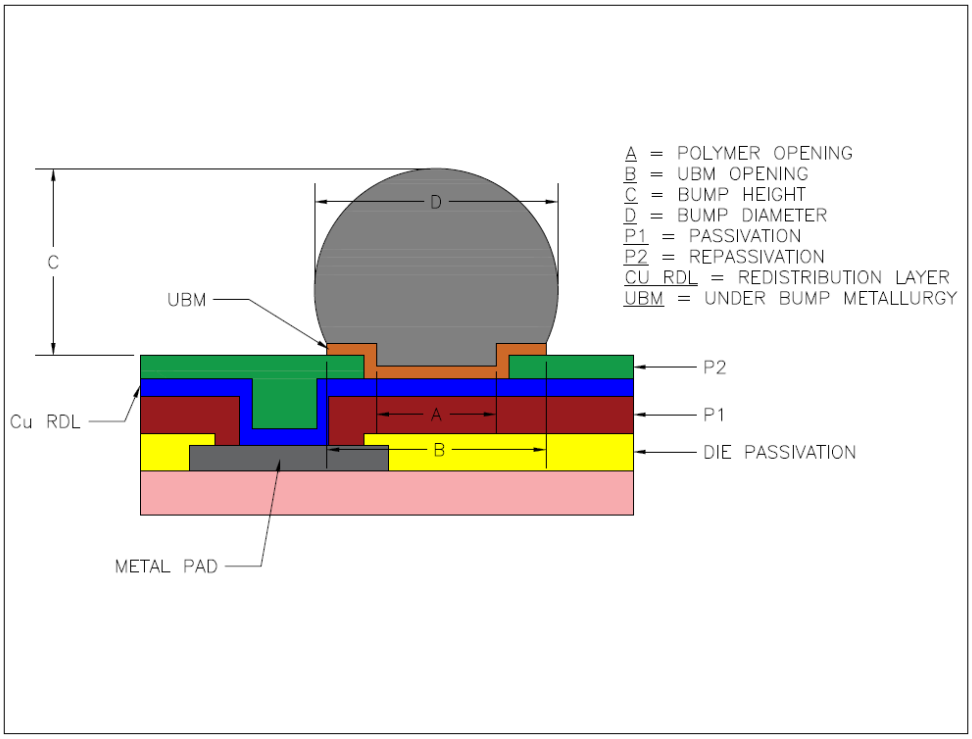

Figure 1. WLCSP with Redistribution Layer (RDL)

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WLCSP Package

WLCSPs are solder bump dies manufactured as an extension of the wafer fabrication process. A typical die has a first layer dielectric, conductive metal redistribution layer (RDL) to redistribute the signal path from the die peripheral to the solder ball pad, and a second dielectric layer to cover the RDL metal, which in turn is patterned into a solder ball array.

Dielectric material is applied over the RDL layer for protection. The solder ball is typically a lead-free alloy placed on an under-bump metallurgy (UBM). After electrical testing, the wafer is thinned and singulated, and the WLCSPs are packaged in tape and reel. pSemi's WLCSPs are of two types: with RDL and without RDL. See *J-STD-012: Implementation of Flip Chip and Chip Scale Technology*[1] and *IPC–7094: Design and Assembly Process Implementation for Flip Chip and Die-Size Components*[2], for industry best practices.

WLCSP Package with RDL

WLCSPs with an RDL layer range from 1.555 mm × 0.855 mm × 0.260 mm to 8.095 mm × 4.095 mm × 0.523 mm. The bump height is 0.198 mm nominal, and the bump diameter is 0.265 mm for 250 µm solder balls. The minimum bump pitch is typically 0.4 mm. See the pSemi product data sheet to verify minimum bump pitch, bump height, and other dimensions.

WLCSP Bump Composition

The solder bump composition of WLCSPs with RDL is SAC405 (Sn 95.5%, Ag 4.0%, Cu 0.5%) for power management products. Alternatively, an alloy composed of Sn 98.2%, Ag 1.2%, Cu 0.5%, and Ni 0.05% can be used for other WLCSPs.

[1] J-STD-012: Implementation of Flip Chip and Chip Scale Technology

[2] IPC-7094: Design and Assembly Process Implementation for Flip Chip and Die-Size Components

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WLCSP Package Cross Section

pSemi WLCPS are categorized as surface mount components (SMCs). Unlike through-hole components, SMCs rely entirely upon the solder interface for mechanical strength. The solder joint properties, design and reflow process are critically important for successful assembly. See *Surface Mount Technology–Principles and Practice*[3] for SMT guidelines. A typical package is shown in Figure 2 and Figure 3. Cross section images of the WLCSP are shown in Figure 4 and Figure 5.

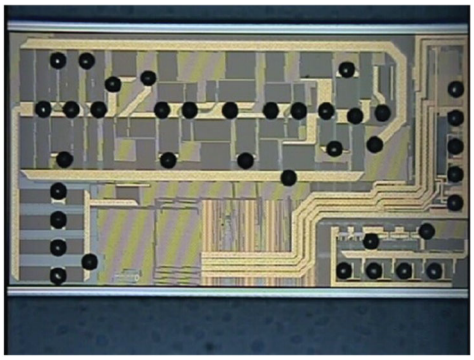

Figure 2. WLCSP Top Side with Solder Bumps

Figure 3. WLCSP Back Side with Opaque Finish

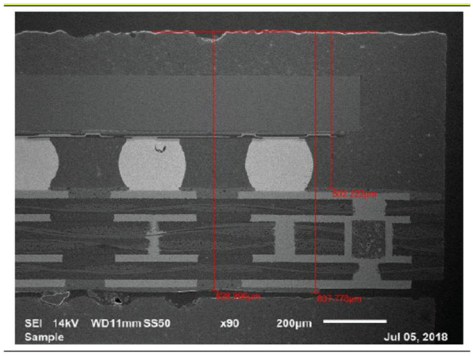

Figure 4. WLCSP Assembly Cross Section

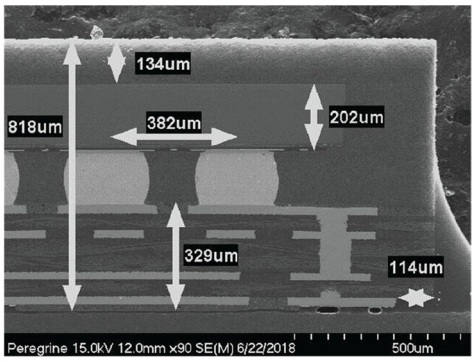

Figure 5. WLCSP Assembly Cross Section with Typical Dimensions

[3] Ray P. Prasad, Surface Mount Technology–Principles and Practice, Van Nostrand Reinhold, New York, 1989, pages 311-328

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WLCSP Process Flow

Figure 6 depicts the WLCSP process flow.

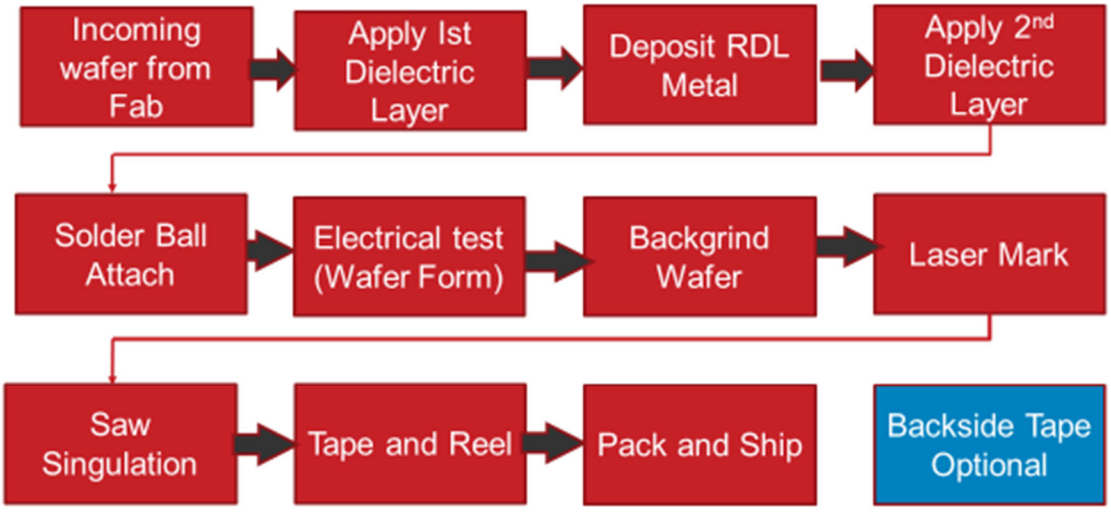

Figure 6. WLCSP Process Flow

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Substrate for Assembly

PC Board Material

WLCSPs are typically soldered to an organic substrate such as PCB. See individual pSemi data sheets for recommended land patterns for the package terminal pads. High-temperature FR-4 or bismaleimide–triazine (BT) laminate with a glass transition temperature (Tg) ≥ 170°C is recommended for lead-free WLCSP assembly. The peak reflow temperatures range from 240°C to 260°C. Follow board design requirements based on *IPC-6012D: Qualification and Performance Specification for Rigid Printed Boards*[4] and *IPC-A-600: Acceptability of Printed Boards*[5]. Table 1 shows commonly used high-frequency substrates and their material properties.

Table 1. High-frequency PCB Substrates

Parameter	Panasonic Megtron 6	Rogers 4350	Rogers 4003	Units
Max Reflow Temp T_P	≥ 260	≥ 260	≥ 260	°C
Glaciation Temp T_g	180-210	> 280	> 280	°C
CTE (w/c X,Y,Z)	45	32	46	ppm/°C

Table 2 shows some commonly used power substrates and their material properties.

Table 2. Power PCB Substrates

Parameter	Isola IS550H	Isola IS580G	Isola 370HR	EM528 (Low CTE)	EM827	Units
Max Reflow Temp T_P	≥ 260	≥ 260	≥ 260	≥ 260	≥ 260	°C
Glaciation Temp T_g	180-210	> 280	> 280	> 280	> 280	°C
CTE (w/c X,Y,Z)- below Tg	13 – 17 38	13 - 14 30	13 – 14 45	9 – 10 25 - 30	12 -15 45	ppm/°C

PC Board Recommended Land Pattern

The printed board land pattern for WLCSP and other die-size array packages is typically a circle of coated copper foil whose diameter is the same or slightly less than the bump or ball contact diameter. Typically, there is a 10% to 20% reduction in size in the land diameter from the bump diameter. Table 3 shows the recommended land pattern for PCB pads. See *IPC–7351C: Surface Mount Design and Land Pattern Standard*[6] for land pattern guidelines based on package dimensions.

Table 3. Recommended PCB Land Pattern

Recommended Land Patterns			
Contact Pitch	Nominal Bump Diameter	Nominal Land Size	Land Size Variations
500	300	250	200–250
400	250	200	170–200
300	200	150	120–150
250	150	125	100–125

[4] IPC-6012D: Qualification and Performance Specification for Rigid Printed Boards

[5] IPC-A-600: Acceptability of Printed Boards

[6] IPC–7351C: Surface Mount Design and Land Pattern Standard

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In general, non-solder mask defined (NSMD) pads are preferred over solder mask defined (SMD) pads for solder bump grid array packages; however, the decision to select NSMD or SMD pads should be based on the complexity of the board design and the board supplier's capability for solder mask registration and tolerance.

Figure 7 shows an NSMD pad, and Figure 8 shows an SMD pad.

Figure 7. Non-solder Mask Defined (NSMD) Pad

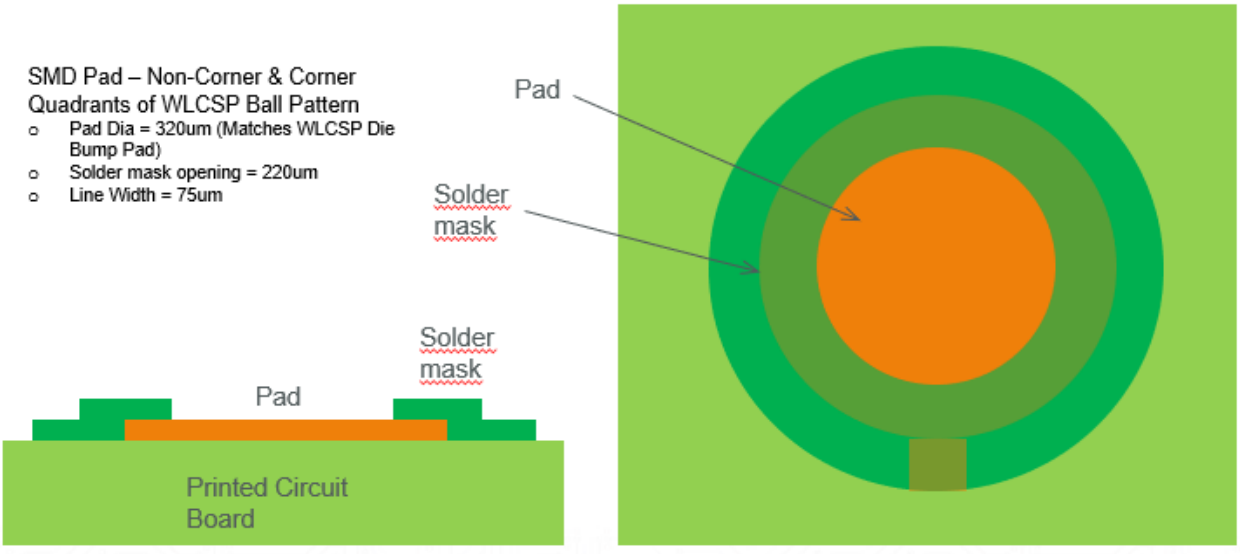

Figure 8. Solder Mask Defined (SMD) Pad

For WLCSP packages with RDL, the corner pads should be NSMD, and the solder mask pull-back from the pads is typically 50 µm. Flooded metal can be broken up with thermal reliefs to maintain an NSMD-defined aspect as shown in Figure 9, Figure 10, Figure 11, and Figure 12.

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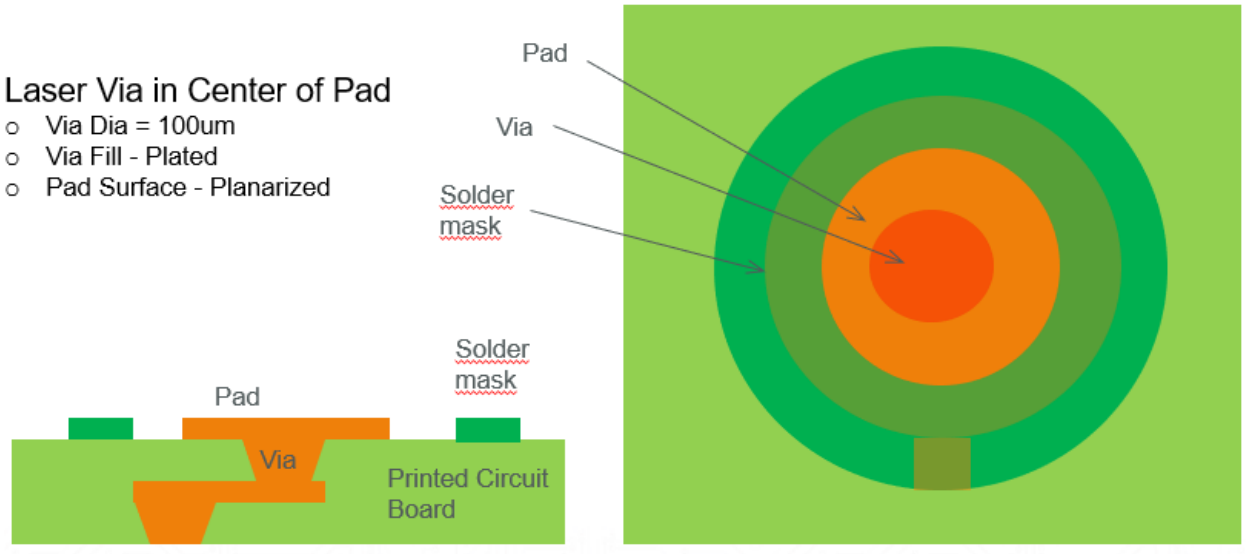
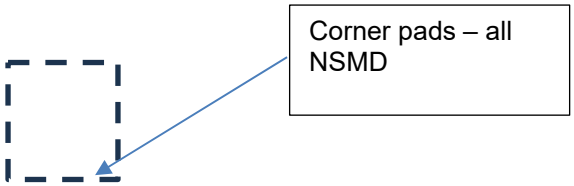


Figure 9. NSMD Pad and Via in Pad

Figure 10. Thermal Relief Pad



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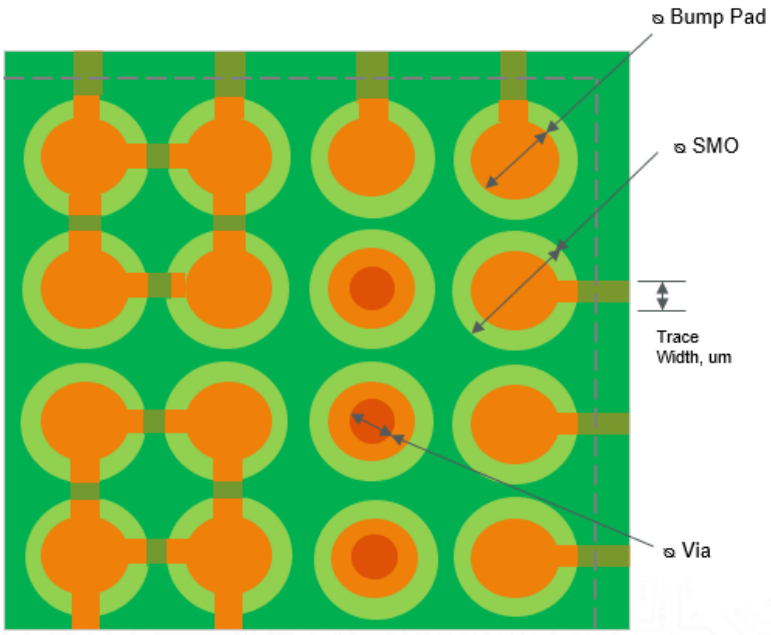

Symbol	Min	Nom
Pitch um		400
⦸ Bump Pad, um	200	220
⦸ Solder Mask Opening – SMO, um		320
⦸ Via in Pad, um	80	100
Trace Width, um		0.075

Figure 11. Corner Pad NSMD

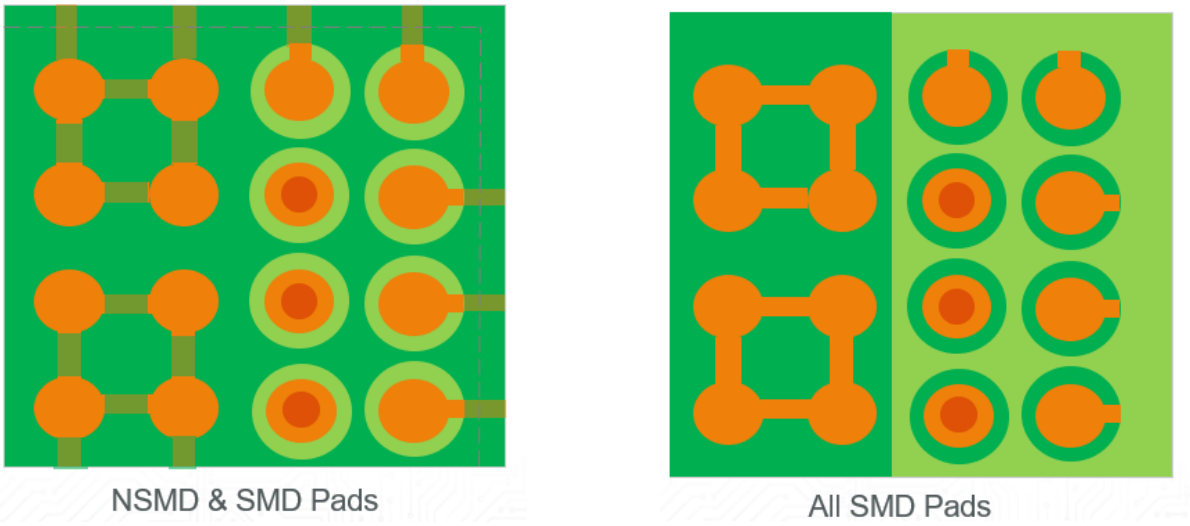

Figure 12. NSMD and SMD, and All SMD Pads

Solder mask is recommended between all pads. The X-section of NSMD pads is illustrated in Figure 13 and the SMD pads are illustrated in Figure 14. If via in pad design is used for the WLCSP package, the via needs to be copper-filled and planarized to create a smooth surface for the ball to bond. pSemi does not recommend using epoxy-filled vias, because they can cause outgassing and solderability issues.

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Figure 13. NSMD Pads (Solder Mask away from Copper)

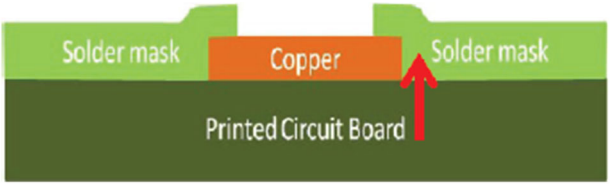

Figure 14. SMD Pads (Solder Mask Encroached on Copper)

Figure 15 and Figure 16 show examples of a WLCSP land pattern.

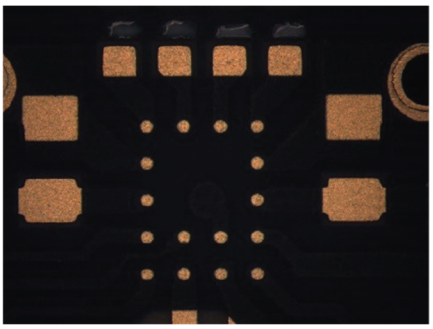

Figure 15. WLCSP Land Pattern

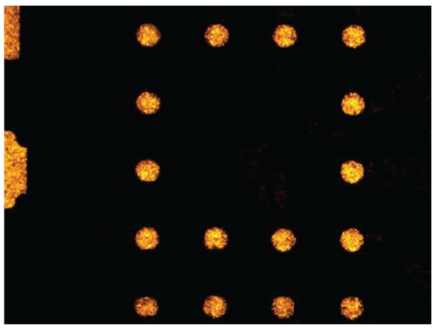

Figure 16. Enlarged Land Pattern

PC Board Surface Finish

Electroless nickel electroless palladium immersion gold (ENEPIG) is the preferred surface finish for the PCB copper land and pads. If you use electroless nickel immersion gold (ENIG) or organic solderability preservative (OSP) coating over copper land pads for cost tradeoffs, carefully evaluate for bump reliability post-reflow prior to manufacturing release. pSemi recommends that the shelf life of the surface finish be monitored to ensure that it has not “expired” to ensure good solderability during assembly. If you use via-in-pad structures, pSemi recommends using copper-filled vias to eliminate voiding of vias due to trapped air. The quality and knowledge of the vendor is critical for via-in-pad designs.

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Solder Stencil/Solder Paste

Stencil Thickness/Opening Recommendation

Solder paste stencil design is critical for correct solder volume and good joint formation, especially as the bump pitch decreases. The stencil thickness and opening determine the amount of solder paste deposited on the PCB land pattern. See *IPC-7525, Stencil Design Guidelines*[7] for guidance on stencil design.

Stencils should be laser-cut stainless steel with nickel plating or electroformed cobalt or chromium-hardened nickel for consistent and repeatable solder paste deposition. pSemi recommends inspecting the stencil openings for burrs, clogs, damage and other quality issues before use.

Both square- and round-shaped apertures have been used successfully; however, square-shaped aperture openings provide more consistent paste release and transfer efficiency compared to round openings. Table 4 summarizes the recommended stencil openings.

Table 4. Recommended Stencil Thickness and Opening

Recommended Stencil Thickness and Openings (mm)		
Description	**WLCSP ≥ 0.4 mm Bump Pitch**	**WLCSP ≥ 0.3 Bump Pitch**
Stencil aperture size	Square	Square
Size	0.25 x 0.25 mm	0.20 x 0.20 mm
Stencil thickness	0.1 mm thick	0.1 mm thick

Solder Paste

Solder paste is a critical material for surface mount assembly. It is a homogenous mixture of metal powder, flux and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct impact on soldering and cleaning, and it is used to pre-condition the surfaces for soldering by removing oxidation and contamination. pSemi recommends Type 4 solder paste (20–38 microns particle size) or finer solder paste and a low-halide content (< 100 ppm halides). No clean flux is recommended to eliminate post-assembly cleaning operations.

WLCSP Board Assembly

WLCSP Placement and Alignment

The WLCSP package pickup and placement requires accuracy, so pSemi recommends using automated fine-pitch pick-and-place tools with vision alignment instead of chip shooters. The board requires local fiducials to support vision alignment. A wide range of choices exist for both low- and high-volume assembly of WLCSP devices. Placement accuracy, repeatability and speed are each critical factors when selecting the system best suited for a specific application. The specific process can influence placement requirements and affect cost and throughput.

Proper pick-and-place nozzle design is critical for damage-free picking from tape and reel. Characterize die placement pressure, and measure actual placement forces periodically using a calibrated load cell with meter. Stationary tape and reel feeder bases are also required for all pick-and-place systems.

[7] IPC-7525: Stencil Design Guidelines

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The placement accuracy of the automated pick-and-place system depends on its vision alignment of package outline centering vs. bump grid array centering. Employ package outline centering for higher speed placement with reduced alignment accuracy requirements or employ bump grid array vision centering for maximum alignment accuracy at lower placement rates. Typical placement tolerance guidelines for WLCSPs are = 10 µm at 4s.

2D transmission X-ray inspection is required for placement accuracy verification and measurement. See *IPC 7094, Design and Assembly Process Implementation for Flip Chip and Die Size Package Component Mounting*[2].

WLCSP Flux Dip

The WLCSP placement step involves the application of flux to the solder bumps either using a spray fluxing arrangement for the substrate or a flux dip station on the pick-and-place machine. Carefully selecting the low-residue flux with adequate tackiness is essential to properly cover the bump with flux.

When performing flux dip, wet at least 1/3 of the total bump height with flux. You can also employ an alternative method using no-flow or flux underfill for assembly, because this flux or underfill material cures during the reflow step and saves an additional process step of underfill dispense and cure. pSemi recommends carefully evaluating this process to ensure there are no flux-to-underfill interactions impacting the assembly.

WLCSP Clearance/Location on PCB

For a typical board assembly, consider the clearance around the maximum size of the component. This clearance is to accommodate for the pick-and-place accuracy of the WLCSP component and the neighboring components. When underfill application is required, make room for dispensing. As with other SMT components, pSemi does not recommend placing WLCSP products near mounting holes, connectors, clamps etc. due to the increased amount of bending stress on the bumps. When using multi-up boards in a large panel, WLCSPs mounted near the separation edge can be damaged during de-paneling, so avoid such edge locations for WLCSPs.

WLCSP Assembly Process Flow

The typical process flow for WLCSP assembly is shown in Figure 17.

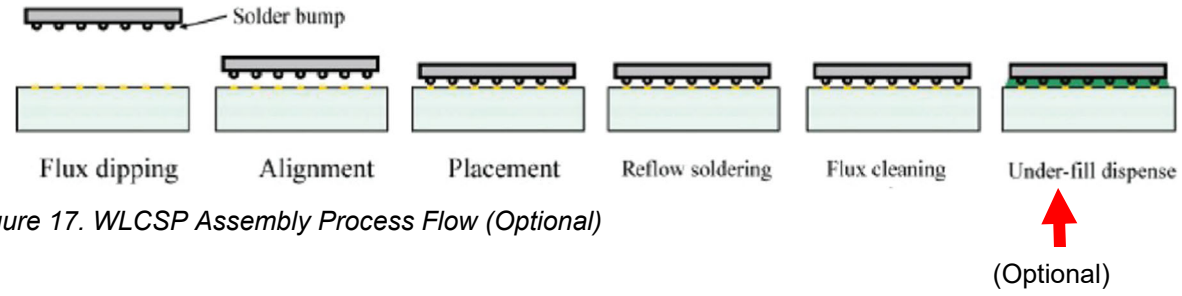

Figure 17. WLCSP Assembly Process Flow (Optional)

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Reflow Specifications

The reflow profile is a critical part of the PCB assembly process. A proper reflow profile must provide adequate time for flux activation and volatilization, proper peak temperature, time above liquidus, and ramp-up and cool-down rates. The profile used has direct bearing on manufacturing yields, solder joint integrity, and the reliability of the assembly. During mass soldering, all solder joints must reach the minimum soldering (reflow) temperature to assure metallurgical bonding of the solder alloy and the base metals to be soldered.

Metallurgical bonding requires that both surfaces to be soldered, and the solder, reach this minimum soldering temperature for a sufficient time to allow the wetting of the solder surfaces. For reflow profile guidelines, see *IPC-7530: Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave)*[8].

Specific production reflow ovens and rework systems vary depending on manufacturer and model. Therefore, a system-specific profile must be established using a profiler and thermocouples at the actual solder joint locations or top of the WLCSP. pSemi recommends using forced-gas convection reflow ovens to maintain controlled heat transfer rates throughout the process. Using nitrogen during reflow is optional. If you use nitrogen, follow the oven manufacturer's guidelines to maintain oxygen content below a certain PPM (typically < 100 PPM). Proper board support during reflow is essential to avoid board sagging, which can result in stress to the solder joints.

A typical reflow profile is made up of four distinct zones: the preheat zone, the soak zone /flux activation zone, the reflow zone and the cooling zone. For moisture-sensitive parts, follow the reflow guidelines in *IPC/JEDEC-J-STD-020E: Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*[9].

Preheat Zone

In the pre-heat zone, the typical heating rate is 2°C to 4°C/second, and the peak temperature is 100°C to 125°C. If the temperature ramp is too fast, the solder paste may splatter and form solder balls. Also, control the maximum heating rate to avoid thermal shock to sensitive components.

Soak Zone

The soak zone is intended to allow the board and components to reach uniform temperature, minimizing thermal gradients. The soak zone also activates the flux within the solder paste. The ramp rate in this zone is very low, and the temperature is raised near to the melting point of the solder (183°C for standard 63Sn/37Pb solder and 217°C for SAC305/SAC405 solder). If very high temperatures are used in the soak zone, the flux evaporates very quickly, resulting in solder balls. If the ramp rate is too slow, the solder paste oxidizes excessively, resulting in solder splatter. Typical soak times are usually around the range of 130°C to 170°C for 60 to 90 seconds. For power products with heavier copper plane boards and higher thermal mass, a longer soak is recommended to allow board and components to come into equilibrium before the solder melts.

Reflow Zone

In this zone, the temperature is kept above the melting point of the solder for 30 to 60 seconds. The peak temperature in the zone should be high enough for adequate flux activity and to obtain good wetting. For lead-free solders SAC 305/405, this range goes up to 250°C–260°C.

The temperature, however, should not be so high as to cause component damage, board damage, discoloration or charring of the board. Extended duration above the solder melt temperature will damage temperature-sensitive components and possibly create extensive intermetallic growth between the solder and the pad metallization, making the solder joint brittle and reducing solder joint fatigue resistance.

[8] IPC-7530: Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave)

[9] IPC/JEDEC-J-STD-020E: Moisture /Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices

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Additionally, high temperature can promote oxide growth depending upon the oven atmosphere, which can degrade solder wetting. pSemi recommends, but does not require, nitrogen reflow. Monitor the board and component temperature during reflow to ensure sufficient heat flow is present to form the joint. This can be achieved by attaching thermocouples at the top of the WLCSP and the board surface and using the profiler to monitor temperatures and ramp rates. Develop a reflow profile for each assembly and conduct a first article inspection on the solder joints prior to committing the entire lot to assembly. See *IPC-A-610F: Acceptability of Electronic Assemblies*[10] for solder joint inspection. For inspection of voids, shorts, and insufficient solder, transmissive X-ray is typically used.

Cooling Zone

The cooling rate of the solder joint after reflowing is also important. For a given solder system, the cooling rate is directly associated with the resulting microstructure which in turn affects the mechanical behavior of the solder joints. The faster the cooling rate, the smaller the grain size of the solder joint, and so the higher the fatigue resistance of the solder joint. Conversely, rapid cooling results in residual stress between coefficient of thermal expansion (CTE) mismatched components; therefore, the cooling rate must be optimized.

Reflow Profile Example

Figure 18 shows an example of a WLCSP reflow profile with lead-free solder bumps.

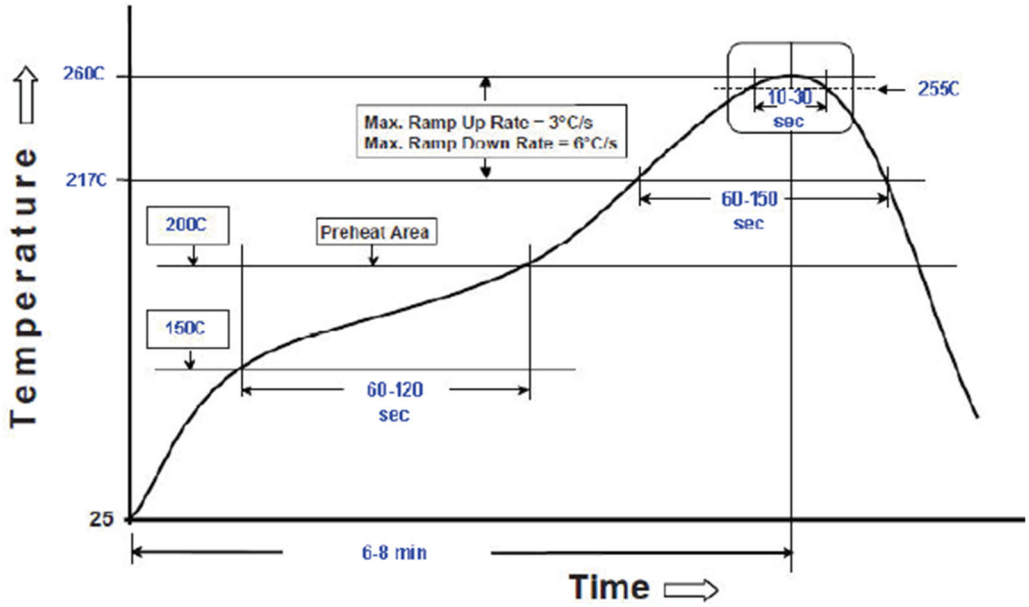

Figure 18. Example of WLCSP Reflow Profile with Lead-free Solder Bumps

[10] IPC-A-610F: Acceptability of Electronic Assemblies

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Table 5 shows the general reflow profile parameter recommendations based on J-STD-020E[9]. Consider the PCB board design and its thermal properties in refining a suitable reflow profile and assembly process.

Table 5. Reflow Profile Parameter Recommendations (Source: JEDEC J-STD-020E)

Profile Parameter	Pb-Free Assembly	Units	Comments
Preheat Temperature	150-200	°C	
Preheat Time	60-120	sec	
Ramp Up Rate	3	°C/sec	
Liquidus Temp T_L	217	°C	SAC 405 and SAC-N
Time above T_L	60-150	sec	
Peak Temperature T_P	260	°C	
Time within 5°C of T_P	10-30	sec	
Time 25°C to T_P	6-8	min	
Ramp Down Rate	3-6	°C/sec	

Post Reflow Inspection

pSemi recommends conducting visual and 2D X-ray inspection after solder reflow for solder joint size and shape irregularities. Well-reflowed solder joints show evidence of good wetting of copper pads with uniform solder surface appearance. Inspect flip-chip solder joints for uniform ball collapse after reflowing. Visual inspection and X-ray can also support inspection of solder shorts, insufficient solder, voids within solder joint and potential solder opens. Sample tilt capability in X-ray may be required to look for solder opens. Use *IPC-A-610F*[10] solder joint acceptance criteria for inspection.

Figure 19 and Figure 20 show an example of a soldered WLCSP. For solder joint acceptance criteria, see *IPC A-610F*[10].

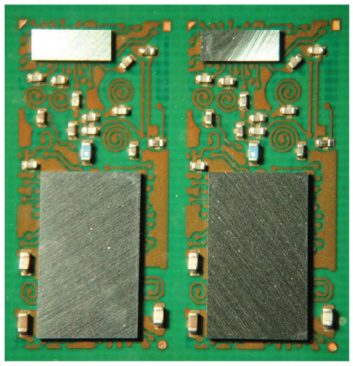

Figure 19. WLCSP Top View

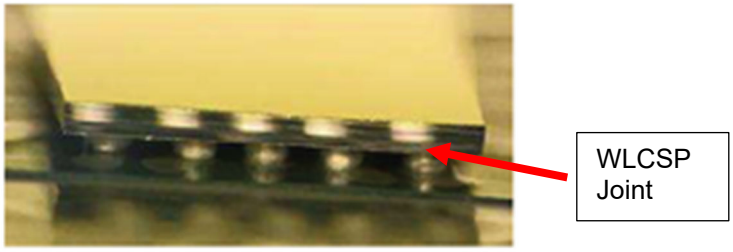

Figure 20. WLCSP Post Reflow

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X-ray inspection to check for uniform bump collapse is essential for process controls. Figure 21 shows the top view of WLCSP X-ray post reflow.

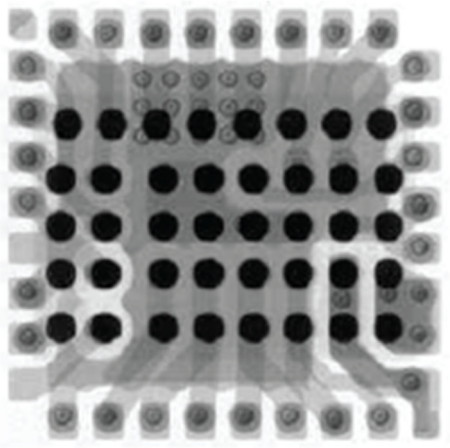

Figure 21. WLCSP X-ray Top View, Post-reflow

Do cross sectional analysis to see proper bump collapse, intermetallic formation, and PC board layers and vias.

Figure 22 illustrates the cross-section of the WLCSP package post-assembly.

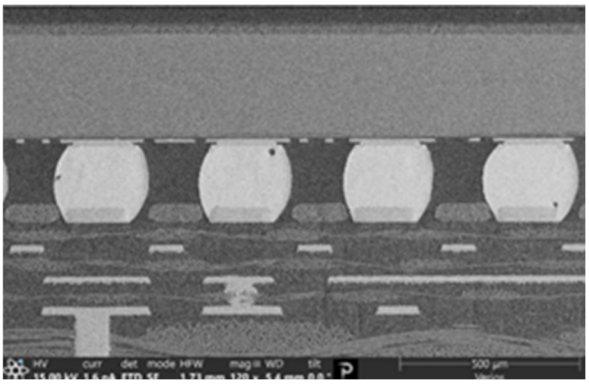

Figure 22. Cross Section, WLCSP Bump Reflow

PCB Cleaning

If you use a low-residue, no-clean solder paste, PCB cleaning is typically not required. No clean fluxes and solders have been formulated to minimize the harmful effects that residues left on the board may cause in the form of corrosion. A wide variety of no-clean solder pastes are available in the market. pSemi recommends you perform application-specific evaluations to identify if any remaining residues can cause harm to the assembly. Contact your solder paste supplier for testing performed and recommended use conditions. Evaluate the cleaning process for water-soluble fluxes , giving special attention to cleaning under low-standoff quad-flat no-leads/surface mount technology (QFN/SMT) components; pSemi recommends you discuss cleaning material interactions with your supplier before cleaning. In addition to cleaning, consider drying PC boards of any residual cleaning medium, such as saponifier, to prevent potential issues such as corrosion.

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Underfill Application

Using underfill improves board-level reliability behavior; however, it might affect the product's electrical performance. pSemi advises you to carefully assess underfill materials. The type of underfill material to use depends on the application. For high-frequency applications, using underfill may make it challenging to maintain peak RF performance. Yet, in some instances, underfill may be needed to address the mechanical stresses that arise primarily from differences in the CTE. The laminate PCB substrates have CTEs above 32 ppm/°C, or more than four times that of the WLCSP die, which is around 4-6 ppm/°C, so these materials may require underfill. In such cases, pSemi suggests using a low-loss, low-dielectric underfill that is compatible with the entire assembly process. Figure 23 illustrates an underfilled WLCSP with a visible underfill fillet on all four sides. Figure 24 illustrates the underfill flow between the solder bumps with uniform, void-free fill.

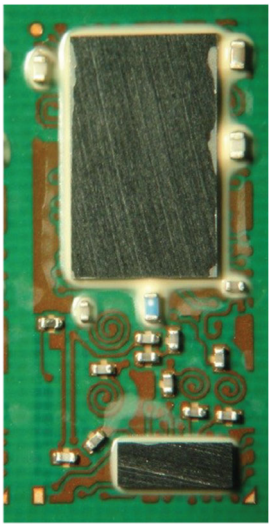

Figure 23. WLCSP Underfill and Cure

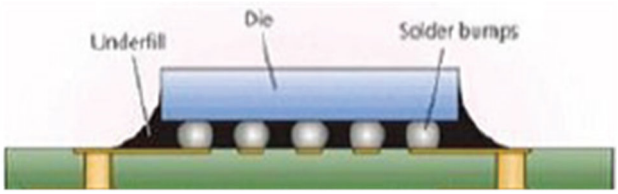

Figure 24. Underfilled Unit

Figure 25 shows the insertion loss of SPDT with and without underfill.

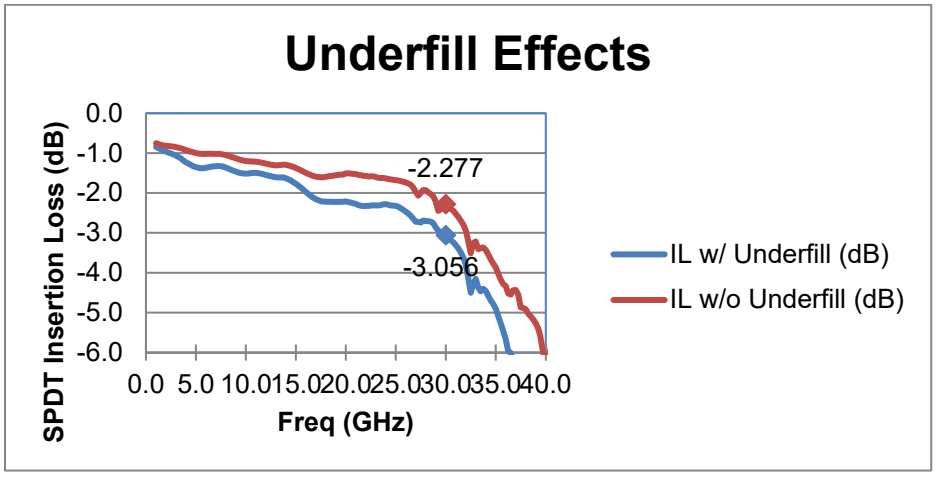

Figure 25. Insertion Loss of Single Pole Double Throw (SPDT) with and without Underfill

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Underfill Materials and Process Flow

The underfill absorbs the stresses of the CTE mismatches between the WLCSP and the board substrate and reduces the stress on the soldered bumps. See *J-STD-030A: Selection and Application of Board Level Underfill Materials*[11].

The following material property should be considered for underfill selection:

- Cured epoxy CTE should match solder joint interconnects (21ppm/°C). Material should have 65% to 70% silica filler to lower CTE.
- High glass transition (Tg) to achieve all product storage life temperature requirements
- Minimum cured epoxy Tg >substrate Tg. BT/ Enhanced FR4 = 170°C to 185°C)
- High adhesion properties to die passivation and to solder mask
- Low ionic < 100 ppm total halides
- Low viscosity and fast flow rate with flow capability to fill minimum 1–2 mil gap size
- Low warpage and low shrinkage matrix
- Minimal moisture absorption
- Evaluate voiding behavior and potential impact on biased humidity reliability performance.
- Underfill thawing curves, storage, shelf life, pot life and use conditions as defined by supplier should be followed.
- Controlled storage and thawing conditions should be followed to avoid moisture absorption in epoxy.

Underfill Dispense and Cure

In high-volume manufacturing, underfill is typically dispensed with auto-dispense tools using a syringe.

Before dispensing, thaw the underfill and bring it to room temperature according to the manufacturer's directions.

Each day or at the start of each shift, calibrate the dispense volume to ensure the consistency of volume dispense. Maintain logs to define syringe change frequency based on the number of drops dispensed, flip-chip size, etc. Conduct visual inspection to ensure that underfill is dispensing consistently and indexing to the correct location on the board.

Develop an oven cure profile for the underfill based on the manufacturer's directions.

Visual Inspection Acceptance Criteria

Underfill epoxy after curing must achieve a continuous positive fillet around the entire perimeter of the die with minimal voids. A positive fillet is defined as having a minimum contact height to the bottom side edge of the die and maximum contact height not to exceed the top side edge of the die. In addition, the fillet must demonstrate a positive wetting angle away from the outside edge to the substrate surface.

The visible epoxy surface area should be uniform and free of voids and pinholes.

Epoxy shall not adjoin any assembly required electrical contact surfaces, such as traces, pads, test points, etc.

Underfill material should not flow on top of the die.

Absence of underfill material between two bumps is not acceptable.

Underfill delamination from die or substrate side is not acceptable.

Scanning acoustic microscopy (C-SAM) can be used as an analytical technique for void detection in underfill.

[11] J-STD-030A: Selection and Application of Board Level Underfill Materials

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Table 6 summarizes the key recommendations for a robust underfill process

Table 6. Summary of Recommendations for Underfill Application

Recommendations	Reasons
High Tg- glass transition underfill material	Compatible with lead free reflow and storage life
Underfill CTE match with solder alloy	Minimize cracking post reflow
Controlled storage and thawing of underfill	Maintain material integrity and yields
Low ionic	Prevent corrosion/migration
Dispense volume calibration	Consistency of visible underfill fillet
Continuous fillet after cure on all sides	Long term reliability
Minimize voids and pin holes	Prevent stress to solder joints.

Rework

Reworking WLCSPs can be challenging and requires proper optimization of the placement and reflow processes. pSemi does not recommend using a soldering iron to perform hand rework. Perform component removal and replacement using a tool with a hot air nozzle and the ability to conduct board preheat. Use proper process controls and shielding to minimize impact to “near neighbor components” on the board and prevent their reflow.

The rework process consists of the following basic elements:

- Pre-heat the PCB
- Reflow component solder
- Vacuum removal of component
- Clean and prepare PCB lands (site redressing)
- Screen print paste on lands
- Place and reflow new component
- Inspect solder joints

PC Board Preheat

Board pre-heat is required for lead-free rework to ensure that the board is heated properly prior to solder melt. Removing a component by topside heat only can result in lifted lands. Pre-heat the board at a temperature of 90°C to 125°C. Pre-heating ensures that the board is in equilibrium before the solder melts. Bake PCBs for moisture removal using the time and temperatures recommended by the PCB board supplier. This bake operation should be conducted before pre-heating the board, and pSemi recommends doing this to prevent delamination and damage to other components. See *IPC-7711/21B: Rework, Modification and Repair of Electronic Assemblies*[12].

Reflow/Removal of the Component from PCB

pSemi recommends using a hot gas nozzle for localized component rework to minimize impact to “near neighbor components” on the board. These nozzles incorporate a hot gas shroud that heats the part to a temperature required for reflowing the solder interconnects. Once the solder reflows, the nozzle vacuum cup automatically lifts the unit from the PCB. Optimize the nozzle size and heat flow to keep the heat flow localized. Parts must not exceed the peak temperature listed on the moisture sensitivity level (MSL) label for the package. pSemi does not recommend reusing the part after it is removed.

Site Redressing of the PCB Land

After removing the component, clean the PCB and prepare it using conventional tools and cleaning processes used for SMT packages. To avoid damaging the board pads or solder mask, perform the site redress process with

[12] IPC-7711/21B: Rework, Modification and Repair of Electronic Assemblies

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caution. Apply flux to the site after component removal. Residual solder remaining on the board pad can typically be removed using a "solder wick" soaked in flux. Using a temperature-controlled soldering iron fitted with a flat blade, gently place the solder wick on the PCB lands to facilitate removal of solder residues. Remove residual flux from the site with alcohol and a lint-free swab. Then, inspect the site before the component replacement process.

Screen Printing of Solder Paste/Flux

Due to the tight geometries used on today's PCBs, it is difficult to screen print paste on the assembled board; as a result, the approach of screen printing the paste directly on the new component using a mini stencil has been adopted. pSemi recommends using a Type 3 or 4 no-clean solder paste. Alternately, use flux to avoid bridging issues.

Placement and Reflow of the Component

Place the SMT component using an optical split prism system combined with a microscope. The image of the screen-printed component and the PCB land pattern are superimposed during the placement and alignment operation. Once the package is correctly aligned, lock the X-Y table to prevent further movement. Reflow the new component with localized hot air reflow. Once the cool-down stage is complete, raise the nozzle and remove the assembly for inspection. The rework profile should have ramp rates and peak temperatures like the initial reflow and follow the guidelines of component handling specified in *J-STD-033D: Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices*[13].

Pack and Ship

WLCSPs are typically packed and shipped in tape and reel, although low-volume or sample parts could be shipped in waffle packs. See the pSemi data sheet for the tape and reel dimensions.

Moisture Sensitivity Level

The MSL rating for pSemi WLCSP is MSL Class 1 per *JEDEC STD-020E*[9] classification. The MSL1 class does not require dry packing using moisture barrier bag during shipment.

Storage and Shelf Life

The label on the packing bag specifies the shelf life and floor life expiration date. Solderability should be checked. See *J-STD-002E: Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires*[14].

[13] J-STD-033D Handling, Packing, Shipping and Use of Moisture/Reflow and Process Sensitive Devices

[14] J-STD-002E: Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

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14. J-STD-002E: Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

Sales Contact

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