PE23108

Document Category: Product Specification

High-Efficiency LED Backlight Driver

General Description

The PE23108 is an ultra-high efficiency DC-DC converter solution with integrated programmable current sinks that drive up to eight strings of LEDs. The PE23108 integrates all MOSFETs and their control and driver circuitry. With its proprietary architecture, the PE23108 provides the highest efficiency—up to 96%—possible in a compact 3.445 mm x 2.095 mm WLCSP 30-pin package. The unique two-stage architecture enables a small and low-profile solution size aligned to the needs of the latest mobile products.

Features

- Synchronous DC-DC converter with integrated FETs
- 2- and 3-cell Li-ion battery input voltage for LED boost: 4.5V to 15V
- 2.7V to 5.5V IC input voltage
- Proprietary architecture for ultra-high LED efficiency, up to 96%
- Integrated output disconnect switch
- Up to 42V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- Up to 12-bit dimming resolution with an additional 3-bit dithering
- Linear/logarithmic analog and PWM dimming for maximum flexibility and resolution
- Phase-shifted PWM dimming among active strings to minimize audible noise
- LED brightness ramp up/down control with programmable ramp rate and linear/ logarithmic ramp profiles
- 1 MHz I^2C 6.0-compatible serial interface to program the brightness
- Extensive programming capability with non-volatile memory for storing user register settings
- Eight independently enabled current sinks, up to 33 mA per current sink
- External PWM input for fine dimming resolution
- 0.5% current matching at 20 mA per current sink
- Wide range of input and output voltages with 2x charge pump ratio
- Selectable boost switching frequency from 179 kHz to 1.43 MHz
- Extensive fault protection, including boost over-current protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Applications

Typical applications for 2- and 3-cell platforms include the following:

- 8”-17” FHD/UHD + LCD backlight panels
- Ultrabooks, ultraportables, and notebooks
- 2-in-1, convertible, and detachable notebooks
- Full-size tablet computers
- LCD panels
- Ultra-thin form factor mobile platforms

Efficiency

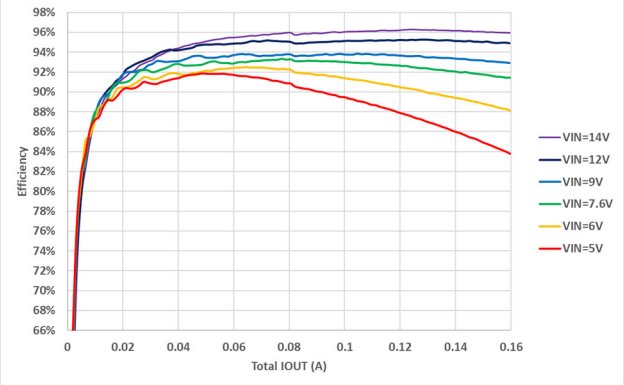

Figure 1. Typical Boost Efficiency – 8p12s, 20 mA, 715 kHz

Application

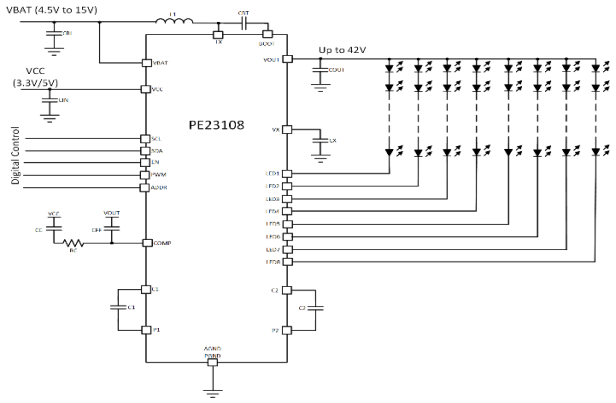

Figure 2. Typical Application Circuit

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Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1.

Table 1. PE23108 Absolute Maximum Ratings

Parameter	Min	Max(1)	Unit
VBAT to AGND	-0.3	18	V
VCC, PWM, COMP, EN, SCL, SDA, ADDR to AGND	-0.3	6	V
VOUT, C1, C2 to AGND	-0.3	45	V
LEDx to AGND	-0.3	40	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1, P2, to PGND	-0.3	22	V
VX to LX, P1, P2	-0.3	22	V
BOOT to VBAT	-18.3	28	V
BOOT to LX	-0.3	6	V
C1, C2 to VX	-0.3	22	V
Storage temperature	-65	150	°C
Junction temperature (J_T)	–	150	°C
Bump or lead temperature (soldering and reflow)	–	260	°C
ESD tolerance, HBM(2)	–	1000	V
ESD tolerance, CDM(3)	–	1000	V

Notes:

1. These “Absolute Maximum Ratings” are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.
2. Human body model, per JEDEC standard JS-001-2017.
3. Field-induced charge device model, per JEDEC standard JESD22-C101.

Recommended Operating Conditions

Table 2 lists the PE23108 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE23108 Recommended Operating Conditions

Parameter	Min	Max	Unit
VBAT Input Voltage Range, relative to AGND or PGND(*)	4.5	15	V
VCC Voltage Range, relative to AGND	2.7	5.5	V
VOUT Output Voltage Range, relative to AGND PGND(*)	18	42	V
VX Boost Output Voltage Range, relative to AGND or PGND	1.2*VBAT	21	V
Junction temperature range (J_T)	-40	+125	°C

Note: * VBAT and VOUT ranges must meet the valid operating regions in continuous conduction mode (CCM): $(VBAT \leq \frac{VOUT}{2.15})$

Package Thermal Characteristics

Table 3 lists the package thermal characteristics.

Table 3. Package Thermal Characteristics(1)(2)

Parameter	Max	Unit
Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	46	°C/W
Junction-to-board thermal characterization (Ψ_{JB})	11	°C/W
Junction-to-top case thermal characterization (Ψ_{JC})	8	°C/W

Notes:

1. Package thermal characteristics and performance are measured and reported in a manner consistent with JEDEC standards JESD51-8 and JESD51-12.
2. Junction-to-ambient thermal resistance (Θ_{JA}) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight/routes, and air flow. To realize the expected thermal performance, pay close attention to the board layout.

Electrical Specifications

Table 4 lists the PE23108 key electrical specifications at the following conditions, unless otherwise noted. Typical values are at $T_A = T_J = 25$ °C with 8p12s.

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, $T_A = T_J$ = -40 °C to +85 °C

Table 4. PE23108 Electrical Specifications

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input supply							
IC input voltage range	V_{VCC}	–		2.7	–	5.5	V
Input voltage range	V_{VBAT}	–		4.5		15	V
VCC under-voltage lockout (UVLO) threshold high	$V_{VCC\_UVLO\_H}$	V_{VCC} rising		–	–	2.6	V
VBAT under-voltage lockout (UVLO) threshold high	$V_{VBAT\_UVLO\_H}$	V_{VBAT} rising		–	–	4.4	V
Under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}	VBAT		–	65	–	mV
		VCC		–	50	–	
VCC shutdown supply current	I_{VCC_SD}	IVCC with VEN = 0V		–	–	1	µA
VBAT shutdown supply current	I_{VBAT_SD}	IVBAT with VEN = 0V		–	–	1	µA
VCC quiescent current	I_{VCC}	EN = 1.8V, ILED = 100 µA, f_{SW_BOOST} = 715 kHz		–	2	–	mA
Thermal shutdown threshold(3)	T_{TSD}	–		–	150	–	°C
Thermal shutdown hysteresis(3)	T_{TSD_HYST}	–		–	20	–	°C
Soft start timeout duration	–	–		–	10	–	ms
Step-up converter							
Output voltage range(4)	V_{OUT}	–		18	–	42	V
Maximum output power	–	–		6	–	–	Watts
Boost switching frequency range	f_{SW_BOOST}	FSW_BOOST [3:0]	0100	–	715	–	kHz
			1010	–	286	–	
Boost switching frequency accuracy	–	f_{SW_BOOST} = 715 kHz		-4	–	+4	%
Boost minimum off-time	$T_{OFF\_BOOST\_MIN}$	–		–	170	–	ns
Boost minimum on-time	$T_{ON\_BOOST\_MIN}$	–		–	60	–	ns
Boost low-side switch current limit, cycle-by-cycle	I_{BOOST_LIMIT}	I_{LX} rising	BOOST_ILIM [1:0]=00	–	2.0	–	A
			BOOST_ILIM [1:0]=01	–	1.0	–	
			BOOST_ILIM [1:0]=10	–	2.5	–	
			BOOST_ILIM[1:0]=11	–	3.0	–	

Output over-current threshold	I_{OUT_OC}	I_{OUT} rising		250	–	–	mA
Output over-voltage threshold	V_{OUT_OVP}	$O_{VP\_TH[3:0]}$	0010	–	43.75	–	V
			0011	–	41.875	–	
			…	–	…	–	
			1111	–	19.375	–	
Output over-voltage hysteresis	$V_{OUT\_OVP\_HYST}$	–		–	0.35	–	V
Accuracy of output over-voltage protection threshold	–	–		-5	–	5	%
LED current sinks (LED1 to LED8)							
LED current full-scale output range	I_{LED_MAX}	I^2C register setting MAX_I[4:0]	MAX_I [4:0]=00000	–	2	–	mA
			MAX_I [4:0]=00001	–	3	–	
			…	–	…	–	
			MAX_I [4:0]=11111	–	33	–	
Minimum sink current LED1–8	I_{LEDx_MIN}	IMAX programmed to 20 mA, linear mapping		–	4.88	–	µA
Leakage current	$I_{LED\_LEAKAGE}$	LED1…LED8 = 0, VOUT = 36V		–	–	1	µA
LED current matching[5]	$I_{LED\_MATCHING}$	IMAX programmed to 20 mA ILEDX programmed to full scale		-1	–	1	%
LED current matching[5]	$I_{LED\_MATCHING}$	IMAX programmed to 20 mA ILEDX programmed to 2% brightness level		-2.6	C	2.6	%
LED current accuracy[6]	$I_{LED\_ACCURACY}$	IMAX programmed to 20 mA ILEDX programmed to full scale		-2	C	2	%
LED regulation voltage	$V_{LED\_REGULATION}$	ILEDX programmed to 20 mA		–	320	–	mV
LED shorted string detection threshold	–	VLEDX falling	LED_SHORT_VTH [1:0] = 00	–	4.35	–	V
			LED_SHORT_VTH [1:0] = 01	–	4.85	–	
			LED_SHORT_VTH [1:0] = 10	–	5.25	–	
			LED_SHORT_VTH [1:0] = 11	–	5.75	–	
Current Ripple	–	ILED programmed to 20 mA DC LED current output		–	1	–	%
Internal PWM dimming							
Transition point between internal PWM and analog dimming	–	DIM_MODE=0		–	0	–	%
		DIM_MODE=1	PWM_IX[1:0] = 00	–	12.5	–	
			PWM_IX[1:0] = 01	–	25 (default)	–	
			PWM_IX[1:0] = 10	–	50	–	
			PWM_IX[1:0] = 00	–	100	–	
LED PWM output frequency	f_{LEDX}	PWM_DIM_FREQ[2:0]		2.79	–	22.49	kHz

LED current sink minimum output pulse width	–	–	–	350	–	ns
Logic interface						
EN logic input high voltage	V_{IH_EN}	–	1.2	–	–	V
EN logic input low voltage	V_{IL_EN}	–	–	–	0.4	V
PWM logic input high voltage	V_{IH_PWM}	–	0.9	–	–	V
PWM logic input low voltage	V_{IL_PWM}	–	–	–	0.5	V
Logic input current	$I_{PWM, IEN}$	–	-1.0	–	1.0	µA
ADDR input resistance	I_{ADDR_R}	–	–	100	–	kΩ
ADDR input high voltage	V_{IH_ADDR}	–	VCC-0.4V	–	–	V
ADDR input low voltage	V_{IL_ADDR}	–	–	–	0.4	V
PWM pin input frequency for internal PWM mode	F_{IPWM}	–	0.1	–	40	kHz
PWM pin minimum input high pulse	–	–	–	350	–	ns
PWM pin minimum input low pulse	–	–	–	350	–	ns
PC serial interface (SCL and SDA)						
SDA, SCL input high voltage	V_{IH}	–	1.26	–	3.6	V
SDA, SCL input low voltage	V_{IL}	–	–	–	0.99	V
SDA, SCL input hysteresis	V_{HYS}	–	–	0.1	–	V
SDA, SCL input current	I_{SCL}, I_{SDA}	–	–	–	1	µA
SDA output low level	V_{OL}	I_{SDA} = 20 mA	–	–	0.4	V
I^2C interface initial wait time		Initial wait time from EN logic high to the first accepted I^2C command	1	–	–	ms
SDA, SCL pin capacitance	$C_{I/O}$	–	–	–	10	pF
I^2C interface timing characteristics for standard, fast mode, and fast mode plus						
Serial clock frequency	F_{SCL}	Standard mode	–	–	100	kHz
		Fast mode	–	–	400	
		Fast mode plus	–	–	1000	
Clock low period	t_{LOW}	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
Clock high period	t_{HIGH}	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	

BUS free time between a STOP and a START condition	t_{BUF}	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
Setup time for a repeated START condition	$t_{SU:STA}$	Standard mode	4.7	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Hold time for a repeated START condition	$t_{HD:STA}$	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Setup time of STOP condition	$t_{SU:STO}$	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Data setup time	$t_{SU:DAT}$	Standard mode	0.25	–	–	µs
		Fast mode	0.1	–	–	
		Fast mode plus	0.05	–	–	
Data hold time	t_{HD_DAT}	Standard mode	0	–	–	µs
		Fast mode	0	–	–	
		Fast mode plus	0	–	–	
Rise time of SCL signal	t_{RCL}	Standard mode	–	–	1	µs
		Fast mode	0.02	–	0.3	
		Fast mode plus	–	–	0.12	
Fall time of SCL signal	t_{FCL}	Standard mode	–	–	0.3	µs
		Fast mode	–	–	0.3	
		Fast mode plus	–	–	0.12	
Rise time of SDA signal	t_{RDA}	Standard mode	–	–	1	µs
		Fast mode	0.02	–	0.3	
		Fast mode plus	–	–	0.12	
Fall time of SDA signal2	t_{FDA}	Standard mode	–	–	0.3	µs
		Fast mode	0.02	–	0.3	
		Fast mode plus	0.02	–	0.12	
Data valid time	t_{VD}	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
Data valid acknowledge time	t_{VDA}	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
Capacitive load for SDA and SCL	C_{BUS}	Standard mode	–	–	400	pf
		Fast mode	–	–	400	
		Fast mode plus	–	–	550	
MTP non-volatile memory write cycle time	–	–	–	–	50	ms

Notes:

1. Min/max specifications are 100% production tested at $T_A=T_J$ = 25 °C, unless otherwise noted. Limits over the operating range are guaranteed by design.
2. Guaranteed by design.

3. Thermal shutdown is not production tested.
4. VBAT and VOUT ranges must meet valid operating regions when in CCM operation:
   $(VBAT \leq \frac{VOUT}{2.15})$
5. The sink current matching is defined and tested as $(I_{LED\_MAX} - I_{LED\_MIN})/I_{LED\_AVG}$.
6. The LED current accuracy is defined and tested as: $100*(I_{LED\_AVG} - I_{LED\_Target})/I_{LED\_AVG}$.

Pin Configuration

This section includes the PE23108 30-pin configuration information. Figure 3 shows the pin map of this device for the 3.445 mm x 2.095 mm WLCSP package. Table 5 lists the descriptions for each pin.

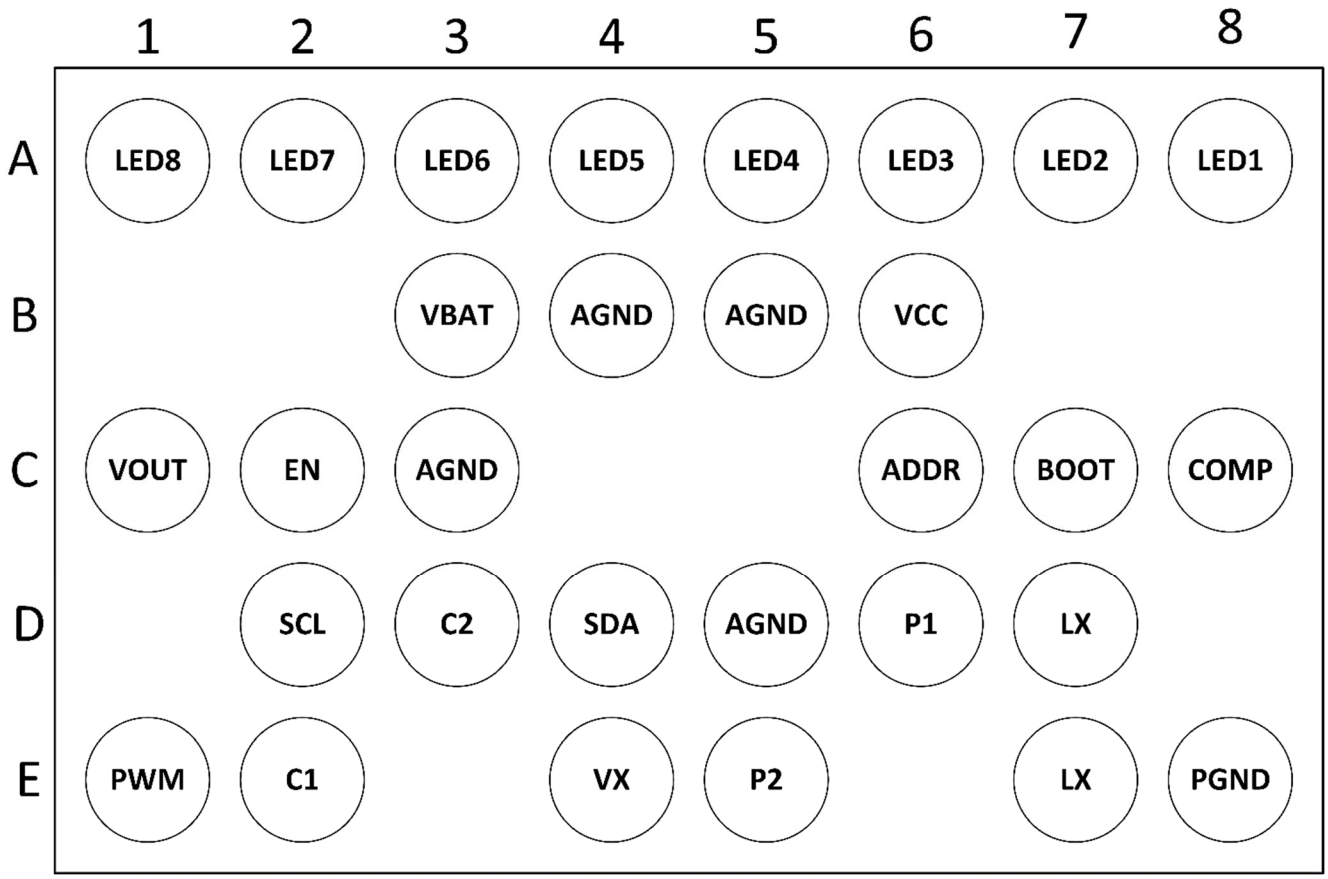


Figure 3. Pin Configuration (Top View)

Pin Descriptions

Table 5 lists the PE23108 pin descriptions. For the capacitor and inductor selection guidelines, see Component Selection on page 55.

Table 5. PE23108 Pin Descriptions

Pin No.	Pin Name	Description
A1	LED8	Individual LED current sink. Connect to the low side of individual LED strings.
A2	LED7	Individual LED current sink. Connect to the low side of individual LED strings.
A3	LED6	Individual LED current sink. Connect to the low side of individual LED strings.
A4	LED5	Individual LED current sink. Connect to the low side of individual LED strings.
A5	LED4	Individual LED current sink. Connect to the low side of individual LED strings.
A6	LED3	Individual LED current sink. Connect to the low side of individual LED strings.
A7	LED2	Individual LED current sink. Connect to the low side of individual LED strings.
A8	LED1	Individual LED current sink. Connect to the low side of individual LED strings.
B3	VBAT	LED boost input voltage, battery power supply pin.
B4, B5, C3, D5	AGND	Analog and LED current sink ground, star ground to system ground plane.
B6	VCC	IC input voltage. Connect to a 3.3V or 5V supply.
C1	VOUT	Power converter output voltage. Connect to the high side of all LED strings. Connect externally to four 2.2 µF 0603 capacitors.
C2	EN	Enable input
C6	ADDR	Sets lower three bits of the I^2C slave address. Tie to AGND pin for ‘000’. Leave floating for 010. Tie to VCC pin for 101.
C7	BOOT	Bootstrap capacitor for the boost stage high side FET. Connect a 2.2 nF, 10V or higher capacitor from BOOT to LX.
C8	COMP	External compensation pin. For details, see Switching Converter Compensation on page 27.
D2	SCL	Serial clock for I^2C bus.
D3	C2	Charge pump fly capacitor positive node. Connect two 4.7 µF 0603 capacitors from C2 to P2.
D4	SDA	Serial data for I^2C bus.
D6	P1	Charge pump fly capacitor phase node. Connect two 4.7 µF 0603 capacitors from P1 to C1.
D7,E7	LX	Fully synchronous switching node for the boost power inductor, which connects between LX and input voltage VBAT.
E1	PWM	PWM dimming input for brightness control. If not used, connect to the VCC pin.
E2	C1	Charge pump fly capacitor positive node. Connect two 4.7 µF 0603 capacitors from C1 to P1.
E4	VX	Charge pump input node, internally driven by the output of the boost converter. Connect a 2.2 µF 0402 capacitor between this pin and PGND.
E5	P2	Charge pump fly capacitor phase node. Connect two 4.7 µF 0603 capacitors from P2 to C2.
E8	PGND	Power ground must tie externally to system ground plane. High current path.

Operating Voltage Range and Charge Pump Ratio

The PE23108 uses a 2X charge-pump to improve efficiency. The charge pump architecture requires the battery input voltage to be less than the output voltage divided by 2.15 when boost DC-DC is operating in continuous conduction mode (CCM) condition:

$$VBAT \leq \frac{VOUT}{2.15}$$

Functional Block Diagram

Figure 4 shows the PE23108 functional block diagram.

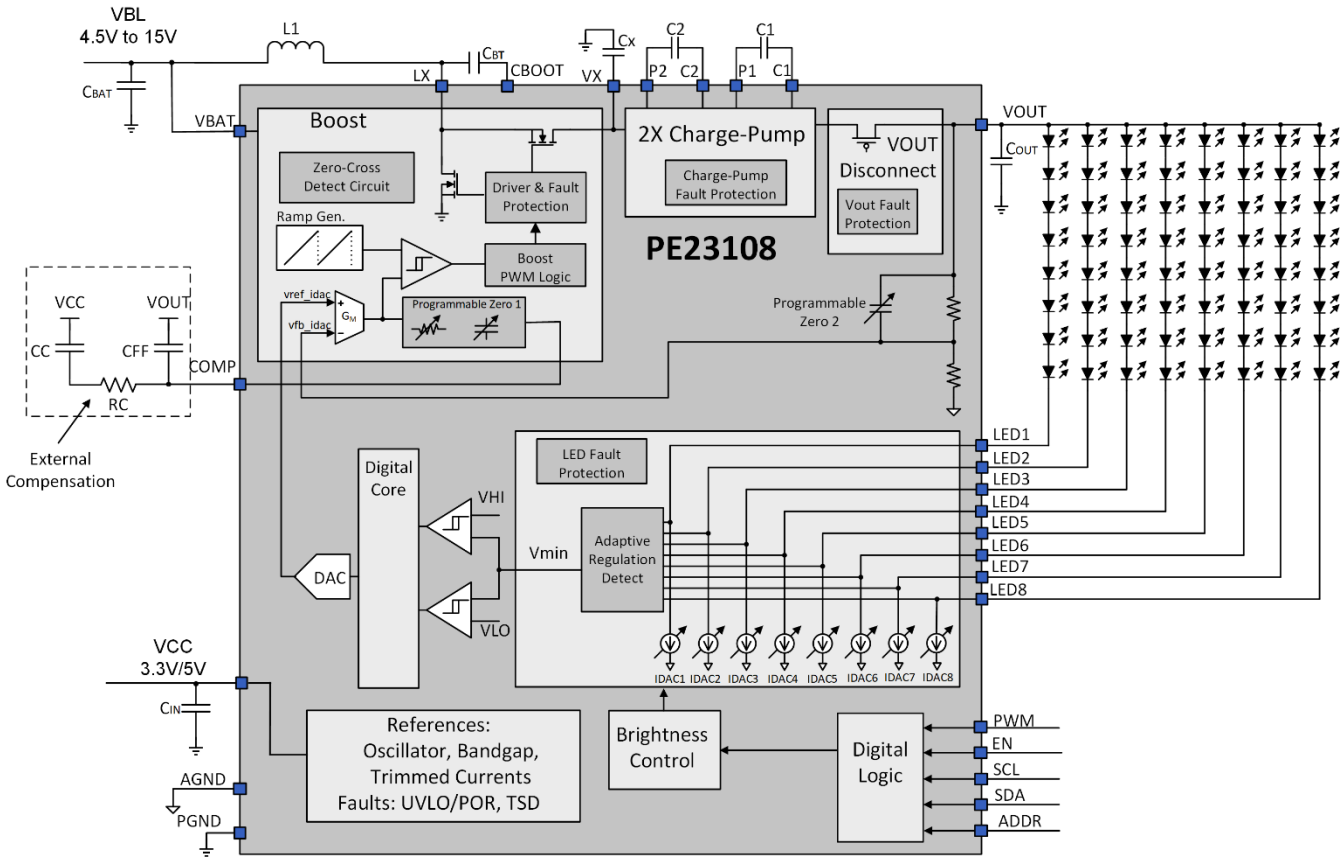


Figure 4. PE23108 Functional Block Diagram

Application Circuit

For the application circuit, star ground PGND and AGND on a system ground plane.

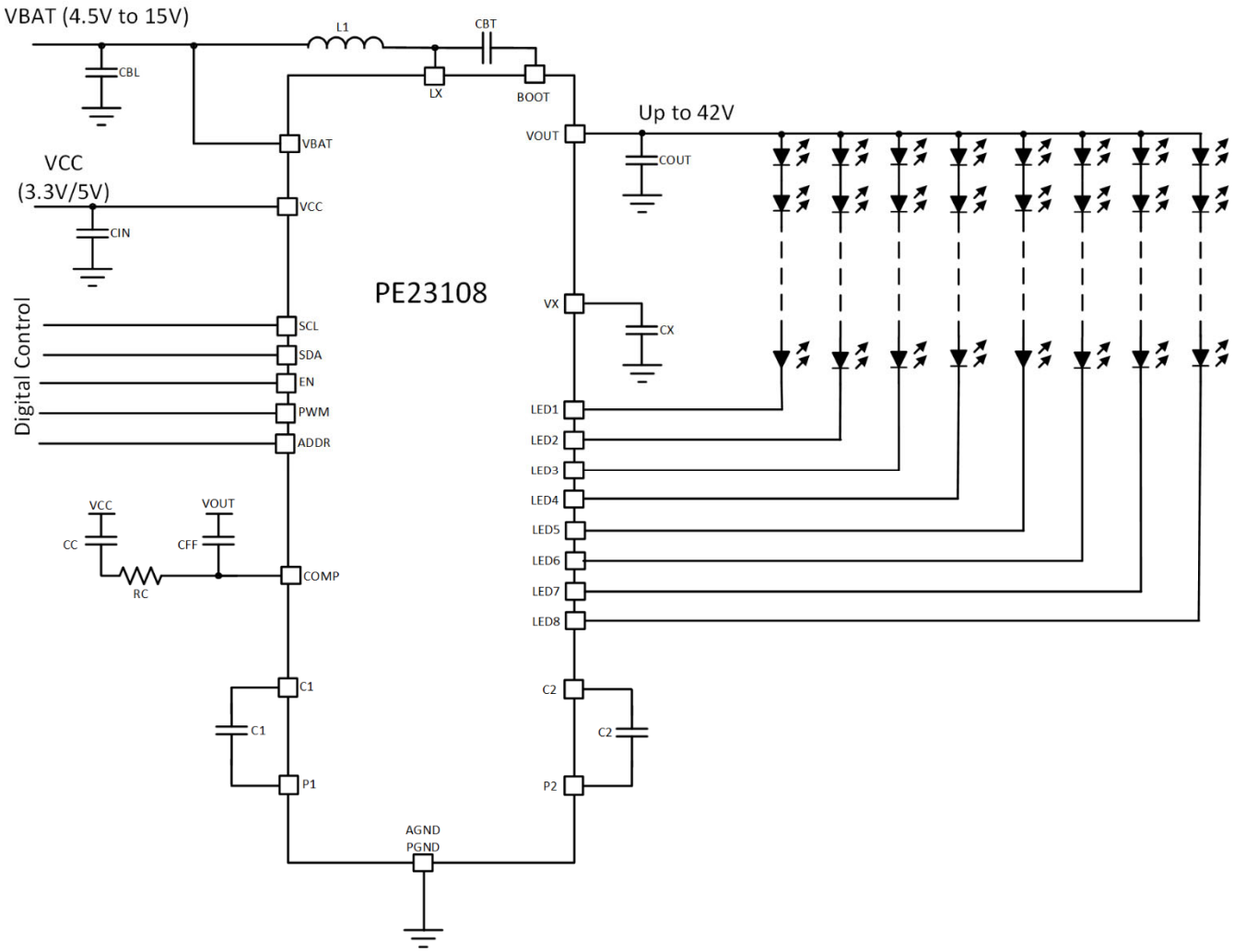


Figure 5. I²C Interface Application Schematic

Typical Performance Data

Figure 6–Figure 11 show the PE23108 typical performance data at VCC = 3.3V, VBAT = 12V, L1=10 µH, C_{OUT} = 4 x 2.µF, I_{MAX} = 20 mA, LED VF = 2.8V at 20 mA (typical), and analog dimming, unless otherwise specified.

Efficiency: 286 kHz boost switching frequency

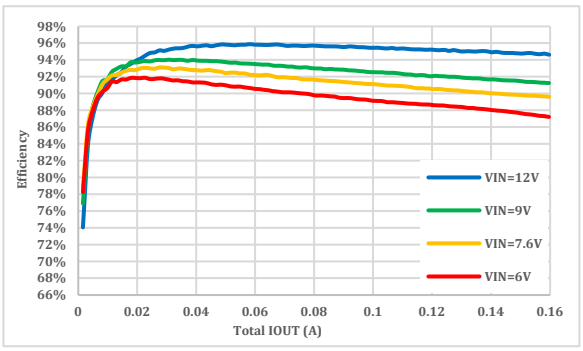


Figure 6. 8P10S Boost Efficiency[1], 10 µH Inductor

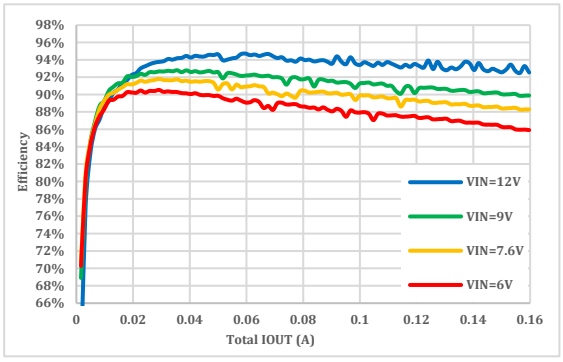


Figure 7. 8P10S System Efficiency[2], 10 µH Inductor

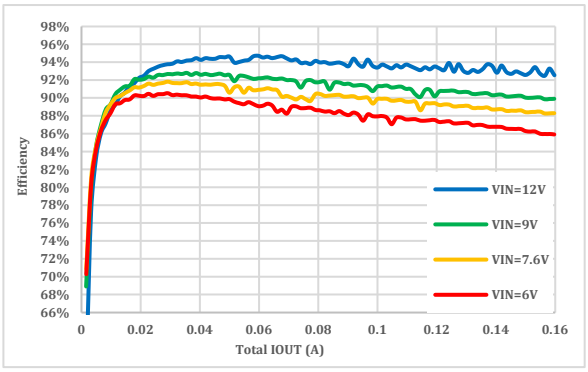


Figure 8. 8P12S Boost Efficiency[1], 10 µH Inductor

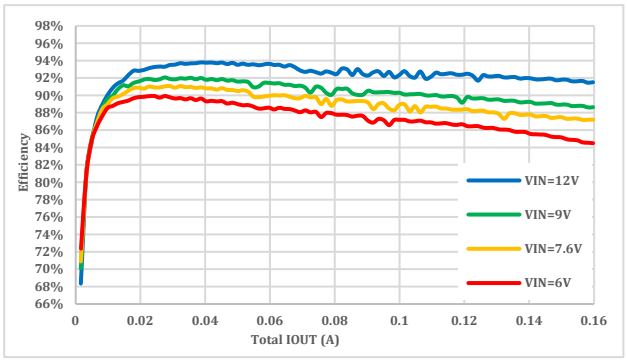


Figure 9. 8P12S System Efficiency[2], 10 µH Inductor

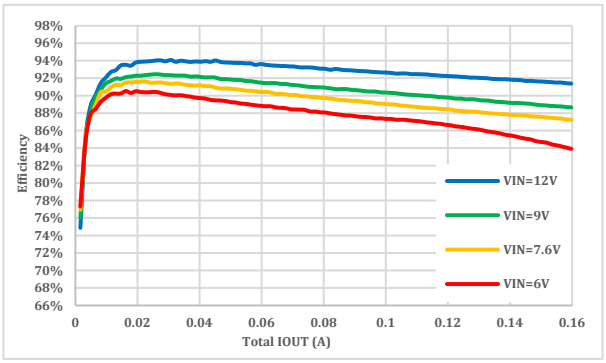


Figure 10. 8P14S Boost Efficiency[1], 10 µH Inductor

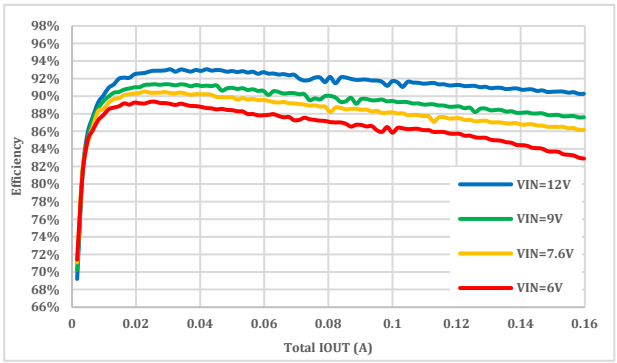


Figure 11. 8P14S System Efficiency[2], 10 µH Inductor

Notes:

1. Boost Efficiency = POUT/PVBAT
2. System Efficiency = (VOUT-VREG) * IOUT / (PVBAT+PVCC), where VREG = LED regulation voltage.

Figure 12–Figure 17 show the PE23108 typical performance data at VCC = 3.3V, VBAT = 12V, L1=10 µH, C_{OUT} = 4 x 2.µF, I_{MAX} = 20 mA, LED VF = 2.8V at 20 mA (typical), and analog dimming, unless otherwise specified.

Efficiency: 715 kHz boost switching frequency

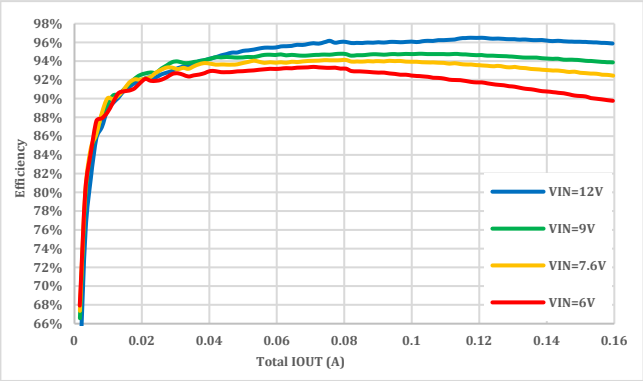


Figure 12. 8P10S Boost Efficiency[1], 10 µH Inductor

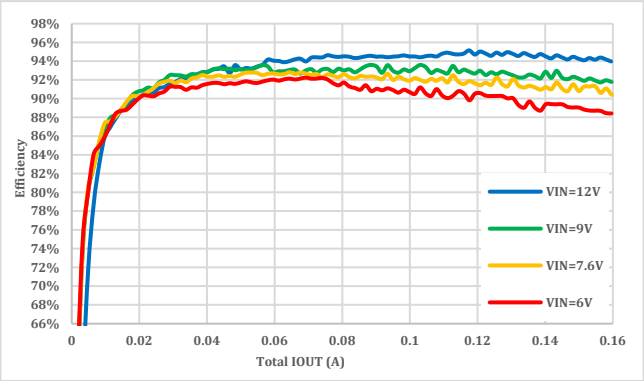


Figure 13. 8P10S System Efficiency[2], 10 µH Inductor

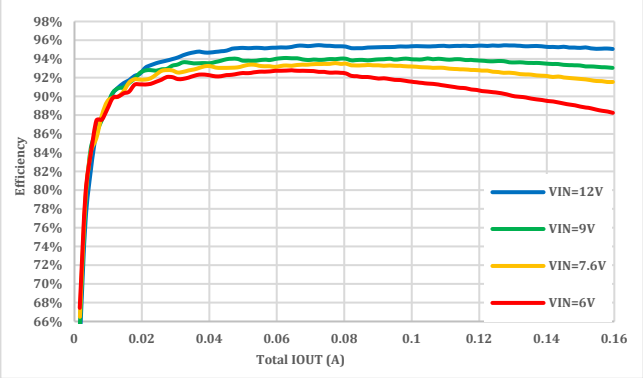


Figure 14. 8P12S Boost Efficiency[1], 10 µH Inductor

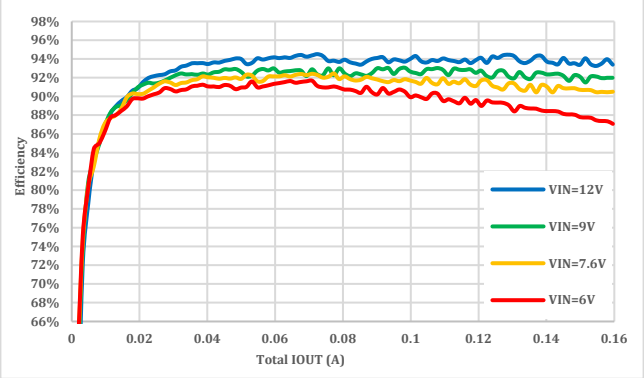


Figure 15. 8P12S System Efficiency[2], 10 µH Inductor

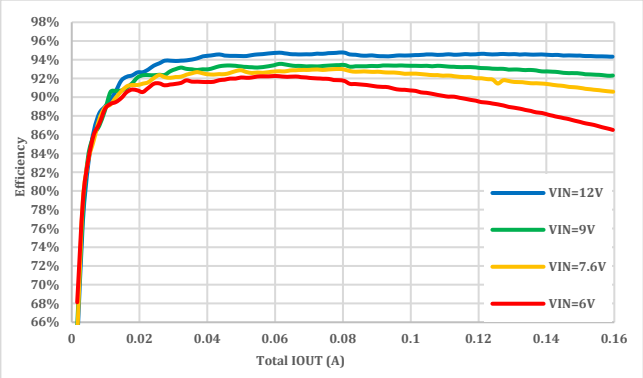


Figure 16. 8P14S Boost Efficiency[1], 10 µH Inductor

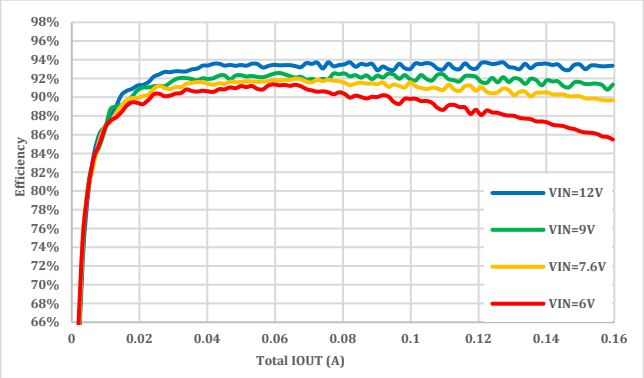


Figure 17. 8P14S System Efficiency[2], 10 µH Inductor

Notes:

1. Boost Efficiency = POUT/PVBAT
2. System Efficiency = (VOUT-VREG) * IOUT / (PVBAT+PVCC), where VREG = LED regulation voltage.

Figure 18–Figure 23 show the PE23108 typical performance data at VCC = 3.3V, VBAT = 12V, L1=10 µH, C_{OUT} = 4 x 2.µF, I_{MAX} = 20 mA, LED VF = 2.8V at 20 mA (typical), and analog dimming, unless otherwise specified.

Efficiency: 953 kHz boost switching frequency

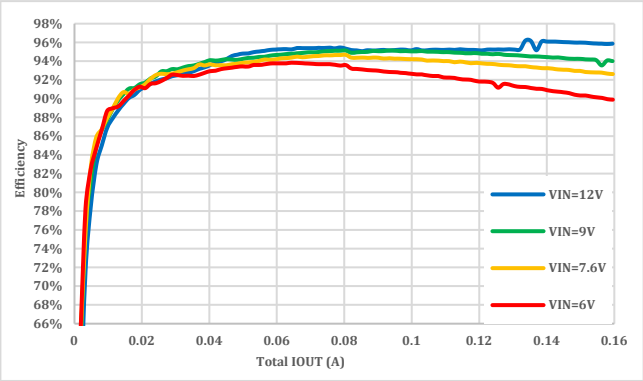


Figure 18. 8P10S Boost Efficiency[1], 10 µH Inductor

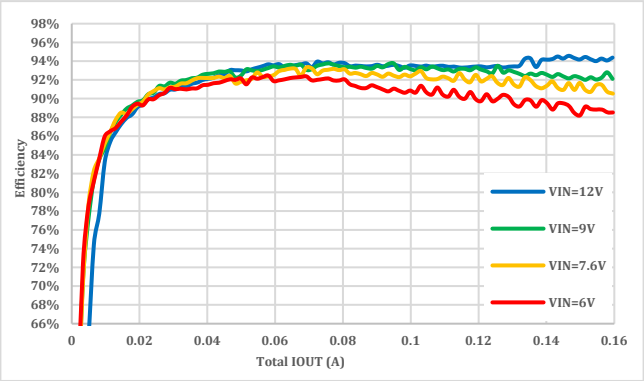


Figure 19. 8P10S System Efficiency[2], 10 µH Inductor

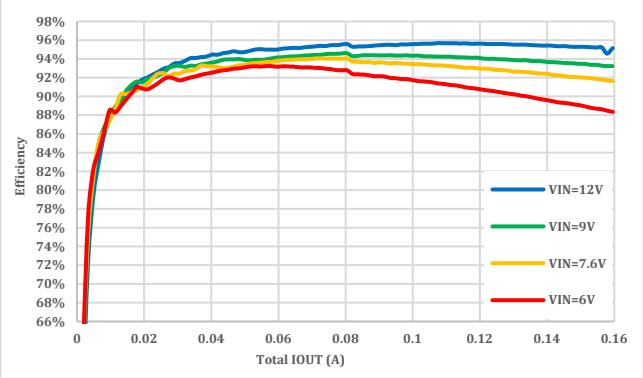


Figure 20. 8P12S Boost Efficiency[1], 10 µH Inductor

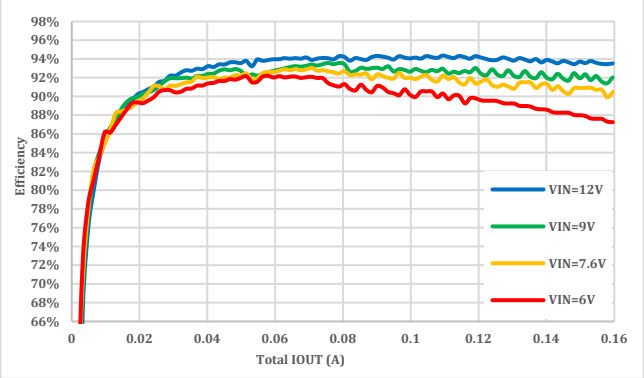


Figure 21. 8P12S System Efficiency[2], 10 µH Inductor

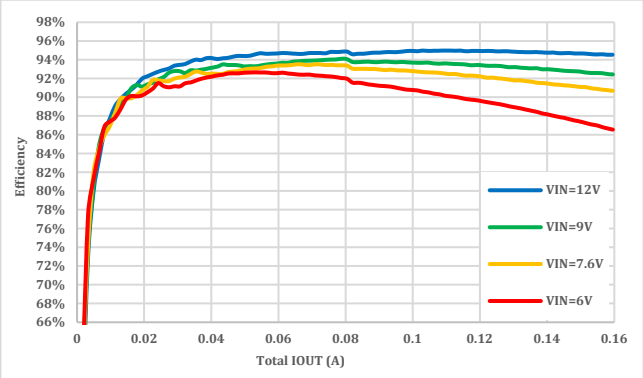


Figure 22. 8P14S Boost Efficiency[1], 10 µH Inductor

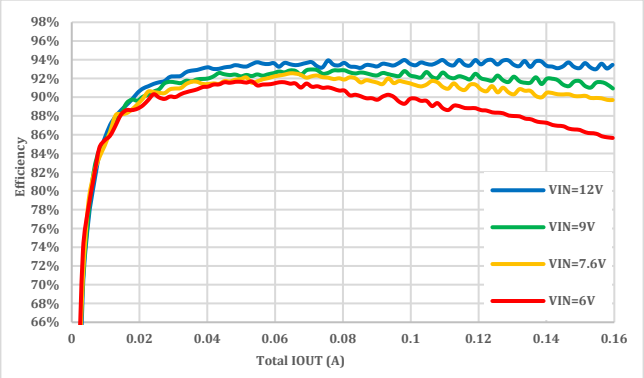


Figure 23. 8P14S System Efficiency[2], 10 µH Inductor

Notes:

1. Boost Efficiency = POUT/PVBAT
2. System Efficiency = (VOUT-VREG) * IOUT / (PVBAT+PVCC), where VREG = LED regulation voltage.

Figure 24–Figure 27 show the PE23108 typical performance data at VCC = 3.3V, VBAT = 12V, L1=10 µH, C_{OUT} = 4 x 2.µF, I_{MAX} = 20 mA, LED VF = 2.8V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED current sinks

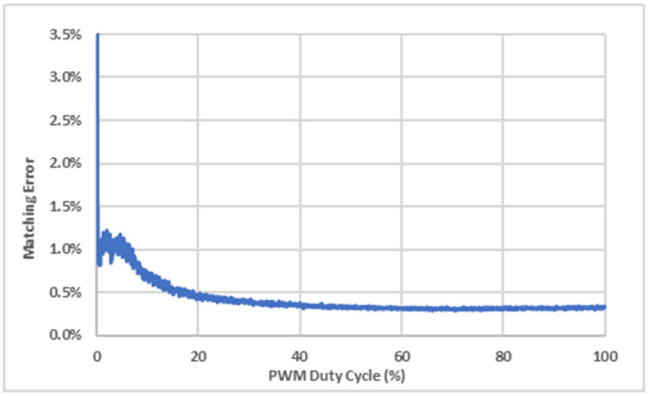


Figure 24. LED matching: Analog (DC) dimming mode at 20 mA MAX_I

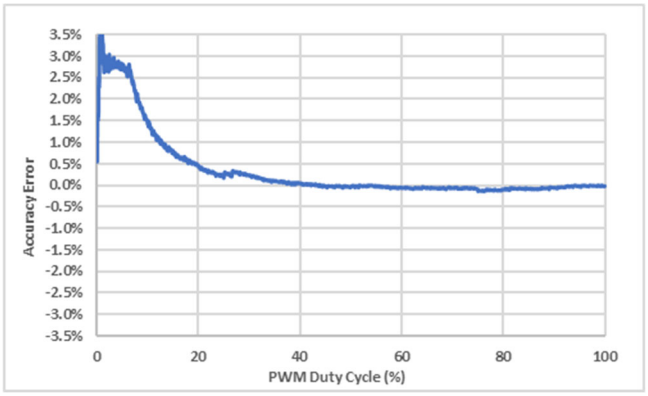


Figure 25. LED accuracy – Analog (DC) dimming mode at 20 mA MAX_I

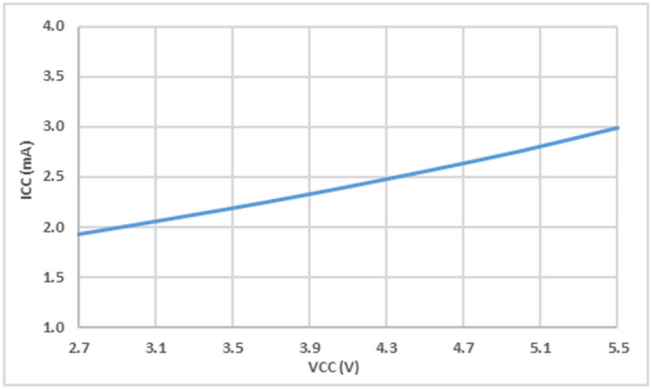


Figure 26. ICC vs. VCC at 10 mA MAX_I, Fsw=715 kHz

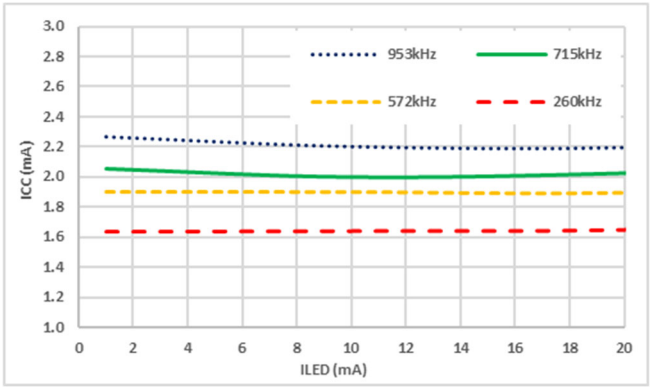


Figure 27. ICC vs. ILED at VCC = 3.3V

Startup Characteristics

Figure 28–Figure 30 show the PE23108 startup characteristics at VCC = 3.3V, VBAT = 12V, L1=10 µH, C_{OUT} = 4 x 2.µF, I_{MAX} = 20 mA, LED VF = 2.8V at 20 mA (typical), and analog dimming, unless otherwise specified.

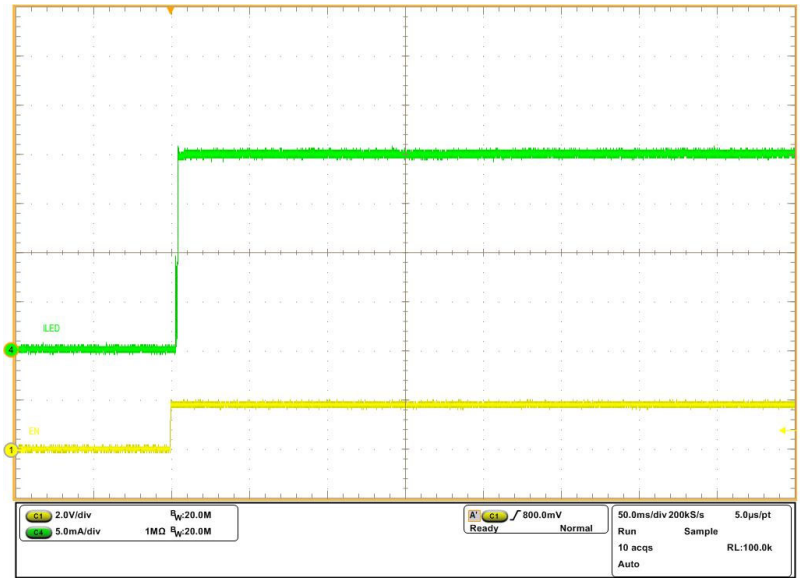


Figure 28. Startup under 99% PWM condition. 8P12S configuration. Hybrid dimming @ 25%. VBAT = 12V (CH1 – EN, CH4 – ILED)

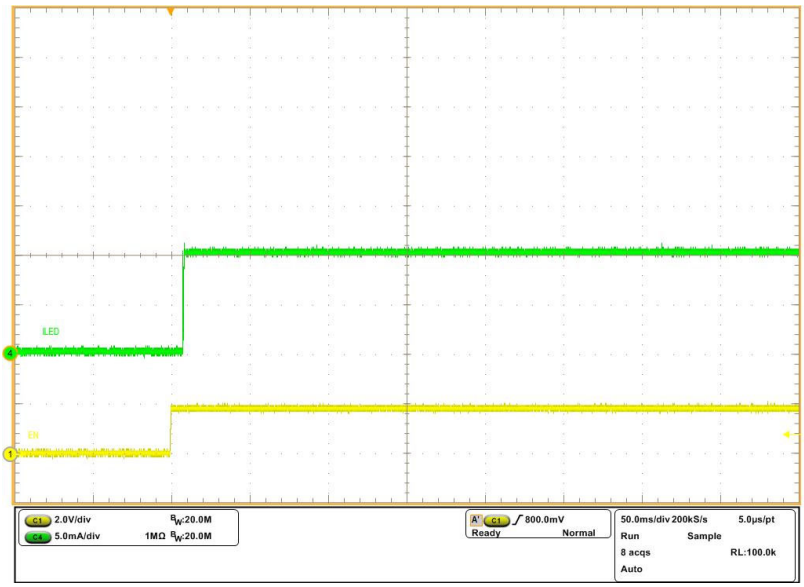


Figure 29. Startup under 50% PWM condition. 8P12S configuration. Hybrid dimming @ 25%. VBAT = 12V (CH1 – EN, CH4 – ILED)

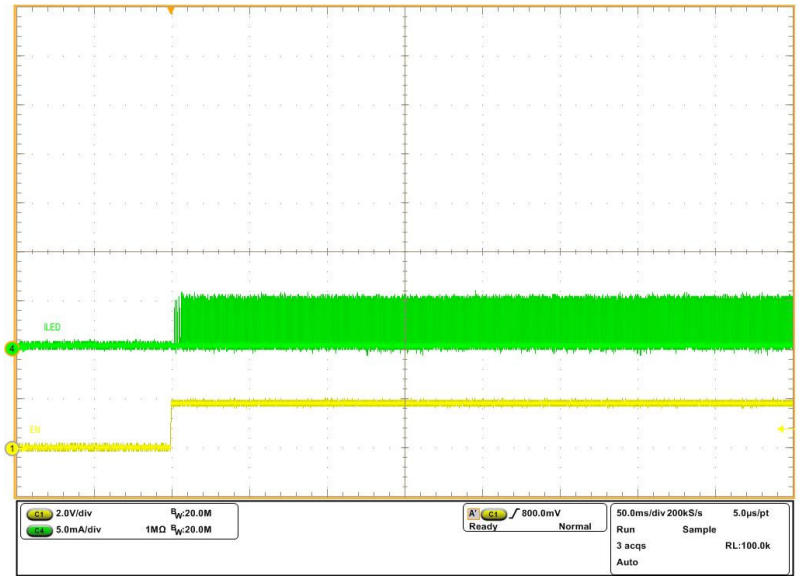


Figure 30. Startup under 1% PWM condition. 8P12S configuration. Hybrid dimming @ 25%. VBAT = 12V (CH1 – EN, CH4 – ILED)

Thermal Performance

Figure 24 shows the PE23108 thermal performance at VCC = 3.3V, VBAT = 12V, L1=10 µH, C_{OUT} = 4 x 2.µF, I_{MAX} = 20 mA, LED VF = 2.8V at 20 mA (typical), and analog dimming, unless otherwise specified.

Figure 31. PE23108 Thermal Performance

Conditions

- 8p14s configuration
- 38.8V VOUT
- 120 mA IOUT
- 6V VBAT
- 3.3V VCC
- 0.454W power dissipation
- 1.0 mm 10-µH Inductor (DFE322512F-100M)
- Ambient temperature (T_A) is 25 °C
- Maximum case temperature is 42.5 °C close to the LX and PGND pins of the package

Detailed Description

The PE23108 uses a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve high peak efficiencies and superior efficiency over the two-cell/three-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the LED selection.

The PE23108 supports 1–8 LED strings. Tie unused LEDx pins to ground. This provides maximum design flexibility for wide variety of LCD screens. Strings can be paralleled together to drive an LED string at a higher current.

The PE23108 provides a full set of protection features to ensure robust system operation that includes the following:

- Input voltage under-voltage lockout (UVLO)
- Thermal shutdown (TSD)
- Boost and charge pump over-current protection (OCP)
- Boost and charge pump output over-voltage and under-voltage protection (OVP and UVP)
- LED open and short detection

Input Sequencing Requirements

Although there is no specific input sequencing requirement, pSemi recommends the following sequence:

1. Apply VCC.
2. Apply VBAT.
3. Apply EN.

The IC enables when the following conditions are met:

- VBAT > $V_{VBAT\text{-}UVLO\_H}$
- VCC > $V_{VCC\text{-}UVLO\_H}$
- EN > V_{IH_EN}

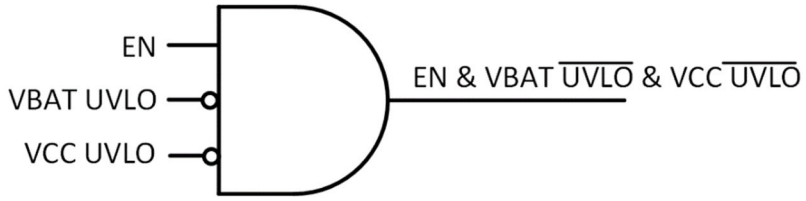


Figure 32. Input Sequencing Logic Diagram

The sequence for the PWM pin does not matter. It can be switched according to the application requirements or at 0%/100% while all other inputs are being turned on and off. Table 6 lists the various PE23108 input conditions.

Table 6. Input Conditions

VCC	VBAT	EN	Device Status
Low	Low	Low	Non-operational
High	High	Low	Non-operational
Low	High	High	Non-operational
High	Low	High	Non-operational
High	High	High	Full device operational

Under-voltage Lockout (UVLO)

The PE23108 continuously monitors the VCC and VBAT inputs. If the VCC voltage drops below approximately 2.5V or if the VBAT voltage drops below approximately 4.2V, the PE23108 immediately shuts down.

Output Over-voltage and Under-voltage Protection

The PE23108 protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when VOUT rises above the over-voltage threshold V_{OUT_OVP}. When a VOUT OVP occurs, the VOUT_OVP bit of the STATUS1 register is updated to 1, and the PE23108 stops the boost converter from switching. The boost converter restarts switching after an OVP event when VOUT decreases 350 mV hysteresis below the OVP threshold.

The over-voltage threshold can be configured through the OVP_TH[3:0] bits in COMMAND register. The accuracy of each over-voltage threshold is ±5%.

Table 7. Over-voltage Threshold

VOUT_OVP_SEL[3:0]	VOUT Over-voltage Threshold (V)
0000	Reserved
0001	
0010	43.75
0011	41.875
0100	40.0
0101	38.125
0110	36.25
0111	34.375
1000	32.5
1001	30.625
1010	28.75
1011	26.875
1100	25.0
1101	23.125
1110	21.25
1111	19.375

Select the output over-voltage threshold with enough voltage margin above the highest expected operating VOUT voltage in the application to ensure proper LED open or grounded string fault detection. The highest expected operating VOUT voltage is a function of the number of series LEDs used, the highest LED forward voltage expected, and the regulation voltage at the LED pins during the maximum LED current used in the application per channel.

Reset and Standby Functions

Table 8 lists the RESET and Standby states when the part uses the I²C interface. For all modes: UVLO high = POR IC (entire chip shutdown).

Table 8. RESET and Standby States

EN Pin Logic Level	I2C_STANDBY	LEDEN[8:1]	Reset	Status	Internal Block ON	Register
0	–*	–	–	OFF	None	Cleared
1	0	0	0	Ready	References ON, Boost/CP off, LED drivers on standby	I²C accessible
1	0	>0	0	ON	All ON	I²C accessible
1	1	–	–	Standby	All off except UVLO + critical reference circuits	I²C accessible
1	0	–	1 (self-clearing)	Reset -> Ready (self-clearing)	Ready state after self-clearing reset	Cleared

Note: * A dash (–) in this table denotes that the level can be high or low and does not affect operation.

The STATUS1 and STATUS2 register bits are all cleared upon read, so the repeated read-back of a logic-high fault bit indicates that the fault event remains persistent.

Boost Output Over-voltage and Under-voltage Protection

The PE23108 monitors the boost output (VX) voltage by initiating over-voltage protection (VX_OV) when VX rises above a typical over-voltage threshold of 22.25V. When a VX OVP occurs, the VX_OVP bit of the STATUS1 register is updated to a 1, and the PE23108 boost converter stops switching. The boost converter restarts switching after a VX_OV event when VX decreases below the VX_OV threshold plus a 0.5V typical hysteresis.

If the boost output voltage (VX) falls below the VBAT voltage plus a VBAT-proportional offset after the LED current sinks have turned on, the PE23108 shuts down the switching converter and the LED current sinks immediately and the VX_UV register bit in the STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and do not start unless the part is shutdown or reset as listed in Table 8.

The PE23108 can detect a missing or unconnected inductor upon startup by monitoring the boost output before enabling the switching converter and LED strings. When an inductor open is detected, the switching converter and LED strings remain off and the SS_TIMEOUT and VX_UV bits in the STATUS1 register are set and are cleared upon read.

Soft-Start Timeout

The PE23108 implements a soft-start timeout fault. If the output voltage does not rise above 2x of the battery voltage within 10 ms, the switching converter and the LED current sinks are disabled. The SS_TIMEOUT bit in the STATUS1 register is set to 1. This is a latched fault. The PE23108 does not start up until a reset event occurs, such as by toggling EN low or setting the RESET bit in the CONFIG4 register (which clears itself).

LED Short Protection

The PE23108 includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator enables when at least one LED pin is in regulation and the shorted LED fault is triggered when an LEDx voltage rises above the shorted LED voltage threshold. The shorted LED voltage threshold can be programmed to 4.35V, 4.85V, 5.25V, and 5.75V by using the CONFIG3 register LED_SHORT_VTH[1:0] bits. This fault condition can occur when some LEDs in a string are electrically bypassed, making that LED string shorter than the other LED strings. The threshold level is referenced to ground.

The reduced forward voltage causes the current sink attached to that string to have a higher voltage than other current sinks, which could cause overheating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED short fault is recorded in the STATUS1 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the LED strings is open, the output rises until it crosses the VOUT OVP threshold. Any string under-regulation at that moment is blocked from controlling VOUT, resulting in the output decreasing to a level needed to regulate the remaining non-open LED strings. An LED open fault is recorded in the STATUS2 register.

If the open LED string is reconnected, the LED current sink re-establishes the current to the level based on the output voltage, but it is not allowed to control the VOUT voltage. To re-enable the output control for any faulted strings, turn off all LEDs or reset the part.

Over-current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit. It starts up initially with a derated over-current limit of 1.0A typically for soft start. The cycle-by-cycle over-current limit can be programmed to 1A, 2A, 2.5A or 3A by using the CONFIG1 register BOOST_ILIM[1:0] bits. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults in which the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds the secondary current limit—which is 1-2A above the programmed BOOST_ILIM[1:0] setting—the converter and the LED current sinks are disabled immediately. The STATUS1 register BST_ILIM_SEC bit is set and is cleared upon read. The switching converter and the LED current sinks remain latched off and do not restart unless the part is shutdown or reset.

A separate short-circuit detection is implemented if the output voltage drops suddenly, forcing a large current out of the charge pump. The output is disconnected from the charge pump and the LED current sinks are temporarily disabled. The boost and charge pump remain switching, regulating at the last-known voltage level. The STATUS1 register DISC_OCP bit is set. The LED current sinks are enabled again when the fault at the VOUT pin is removed.

Current Setting

The LED output maximum currents are set by the CONFIG2 register MAX_I[4:0] bits. The default maximum current is 20 mA per LED string with 31 further settings available: 2 mA to 33 mA in 1 mA increment per step. pSemi trims parts for current accuracy at the default MAX_I[4:0] of 20 mA.

Fine-tuning of the maximum current of the LED outputs can be set by the VREG_IMAXTUNE register IMAXTUNE[3:0] bits. This allows incremental increases in the maximum output current from the MAX_I[4:0] setting mentioned above, in 4-bit resolution (16 steps) ranging from 0% to 7.66% with an average 0.51% per step. Using IMAXTUNE[3:0] to increase the maximum output current from these default values can result in some loss of accuracy.

Table 9. Current Settings

MAX_I[4:0]	Full-scale ILED Ccurrent (mA)	MAX_I[4:0]	Full-scale ILED Current (mA)
00000	2	10000	18
00001	3	10001	19
00010	4	10010	20
00011	5	10011	21
00100	6	10100	22
00101	7	10101	23
00110	8	10110	24
00111	9	10111	25
01000	10	11000	26
01001	11	11001	27
01010	12	11010	28
01011	13	11011	29
01100	14	11100	30
01101	15	11101	31
01110	16	11110	32
01111	17	11111	33

Boost Converter Switching Frequency

The PE23108 boost converter provides wide frequency selection to meet different application requirements. Four bits set the boost switching frequency(f_{SW_BOOST}), which are the CONFIG1 register FSW_BOOST[3:0] bits, as listed in Table 10.

The choice of inductor, charge pump fly capacitors, and compensation components depend on the selected boost switching frequency for proper part operation. For the recommended component types and values, contact pSemi.

Table 10. Boost Switching Frequency Settings

Frequency (kHz)	FSW_BOOST[3:0] binary code
1430	0010
953	0011
715	0100
572	0101
477	0110
409	0111
358	1000
318	1001
286	1010
260	1011
238	1100
220	1101
204	1110
191	1111

Charge Pump Switching Frequency

Table 11 lists the default relationship between the LED brightness setting and the charge-pump frequency ratio from the boost switching frequency. The charge-pump frequency ratio and relationship to the LED brightness setting are programmable using the CONFIG_CP register CP_FREQ_TRAN, SEL_CP_FREQ, and CP_FREQ_DIV[1:0] bits, as described on page 49.

pSemi recommends the following selections:

- 1/8 CP frequency for IOUT ≤ 120 mA
- 1/4 CP frequency for 120 mA < IOUT ≤ 180 mA
- 1/2 CP frequency for IOUT > 180 mA

Table 11. Charge-Pump Frequency Ratio

CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1]	CP_FREQ_DIV[0]	CP Frequency Ratio
0	0	X	X	1/8 at <50% LED brightness 1/4 between ≥50% and <75% LED brightness 1/2 at ≥75% LED brightness
0	1	0	0	1/2 across entire LED brightness range
0	1	0	1	1/4 across entire LED brightness range
0	1	1	0	1/8 across entire LED brightness range
0	1	1	1	1/8 across entire LED brightness range
1	X	X	0	1/4 at <50% LED brightness 1/2 at ≥50% LED brightness
1	X	X	1	1/8 at <50% LED brightness 1/4 at ≥50% LED brightness

Switching Converter Compensation

The switching converter operates in hybrid voltage-mode control and uses Type-II compensation which requires two external components, as shown in Figure 33.

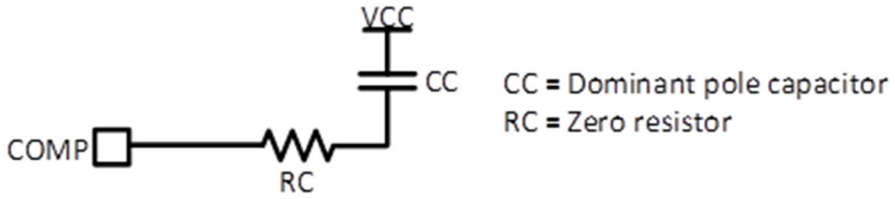


Figure 33. Compensation Components

Table 12 lists the recommended compensation component selection for different inductor values. The SEL_VR[2:0] bits set the control loop DC gain.

For a more specific set of compensation components to optimize the bandwidth and phase margin for your application, contact pSemi.

Table 12. Compensation Components

Inductor (µh)	RC Value (kΩ)	CC Value (nF)	SEL_VR[2:0]
10	200	2.2	110

LED Current Output Dimming

The PE23108 supports three LED current output dimming options for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency and minimal WLED color shift at low brightness levels. These options are analog, phase-shift PWM, and hybrid PWM (mixed-mode) dimming.

Analog Dimming (DC Modulation)

When the CONFIG2 register DIM_MODE bit is set to 0, dimming is set to analog only. In analog dimming, the LED current sink output is always a DC current across the entire brightness range. As the brightness is reduced, the LED current sink output DC level decreases, which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the VOUT voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with a DC current output also minimizes noise in the system.

Phase-shift PWM Dimming

When the CONFIG2 register DIM_MODE bit is set to 1, PWM dimming is enabled. In this mode, the mixed dimming block generates phase-shifted PWM signals to dim the active LED strings when the required LED current is below the threshold set by the PWM_IX[1:0] register bits. The phase difference between the active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

When the LED current outputs are PWM dimming, their switching frequency can be selected from one of four frequency settings between 2.79 kHz and 22.49 kHz using the PWM_DIM_FREQ[2:0] register bits.

Hybrid PWM (Mixed-Mode) Dimming

The PE23108 allows a mixed dimming output scheme for better optical efficiency. The switch point from analog to PWM dimming is set by register bits DIM_MODE=1 and PWM_IX[1:0], and can be 12.5%, 25%, 50%, or 100% of the brightness range. 100% means that PWM dimming is used across the whole brightness range. In the brightness range above the switch point, analog dimming is adopted, and below the switch point, PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved while minimizing system noise at higher brightness levels.

- PWM_IX[1:0]=11 results in a DC output current only when the LED brightness setting is at 100%, otherwise the LED current sink switches off and on to 100% of its full-scale output level.
- PWM_IX[1:0]=10 results in a DC output current only when the LED brightness setting is at 50% or greater, otherwise the LED current sink switches off and on to 50% of its full-scale output level.
- PWM_IX[1:0]=01 results in a DC output current only when the LED brightness setting is at 25% or greater, otherwise the LED current sink switches off and on to 25% of its full-scale output level.
- PWM_IX[1:0]=00 results in a DC output current only when the LED brightness setting is at 12.5% or greater, otherwise the LED current sink switches off and on to 12.5% of its full-scale output level.

Figure 34 shows an example of the LED current output for any one channel at the PWM_IX[1:0]=01 setting.

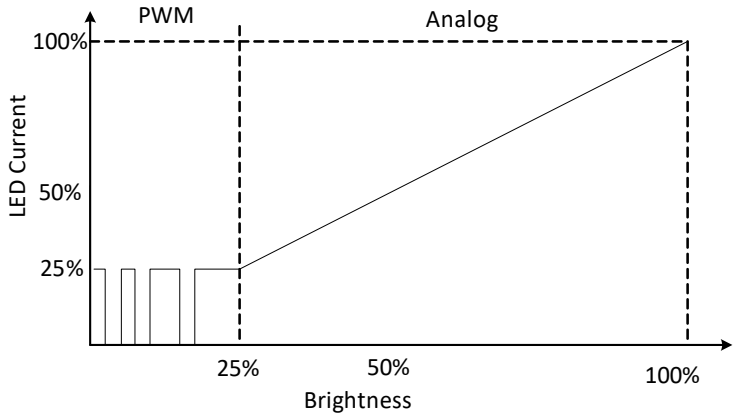


Figure 34. Mixed-Mode Dimming

The choice of four brightness transition points between analog dimming and PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Because the LED current output peak during PWM dimming scales proportionally with the brightness transition point, the LED current pulse width also must scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0]=01 (25% transition point) is four times longer than at PWM_IX[1:0]=11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is typically 700 ns.

LED Brightness Control

The LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET_MSB and WLED_ISET_LSB registers written through the I²C interface, or both. The register bits DIMCODE[1:0] select the three different brightness control options described in this section.

DIMCODE = 00

When DIMCODE = 00, the LED current is controlled only by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate a DC current level or phase-shifted PWM currents at the LED strings.

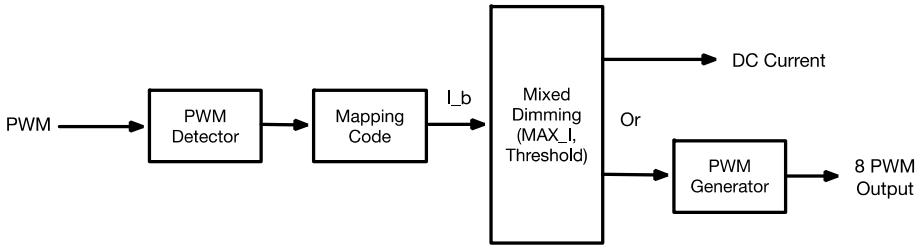


Figure 35. DIMCODE = 00

DIMCODE = 01

When DIMCODE = 01, the LED current is controlled by the WLED_ISET_MSB and WLED_ISET_LSB registers through the I²C interface. The register codes go through a mapping first, then through the mixed dimming block to generate a DC current level or eight phase-shifted PWM currents at the LED strings. Write to the WLED_ISET_LSB register and then the WLED_ISET_MSB register to update the 12-bit dimming value.

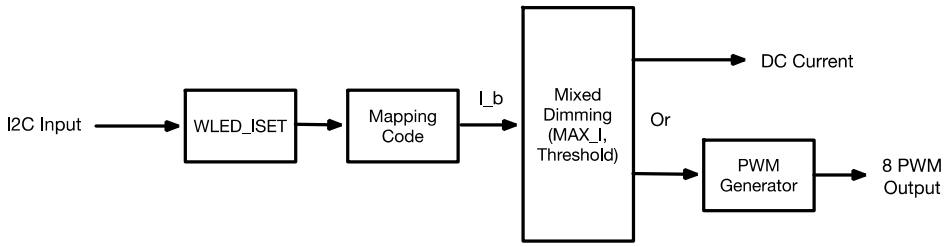


Figure 36. DIMCODE = 01

DIMCODE = 10

When DIMCODE = 10, the LED current is controlled by the PWM input duty cycle and the WLED_ISET_MSB and WLED_ISET_LSB register values through the I²C interface. The register codes go through a mapping first and are then multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate a DC current level or eight phase-shifted PWM currents.

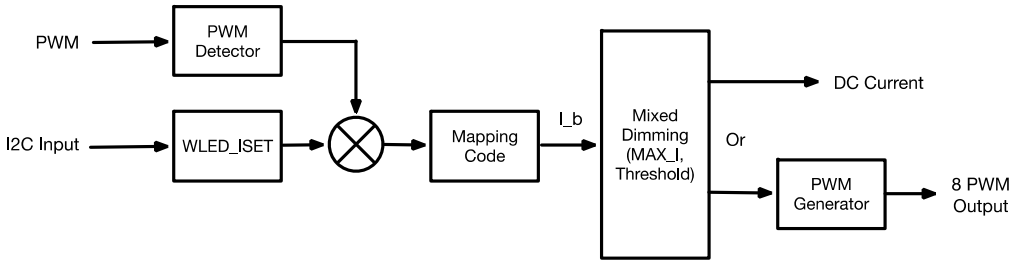


Figure 37. DIMCODE = 10

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either through the PWM input or WLED_ISET_MSB and WLED_ISET_LSB registers are translated linearly into the LED current. This is the factory default setting. There are 4095 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit = 0), and 32767 possible brightness states with the dither function enabled (DITHER_ENABLE bit = 1).

For a better visual experience, the PE23108 can also translate the dimming settings via a logarithmic mapping to produce the LED current. The user can set the LOG_MODE bit to 1 in the CONFIG2 register to enable this feature. There are 1023 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit = 0), and 8191 possible brightness states with the dither function enabled (DITHER_ENABLE bit = 1).

With the dither function enabled, the PE23108 uses the DITHER_LSB[2:0] bits combined with WLED_ISET_MSB[11:4] and WLED_ISET_LSB[3:0] to form a 15-bit LED output current setting, where the DITHER_LSB[2:0] bits become the lower LSBs. You can then write to the eight MSBs in register 0x06 first, then the 7 LSBs in register 0x05, for a 15-bit resolution LED dimming adjustment.

PWM Input and Output Resolution

With DIMCODE = 00, the brightness is controlled by the input PWM signal. The PE23108 PWM input frequency range is 100 Hz to 40 KHz. The input frequency is independent of the PWM output frequency. The PWM output frequency is set by the PWM_DIM_FREQ[2:0] register bits.

Because the on-chip clock is 2.857 MHz, a 12-bit PWM input resolution can be obtained with at 697 Hz PWM input signal (2.857 MHz/2^12 = 697 Hz). Lower PWM input frequencies increase the PWM input resolution, and higher PWM input frequencies reduce the PWM input resolution. Table 13 lists the input resolution at different PWM input frequencies.

Table 13. Input Resolution at Different PWM Input Frequencies

PWM Input Frequency	Input Resolution (bits)
$f_{PWM} \leq 174$ Hz	14
174 Hz < $f_{PWM} \leq 349$ Hz	13
349 Hz < $f_{PWM} \leq 697$ Hz	12
697 Hz < $f_{PWM} \leq 1.395$ kHz	11
1.395 kHz < $f_{PWM} \leq 2.79$ kHz	10
2.79 kHz < $f_{PWM} \leq 5.58$ kHz	9
5.58 kHz < $f_{PWM} \leq 11.16$ kHz	8
11.16 kHz < $f_{PWM} \leq 22.32$ kHz	7

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0]=11). A 2.79 kHz PWM output frequency setting (PWM_DIM_FREQ[2:0]=001) provides 10 bits of dimming resolution relative to the full-scale LED output current, so each 25% segment has 8 bits of dimming resolution. In hybrid dimming, depending on the hybrid transition point, a higher resolution can be achieved by selecting a lower transition point. For example, with a 25% transition point, the same 2.79 kHz PWM output frequency setting would provide a 10 bits resolution from 0% to 25% dimming range vs 8 bits in 100% PWM dimming. The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

The PE23108 provides a dithering function by increasing the dimming resolution. With the DITHER_ENABLE bit set to 1, the dimming resolution increases by three bits by using the DITHER_LSB[2:0] bits as the lower 3 LSB. These three LSB bits combine with the WLED_ISET[11:0] to provide 15-bit of dimming resolution. Table 14 lists the output resolution at the different PWM output frequency settings.

Table 14. Output Resolution at Different PWM Output Frequency Settings

PWM Output Frequency Setting (kHz)	Output Resolution (bits)	Output Resolution with Dither ON (bits)
2.79	10	13
5.59	9	12
11.2	8	11
22.49	7	10

Fade In/Out Control

The Fade in/out control makes a smooth transition from one brightness value to another for a better human eye experience. The PE23108 provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED register FADING_SPEED[7:0] bits. For more details, see the FADING_SPEED register on page 40.

Digital R-C Filter Mode Brightness Change

Due to the variability in the rate of consecutive discrete input brightness changes, it is not possible to select a single fading speed and still produce a visibly smooth output brightness change for all use cases. To resolve this issue, an RC-filter is used to filter the output brightness change response to each input brightness change.

The FILTER_SETTING register RCFILTER[1:0] bits control the coefficient of this RC time constant—as shown in Table 15—for a specific case of brightness changes between 1% and 99%. The RC filter coefficient is independent of the PWM_DIM_FREQ[2:0] frequency settings.

Table 15. RC Filter Settings

RCFILTER[1:0]	RC Time Constant (T, in ms)
00	Disabled
01	417
10	207
11	103

Input PWM Filter

When a duty cycle is applied at the PWM pin to control brightness, the on-time and period are sampled by the internal 2.857 MHz master clock to translate time-domain information into binary values. As inherent with any sampling of an asynchronous signal, the sampled binary values can jitter by ±1 LSB at steady-state, which translates into jitter on the final brightness result, and this can be visible as flicker. Adding some basic filtering to this sampled system can help to eliminate this flicker at steady-state.

The FILTER_SETTING register PWMFILTER[2:0] bits enable or disable this filter and control the amount of filtering. Furthermore, the filtering depends on the direction of the sampled PWM time-step, as follows:

- If the PWM time-step has been decreasing, the sampled binary value is allowed to decrement regardless of the delta time-step size but prevented from incrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.
- If the PWM time-step has been increasing, the sampled binary value is allowed to increment regardless of the delta time-step size but prevented from decrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.

The time-step size is 700 ns.

Table 16. PWM Filter Settings

PWMFILTER[2:0]	Minimum PWM Time-step Size (steps)
000	Off
001	2
010	4
011	6
100	8
101	10
110	12
111	14

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both the SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA, and SCL. A master device such as a microcontroller or a digital signal processor controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives or transmits data on the bus under control of the master device.

The PE23108 operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification:

- Standard mode (100 Kbps)
- Fast mode (400 Kbps)
- Fast mode plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the VCC and VBAT voltages remain above UVLO and the EN pin remains asserted.

The data transfer protocol for standard and fast modes is the same, so they are referred to as F/S-mode in this document. The PE23108 supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as ‘1001XXX‘.

Programming I²C Slave Address - Multiple Parts on One I²C Bus

To enable multiple PE23108 parts to be addressed on one I²C bus, the lower three bits of the I²C slave address are programmable by using the ADDR pin. The ADDR pin configuration to the device 7-bit address and 8-bit address with $R/\overline{W}$ low is shown in Table 17.

Table 17. ADDR Pin Configuration

ADDR Pin	Device 7-Bit Address	Device 8-Bit Address with R/=0
Tied to AGND	1001000 (0x48)	10010000 (0x90)
Floating	1001010 (0x4A)	10010100 (0x94)
Tied to VCC	1001101 (0x4D)	10011010 (0x9A)

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 38. All I²C-compatible devices must recognize a start condition.

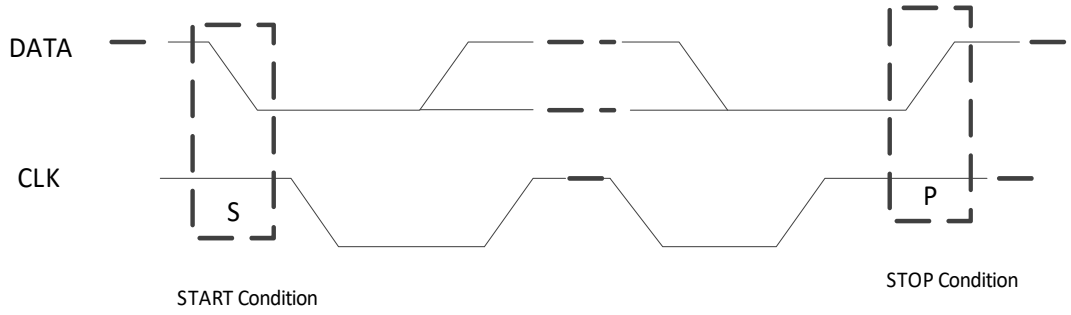


Figure 38. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/Wb on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. See Figure 39.

The master generates further SCL cycles to either transmit data to the slave (R/"W" bit 0) or receive data from the slave ($R/\overline{W}$ bit 1). In either case, the receiver must acknowledge the data sent by the transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. Nine-bit valid data sequences consisting of 8-bit data and a 1-bit acknowledge can continue as long as needed.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 38. This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section result in FFh being read out.

PE23108 I²C Update Sequence

The PE23108 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, PE23108 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the PE23108. The PE23108 performs an update on the falling edge of the acknowledge signal that follows the LSB.

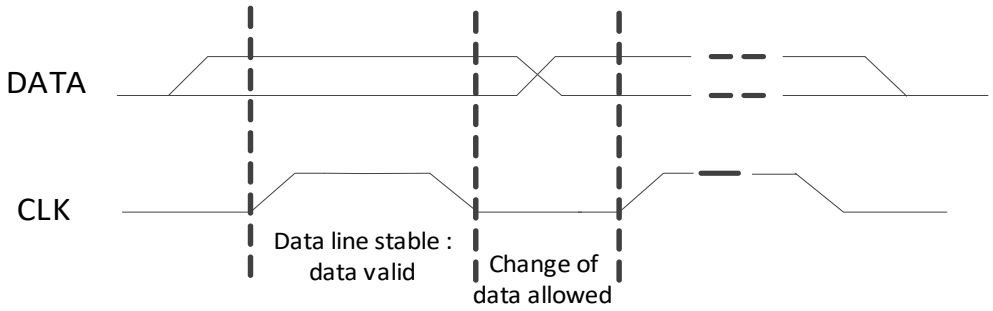


Figure 39. Bit Transfer on the Serial Interface

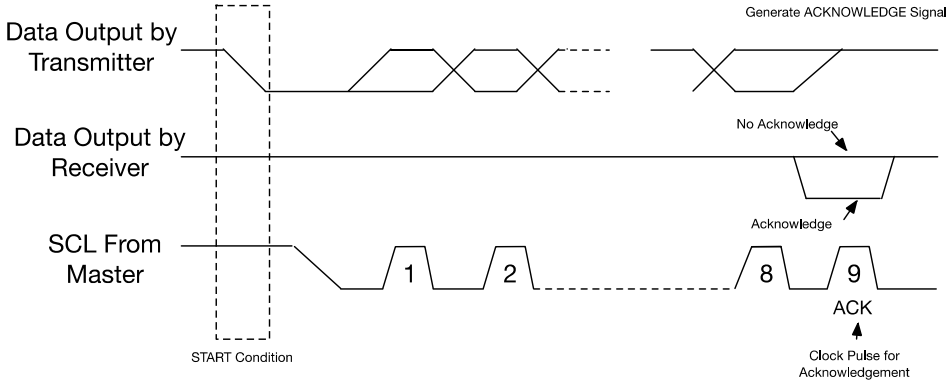


Figure 40. Acknowledge on the I²C Bus

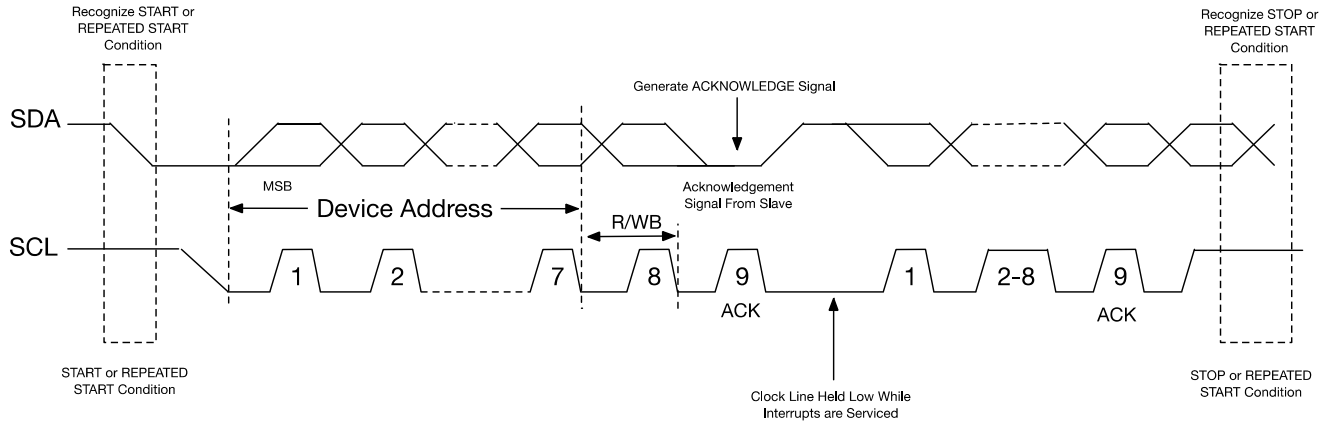


Figure 41. Bus Protocol

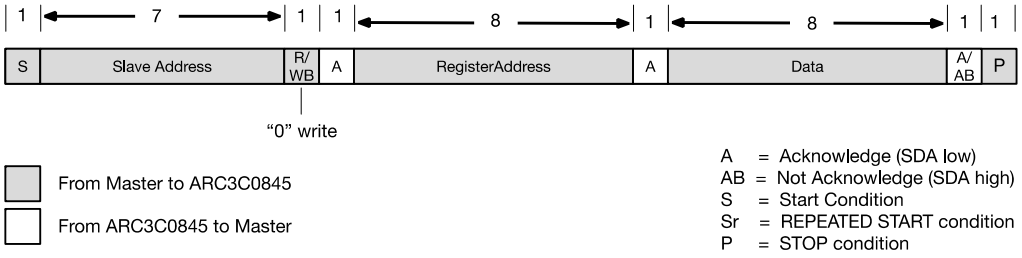


Figure 42. "Write" Data Transfer Format in Standard, Fast, Fast-Plus Modes

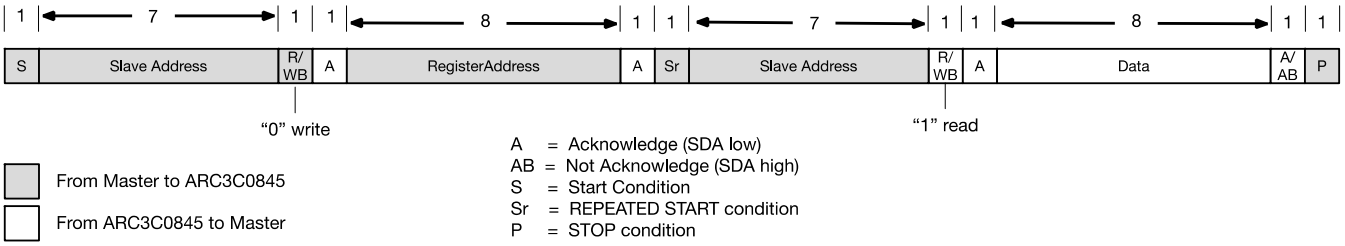


Figure 43. "Read" Data Transfer Format in Standard, Fast, Fast-Plus Modes

PE23108 MTP Non-volatile Memory Description

The PE23108 contains non-volatile memory (NVM) to store the default values for registers 0x00–0x0B. The data in the NVM is recalled to the registers at the device POR event. This function saves system initialization time by allowing you to program the device default setting in the production line instead of programming these settings every time after a POR event. To perform the MTP programming cycle, first write the preferred values for registers 0x00 to 0x0B. Then set the MTP_WRITE_CMD[4:0] bits to 10010 to initialize the MTP programming. During the MTP programming cycle, the MTP_WRITE_CMD[4:0] bits remain at 10010 and MTP_WRITE_DNE bit is at 0. When the MTP programming cycle completes, the MTP_WRITE_CMD[4:0] bits automatically reset back to 00000 and MTP_WRITE_DNE bit is set to 1. The MTP programming cycle takes 50 ms maximum to complete. During the MTP programming cycle, do not write to registers 0x00–0x0B to avoid data corruption.

Register Maps

Slave Address: 1001000 (0x48)

Register Configuration Parameters*

Register	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	SEL_VR[2:0]			BOOST_ MODE	OVP_TH[3:0]			
CONFIG1	0x01	Reserved	BOOST_ILIM[1:0]		Reserved	FSW_BOOST[3:0]			
FADING_ SPEED	0x02	FADING_SPEED[3:0]				Reserved			
CONFIG2	0x03	Reserved	LOG_MODE	DIM_MODE	MAX_I[4:0]				
LEDEN	0x04	LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1
WLED_ISET_ LSB	0x05	WLED_ISET_LSB[3:0]				DITHER_LSB[2:0]			Reserved
WLED_IST_ MSB	0x06	WLED_IST_MSB[11:4]							
CONFIG3	0x07	Reserved	LED_SHORT_VTH[1:0]		PWM_IX[1:0]		PWM_DIM_FREQ[2:0]		
CONFIG4	0x08	I2C_ STANDBY	Reset	Reserved					
FILTER_ SETTINGS	0x09	DIMCODE[1:0]		DITHER_ ENABLE	RCFILTER[1:0]		PWMFILTER[2:0]		
VREG_ IMAXTUNE	0x0A	LED_VREG_CNT_INIT[3:0]				IMAXTUNE[3:0]			
CONFIGCP	0x0B	Reserved				CP_FREQ_ TRAN	SEL_CP_ FREQ	CP_FREQ_DIV[1:0]	
CKSUM0	0x0C	CHKSUM0[7:0]							
CKSUM1	0x0D	CHKSUM1[7:0]							
STATUS1	0x0E	BST_ILIM_ SEC	VOUT_OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_ TIMEOUT	LED_ SHORT
STATUS2	0x0F	MTP_WRITE_CMD[4:0]					MTP_WRITE _DNE	CRC_OK	LED_OPEN

Note: * ADDR pin tied to GND. Excluding read/write bit. 10010000 (0x90) if including R/Wb bit = 0.)

Detailed Register Description

Register COMMAND

Address	Name	POR Value(*)
0x00	COMMAND	0xC2

Bit Assignment

7	6	5	4	3	2	1	0
SEL_VR[2:0]			BOOST_MODE	OVP_TH[3:0]			

Bit Description

Field Name	Bits	Type	POR(*)	Description
SEL_VR[2:0]	[7:5]	$R/\overline{W}$	110	3-bit selection of control loop DC GAIN: From the highest (000) to the lowest (111) in 2-dB increments. For the recommended setting, see Switching Converter Compensation on page 27.
BOOST_MODE	[4]	$R/\overline{W}$	0	0 = DCM fixed-frequency boost switching (no negative inductor current) 1 = Forced CCM fixed-frequency boost switching (negative inductor current allowed)
OVP_TH[3:0]	[3:0]	$R/\overline{W}$	0010	4-bit selection of the VOUT OVP thresholds: 0010 = 43.75V (default) 0011 = 41.875V 0100 = 40V 0101 = 38.125V 0110 = 36.25V 0111 = 34.375V 1000 = 32.5V 1001 = 30.625V 1010 = 28.75V 1011 = 26.875V 1100 = 25V 1101 = 23.125V 1110 = 21.25V 1111 = 19.375V

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG1

Address	Name	POR Value(*)
0x01	CONFIG1	0x4B

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	BOOST_ILIM[1:0]		Reserved	FSW_BOOST[3:0]			

Bit Description

Field Name	Bits	Type	POR(*)	Description
Reserved	[7], [4]	$R/\overline{W}$	0	Reserved
BOOST_ILIM[1:0]	[6:5]	$R/\overline{W}$	10	Boost cycle-by-cycle ILIM threshold: 00 = 2.0A 01 = 1.0A 10 = 2.5A (default) 11 = 3.0A
FSW_BOOST[3:0]	[3:0]	$R/\overline{W}$	1011	Boost switching frequency. For the full frequency chart, see Boost Converter Switching Frequency on page 26. 0000–0010 = 1.43 MHz 0011 = 953 kHz 0100 = 715 kHz 0101 = 572 kHz 0110 = 477 kHz 0111 = 409 kHz 1000 = 358 kHz 1001 = 318 kHz 1010 = 286 kHz 1011 = 260 kHz (default) 1100 = 238 kHz 1101 = 220 kHz 1110 = 204 kHz 1111 = 191 kHz

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register FADING_SPEED

Address	Name	POR Value(*)
0x02	FADING_SPEED	0x02

Bit Assignment

7	6	5	4	3	2	1	0
FADING_SPEED[3:0]				Reserved			

Bit Description

Field Name	Bits	Type	POR(*)	Description
FADING_SPEED[3:0]	[7:4]	$R/\overline{w}$	0000	Sets the fading counter value. This is the period between each intensity step. 0000 = No fading (default) 0001 = 44.70 µs per step 0010 = 1.432 ms per step 0011 = 2.148 ms per step 0100 = 2.860 ms per step 0101 = 3.548 ms per step 0110 = 4.290 ms per step 0111 = 5.012 ms per step 1000 = 5.700 ms per step 1001 = 6.440 ms per step 1010 = 7.160 ms per step 1011 = 7.800 ms per step 1100 = 8.590 ms per step 1101 = 9.300 ms per step 1110 = 10.024 ms per step 1111 = 10.700 ms per step
Reserved	[3:0]	$R/\overline{w}$	0010	Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG2

Address	Name	POR Value(*)
0x03	CONFIG2	0x12

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	LOG_MODE	DIM_MODE	MAX_I [4:0]				

Bit Description

Field Name	Bits	Type	POR(*)	Description
Reserved	[7]	$R/\overline{W}$	0	Reserved
LOG_MODE	[6]	$R/\overline{W}$	0	Dimming mode selector: 0 = Linear mode (default) 1 = Logarithmic mode. The log table uses 1023 codes with the dither function disabled and up to 8191 codes with the dither function enabled.
DIM_MODE	[5]	$R/\overline{W}$	0	Dimming mode selector: 0 = Analog dimming only (default) 1 = Mixed-mode dimming
MAX_I [4:0]	[4:0]	$R/\overline{W}$	10010	Program maximum current per string in 1-mA steps: 00000 = 2 mA 00001 = 3 mA 00010 = 4 mA 00011 = 5 mA 00100 = 6 mA 00101 = 7 mA 00110 = 8 mA 00111 = 9 mA 01000 = 10 mA 01001 = 11 mA 01010 = 12 mA 01011 = 13 mA 01100 = 14 mA 01101 = 15 mA 01110 = 16 mA 01111 = 17 mA 10000 = 18 mA 10001=19 mA 10010 = 20 mA (default) 10011 = 21 mA 10100 = 22 mA 10101 = 23 mA 10110 = 24 mA 10111 = 25 mA 11000 = 26 mA 11001 = 27 mA 11010 = 28 mA 11011 = 29 mA 11100 = 20 mA 11101 = 31 mA 11110 = 32 mA 11111 = 33 mA

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register LEDEN

Address	Name	POR Value(*)
0x04	LEDEN	0xFF

Bit Assignment

7	6	5	4	3	2	1	0
LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1

Bit Description

Field Name	Bits	Type	POR(*)	Description
LEDEN_8…LEDEN_1	[7:0]	$R/\overline{w}$	0	LED string enabled: 0 = string is disabled 1 = string is enabled (default)
Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.				

Register WLED_ISET_LSB

Address	Name	POR Value(*)
0x05	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				DITHER_LSB[2:0]			Reserved

Bit Description

Field Name	Bits	Type	POR(*)	Description
WLED_ISET[3:0]	[7:4]	$R/\overline{w}$	0000	LED output current setting bits 1-0. For details, see LED Brightness Control on page 30. If changing the LSB bits, these must be written before the MSB bits. Changes to these bits are only implemented when the next register is written, which is typically the MSBs but could be any register.
DITHER_LSB[2:0]	[3:1]	$R/\overline{w}$	000	With DITHER_ENABLE=1, these three bits combine with WLED_ISET[11:0] as the lower LSBs to form a 15-bit ILED dimming control. Write to these bits along with WLED_ISET[11:0] for 15-bit dimming adjustment.
Reserved	[0]	$R/\overline{w}$	0	Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register WLED_ISET_MSB

Address	Name	POR Value(*)
0x0	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[9:4]							

Bit Description

Field Name	Bits	Type	POR(*)	Description
WLED_ISET[9:4]	[7:0]	$R/\overline{w}$	00000000	The MSB bits of the WLED_ISET[9:0] brightness code. For details, see LED Brightness Control on page 30.
Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.				

Register CONFIG3

Address	Name	POR Value(*)
0x07	CONFIG3	0x0B

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	LED_SHORT_VTH [1:0]		PWM_IX [1:0]		PWM_DIM_FREQ[2:0]		

Bit Description

Field Name	Bits	Type	POR(*)	Description
Reserved	[7]	$R/\overline{w}$	0	Reserved
LED_SHORT_VTH [1:0]	[6:5]	$R/\overline{w}$	00	LED short detect threshold: 00 = 4.35V (default) 01 = 4.85V 10 = 5.25V 11 = 5.75V
PWM_IX [1:0]	[4:3]	$R/\overline{w}$	01	PWM_IX[1:0] transition point between analog dimming and PWM dimming during mode change: 00 = 12.5% 01 = 25% (default) 10 = 50% 11 = 100% (also 100% PWM dimming)
PWM_DIM_FREQ[2:0]	[2:0]	$R/\overline{w}$	011	PWM_DIM_FREQ in kHz: 000 = 2.79 kHz 001 = 5.59 kHz 010 = 11.2 kHz 011 = 22.49 kHz (default) 100…111 = Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG4

Address	Name	POR Value(*)
0x08	CONFIG4	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2C_STANDBY	RESET	Reserved					

Bit Description

Field Name	Bits	Type	POR(*)	Description
I2C_STANDBY	[7]	$R/\overline{w}$	0	Quasi-low current mode with references and digital blocks disabled, but register contents retained (MTP not reloaded): 0 = Not in standby 1 = Standby mode
RESET	[6]	$R/\overline{w}$	0	Power on reset bit – clears all register contents and MTP is reloaded.
Reserved	[5:0]	$R/\overline{w}$	000000	Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register FILTER_SETTINGS

Address	Name	POR Value(*)
0x09	FILTER_SETTINGS	0x24

Bit Assignment

7	6	5	4	3	2	1	0
DIMCODE[1:0]		DITHER_ENABLE	RCFILTER[1:0]		PWMFILTER[2:0]		

Bit Description

Field Name	Bits	Type	POR(*)	Description
DIMCODE[1:0]	[7:6]	$R/\overline{W}$	00	Brightness control method: 00 = PWM control only (default) 01 = I²C control only 10 = Input PWM x I²C control 11 = Reserved
DITHER_ENABLE	[5]	$R/\overline{W}$	1	0 = Dithering disabled 1 = Enable dithering for up to 15-bit effective resolution for linear dimming mode, up to 13-bit effective resolution for logarithmic dimming mode (default).
RCFILTER[1:0]	[4:3]	$R/\overline{W}$	00	RC filter time constant: 00 = RC filter OFF (default) 01 = 373.3 ms 10 = 185.2 ms 11 = 92.2 ms
PWMFILTER[2:0]	[2:0]	$R/\overline{W}$	100	Enables or disables the PWM filter and sets step size: 000 = OFF 001 = 2 steps 010 = 4 steps 011 = 6 steps 100 = 8 steps (default) 101 = 10 steps 110 = 12 steps 111 = 14 steps

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register VREG_IMAXTUNE

Address	Name	POR Value(*)
0x0A	VREG_IMAXTUNE	0x00

Bit Assignment

7	6	5	4	3	2	1	0
LED_VREG_CNT_INIT[3:0]				IMAXTUNE[3:0]			

Bit Description

Field Name	Bits	Type	POR(*)	Description
LED_VREG_CNT_INIT[3:0]	[7:4]	$R/\overline{W}$	0000	Initial VOUT starting target voltage: 0000 = 13.75V (default) 0001 = 16.02V 0010 = 18.29V 0011 = 20.56V 0100 = 22.83V 0101 = 25.1V 0110 = 27.37V 0111 = 29.64V 1000 = 31.91V 1001 = 34.18V 1010 = 36.45V 1011 = 38.72V 1100-1111 = Reserved
IMAXTUNE[3:0]	[3:0]	$R/\overline{W}$	0000	Sets the percentage increase of LED full-scale current set by MAX_I[4:0]: 0000 = 0.00% increase 1000 = 3.84% increase 0001 = 0.52% increase 1001 = 4.37% increase 0010 = 0.93% increase 1010 = 4.77% increase 0011 = 1.45% increase 1011 = 5.30% increase 0100 = 1.86% increase 1100 = 5.70% increase 0101 = 2.38% increase 1101 = 6.23% increase 0110 = 2.79% increase 1110 = 6.63% increase 0111 = 3.31% increase 1111 = 7.60% increase

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG_CP(2)

Address	Name	POR Value(1)
0x0B	CONFIG_CP	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved				CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1:0]	

Bit Description

Field Name	Bits	Type	POR(1)	Description
Reserved	[7:4]	$R/\overline{w}$	0000	Reserved
CP_FREQ_TRAN	[3]	$R/\overline{w}$	0	0 = Charge pump frequency changes at 75% and 50% LED brightness automatically. 1 = Charge pump frequency changes at 50% LED brightness only, and as a function of CP_FREQ_DIV[0].
SEL_CP_FREQ	[2]	$R/\overline{w}$	0	When CP_FREQ_TRAN=0: 0 = Charge pump frequency changes at 75% and 50% LED brightness automatically 1 = Charge pump is independent of LED brightness and selected by CP_FREQ_DIV[0] When CP_FREQ_TRAN=1: SEL_CP_FREQ bit is don't care.
CP_FREQ_DIV[1:0]	[1:0]	$R/\overline{w}$	00	When CP_FREQ_TRAN=0, SEL_CP_FREQ=1: 00 = 1/2 01 = 1/4 10 = 1/8 11 = 1/8 When CP_FREQ_TRAN=1: CP_FREQ_DIV[0] = 0 the charge pump frequency changes between 1/2 (≥50% LED brightness) and 1/4 (<50% LED brightness). CP_FREQ_DIV[0] = 1 the charge pump frequency changes between 1/4 (≥50% LED brightness) and 1/8 (<50% LED brightness).

Notes:

1. The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.
2. See the Charge Pump Switching Frequency Section for detailed operation description.

Register CHKSUM0

Address	Name
0x0C	CHKSUM0

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM0[7:0]							

Bit Description

Field Name	Bits	Type	Description
CHKSUM0[7:0]	[7:0]	R	Lower eight bits of the 16-bit register checksum for registers 0x00–0x0B. If incorrect, the MTP values are still loaded if the internal factory checksum is correct. After each MTP write, the CHKSUM0 register value is updated after toggling EN pin or cycling VCC.

Register CHKSUM1

Address	Name
0x0D	CHKSUM1

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM1[7:0]							

Bit Description

Field Name	Bits	Type	Description
CHKSUM1[7:0]	[7:0]	R	Upper 8 bits of the 16-bit register checksum for registers 0x00 to 0x0B. If incorrect, the MTP values are still loaded if the internal factory checksum is correct. After each MTP write, the CHKSUM1 register value is updated after toggling EN pin or cycling VCC.

Register STATUS1

Address	Name	POR Value(*)
0x0E	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_TIMEOUT	LED_SHORT

Bit Description

Field Name	Bits	Type	POR(*)	Description
BST_ILIM_SEC	[7]	R	0	Status bit to flag a secondary current limit: 0 = No error 1 = Boost current exceeded secondary current limit
VOUT_OVP	[6]	R	0	Status bit to flag an output over-voltage condition: 0 = No error 1 = Output over-voltage
VX_OV	[5]	R	0	Status bit to flag a VX over-voltage condition: 0 = No error 1 = VX voltage is above over-voltage threshold
VX_UV	[4]	R	0	Status bit to flag a VX under-voltage condition: 0 = No error 1 = VX voltage is below under-voltage threshold
DISC_OCP	[3]	R	0	Status bit to flag a disconnect switch over-current event: 0 = No error 1 = Disconnect switch exceeded over-current threshold, or VOUT is shorted to ground
TSD	[2]	R	0	Status bit to flag a thermal shutdown condition: 0 = No error 1 = Part has exceeded thermal shutdown threshold
SS_TIMEOUT	[1]	R	0	Status bit to flag a soft start timeout condition: 0 = No error 1 = Soft start has not completed before the timeout event
LED_SHORT	[0]	R	0	Status bit to flag an LED shorted-string fault: 0 = No error 1 = An LED shorted-string event occurred on one or more enabled strings

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register STATUS2

Address	Name	POR Value(*)
0x0F	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
MTP_WRITE_CMD[4:0]					MTP_WRITE_DNE	CRCOK	LED_OPEN

Bit Description

Field Name	Bits	Type	POR(*)	Description
MTP_WRITE_CMD[4:0]	[7:3]	$R/\overline{W}$	00000	Writing 10010 to these register bits automatically initiates an MTP programming cycle to register 0x00–0x0B. At the end of programming, this register is automatically cleared, and the MTP_WRITE_DNE read-only status bit shows '1'.
MTP_WRITE_DNE	[2]	R	0	Status bit indicating the completion of MTP programming for registers 0x00–0x0B. Clears upon read.
CRCOK	[1]	R	0	Status bit indicating that the CHECKSUM for registers 0x00–0x0B is good.
LED_OPEN	[0]	R	0	Status bit to flag an open or grounded condition on any LED pin: 0 = No error 1 = One or more LED strings is grounded open

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Application Schematic

Figure 44 shows the PE23108 detailed application schematic.

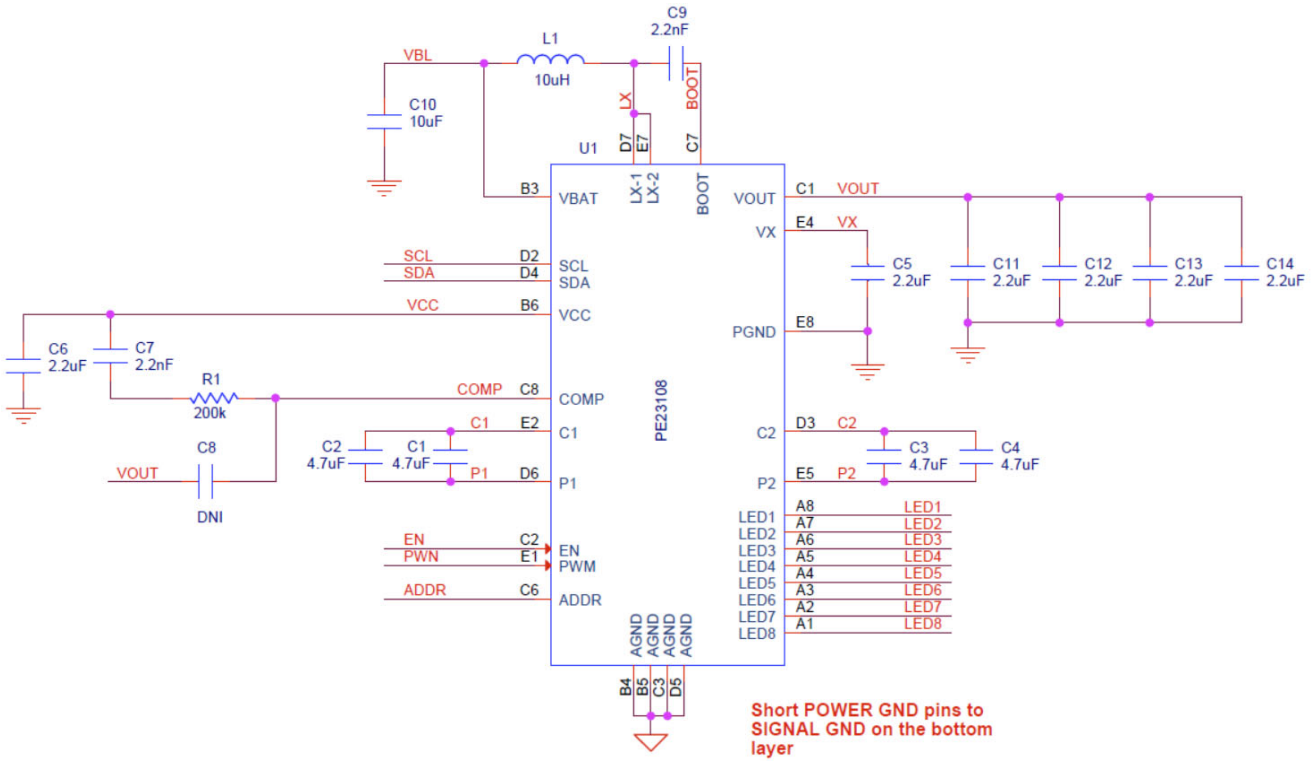


Figure 44. PE23108 Application Schematic

Application Circuit Part List

Table 18 lists the recommended part numbers.

Table 18. Recommended Parts[1]

Component	Value	Part Size	Mfg. Part Number
C1, C2, C3, C4 [2]	4.7 µF 35V X5R or better	0603	GRM188R6YA475KE15D
C5, C6	2.2 µF 25V X5R or better	0402	GRM155C81E225KE11D
C7 [4], C9	2.2 nF 50V X5R or better	0402	GRM155R71H222KA01D
C8 [4]	DNI	0402	–
C10 [3]	10 µF 25V X5R or better	0603	GRM188R61E106MA73J
C11, C12, C13, C14 [6]	2.2 µF 50V X5R or better	0603	GRM188R61H225ME11D
L1 [5]	10 µH	3.2 mm x 2.5 mm x 1.2 mm	DFE322512F-100M
R1 [4]	200 kΩ	0201	–

Notes:

1. Components in this part list are optimized for 8P12S or higher applications. For an optimized selection based on your application, contact pSemi.
2. Quantity and value are based on effective capacitance per applications. pSemi recommends a total of >0.7-µF efficiency capacitance on the C1 and C2 pins at the bias voltage.
3. Value might require an adjustment based on proximity of the input source to eliminate input voltage ringing.
4. For the general selection, see Switching Converter Compensation on page 27. For an optimized selection based on your application, contact pSemi.
5. See also recommended inductor values below for varying operating conditions.
6. Value might require an adjustment based on loading, boost switching frequency, and inductor selection to reduce output voltage ripple.

Component Selection

pSemi recommends that PE23108 customers adhere closely to the parts selected for the Application Circuit Part List in Table 18. Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. If you want to deviate from these recommended components, contact pSemi for guidance.

Efficiency Optimization

The PE23108 is designed specifically to address 2-cell and 3-cell narrow-voltage DC (NVDC) platforms, and for a wide range of LED configurations. The two-stage architecture relies less on the inductor for power and voltage conversion; therefore, reduction in the physical size of the inductor has less impact on the overall conversion efficiency compared with traditional single stage architectures. This enables the use of low profile, small footprint and low-cost chip inductors versus wire-wound inductors used by traditional LED boost drivers.

Capacitor Selection

If, due to component availability, size, second-source requirement, or other reasons that the Application Circuit Part List in Table 18 cannot be followed, use the following guidelines to select the proper PE23108 capacitors.

Charge Pump Capacitors (C1 and C2)

The effective capacitance of the capacitors used for C1 and C2 must have a minimum value of 0.7 µF, and the ideal value is 1 µF. The effective capacitance must match closely between charge pump capacitors; therefore, the same capacitor cannot be used for both the first and second charge pump stages. For example, with VOUT at 40V, 20V is applied across the charge pump capacitors C1 and C2. This wide capacitance difference between C1 and C2 or lower capacitance value can lower efficiency.

If a single capacitor cannot meet the effective capacitor requirement, use two or more capacitors in parallel together to meet the effective capacitor requirement.

VX Capacitor

The VX boost convertor output capacitor must have an effective capacitance between 0.1 µF and 0.3 µF. VX voltage is approximately VOUT/2.

VCC Capacitor

The VCC must have a minimum effective capacitance of 0.5 µF. The typical VCC input voltage is 3.3V with a maximum input voltage of 5.5V.

VOUT Capacitor

The VOUT LED output voltage capacitor must have an effective capacitance of 1 µF or higher.

Layout Example

Figure 45–Figure 48 show a Type-III PCB layout example using a four-layer board. The trace width and spacing is 0.1 mm/0.1 mm. The size for the vias is a 0.2-mm hole and a 0.5-mm pad.

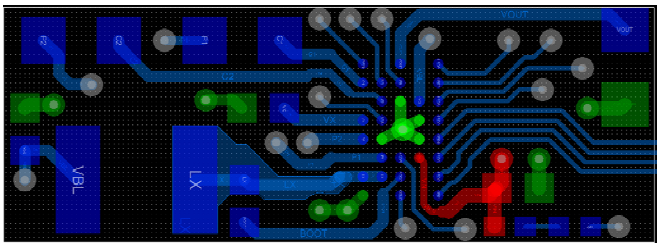


Figure 45. Top Layer

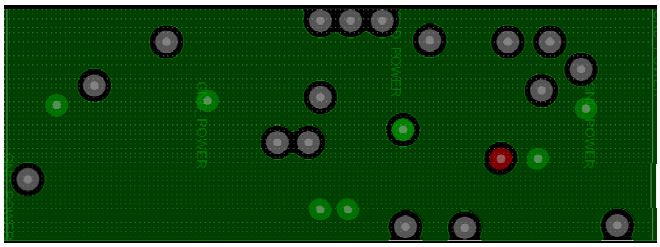


Figure 46. Layer 2

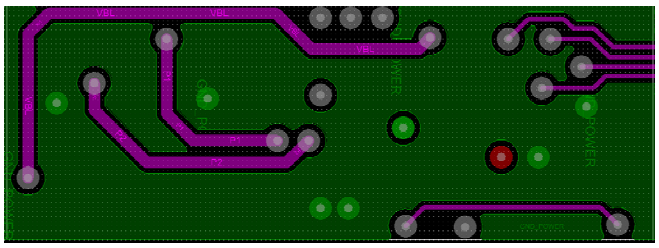


Figure 47. Layer 3

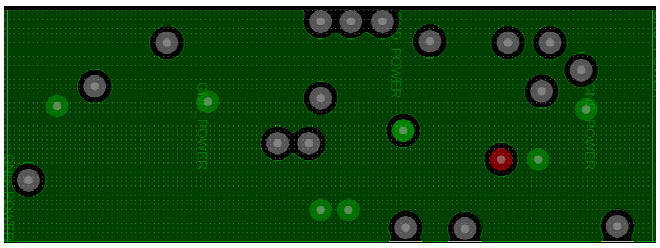


Figure 48. Bottom Layer

Packaging Information

This section includes the following packaging data:

- Moisture sensitivity level (MSL)
- Package drawing
- PCB Land Design Guidelines
- Package marking
- Tape-and-reel information

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE23108 in the 3.445 mm x 2.095 mm WLCSP package is MSL1.

Package Drawing

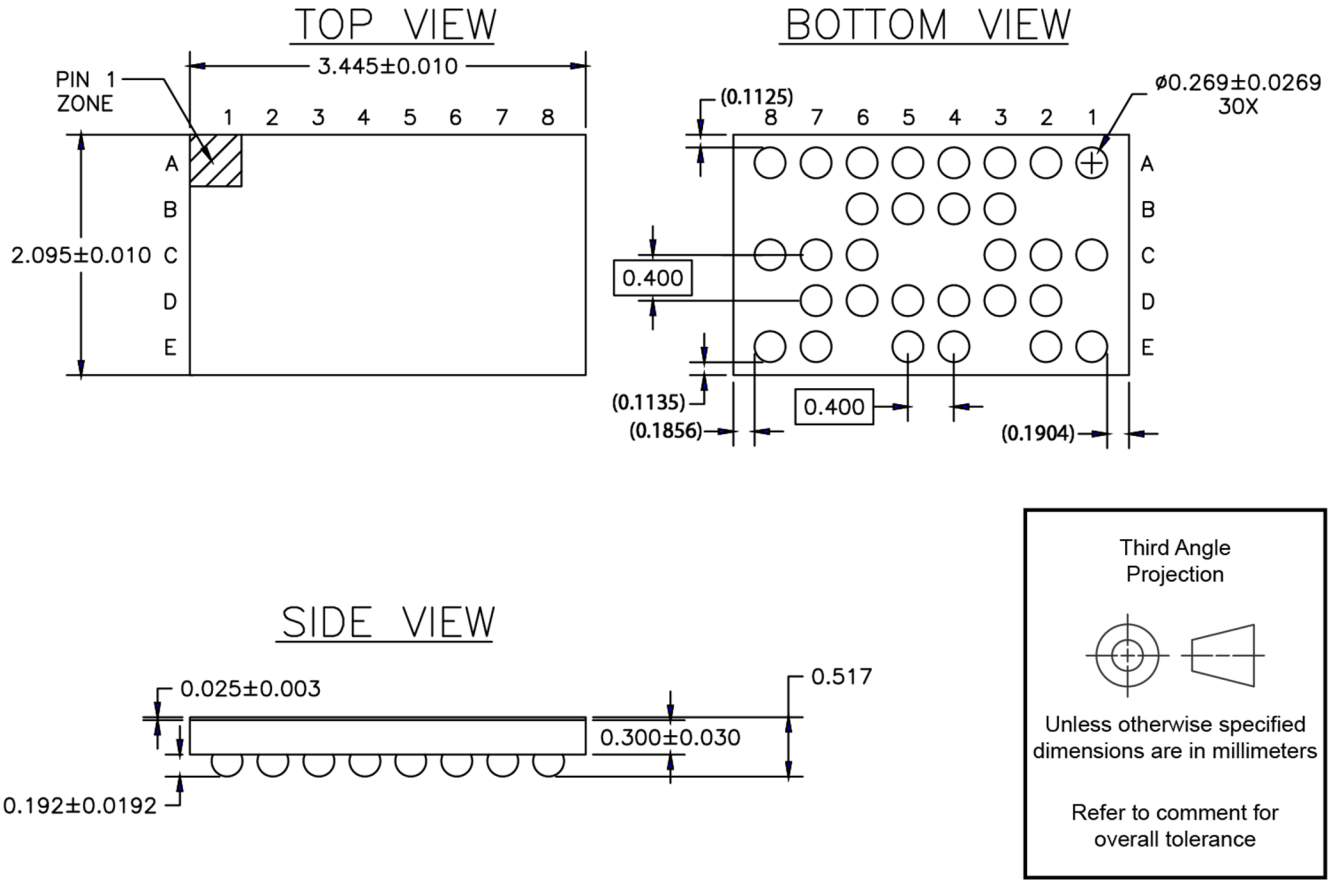


Figure 49. 3.445 mm x 2.095 mm WLCSP Package Mechanical Drawing

PCB Land Design Guidelines

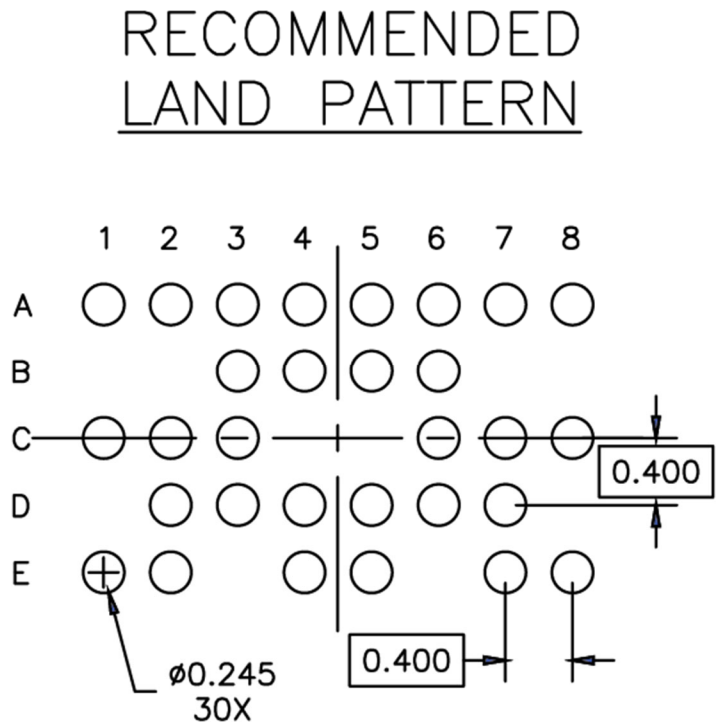
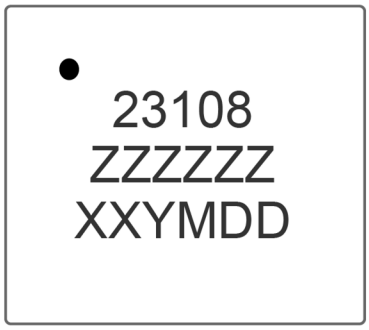


Figure 50. PE23108 Recommended PCB Footprint

The solder mask openings must be larger with a typical 0.05-mm ring all around each of the perimeter pads. The center pad is solder mask defined, with the dimensions as shown above. The copper for the center pad can be extended beyond the solder mask defined pad as needed to optimize the thermal performance. Put as many thermal vias as possible in this copper. There must be no PCB Layer 1 copper under any package exposed metal, except for the center pad. All the exposed metal is dimensioned in the package mechanical details.

Top-Marking Specification



● = Pin 1 indicator
23108 = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
XX = Supplier code (maximum two characters)
Y = Last digit of assembly year (2022 = 2)
M = Assembly month (1,2,3...9,O,N,D)
DD = Assembly day (01,02,03...31)

Figure 51. 3.445 mm x 2.095 mm WLCSP Package Marking Specifications

Tape and Reel Specification

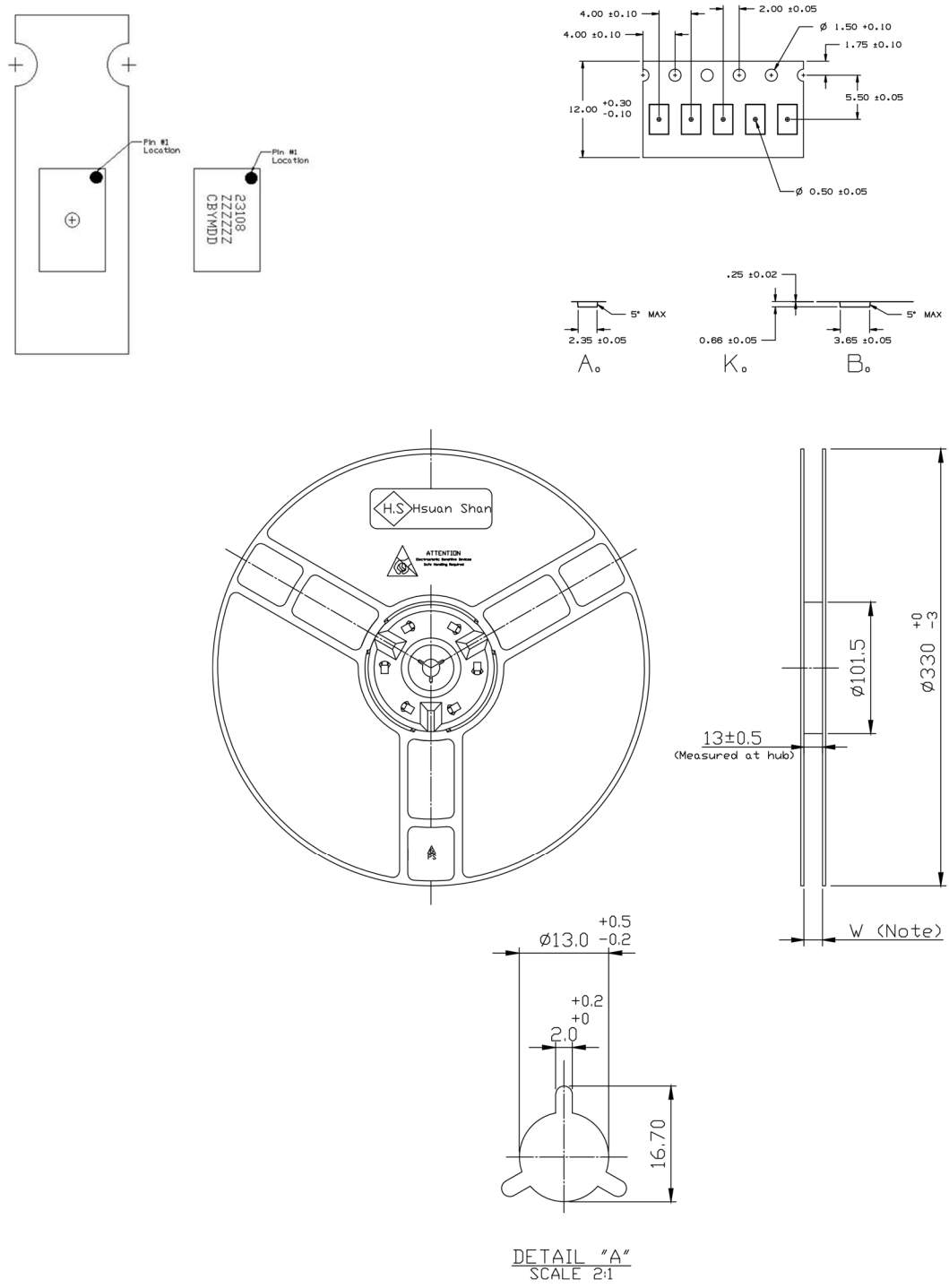


Figure 52. 3.445 mm x 2.095 mm WLCSP Tape and Reel Specifications

Ordering Information

Table 19 lists the PE23108 order codes and shipping methods.

Table 19. PE23108 Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
PE23108A-R	High-Efficiency LED Backlight Driver	3.445 mm x 2.095 mm WLCSP on tape and reel	5000 units/large tape and reel
PE23108A-V	High-Efficiency LED Backlight Driver	3.445 mm x 2.095 mm WLCSP on tape and reel	250 units/small tape and reel
PE23108A-G	High-Efficiency LED Backlight Driver	3.445 mm x 2.095 mm WLCSP	10 units/sample waffle tray

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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