Product Specification

PE4251

UltraCMOS® SPDT RF Switch
10–4000 MHz, Absorptive

Features

- HaRP™ technology enhanced
- Low insertion loss: 0.60 dB @ 1000 MHz
- High isolation: 62 dB @ 1000 MHz
- P1dB typical: +30.5 dBm
- IIP3 typical: +59 dBm
- Fast switching time: 150 ns
- Flexible supply voltage: 3.3V ±10% or 5.0V ±10% supply (see *Table 3*)
- Excellent ESD protection: 4000V HBM
- No blocking capacitors required
- Single pin or complementary control inputs

Product Description

The PE4251 is a HaRP™ technology-enhanced absorptive single-pole, double-throw (SPDT) RF switch for use in general switching applications and mobile infrastructure. This device offers a flexible supply voltage of 3.3V or 5V, single-pin or complementary-pin control inputs, and 4000V ESD tolerance. It presents a simple alternative solution to pin diode and mechanical relay switches.

The pSemi HaRP™ technology enhancements deliver high linearity and exceptional performance. It is an innovative feature of the UltraCMOS® process.

Figure 1. Functional Diagram

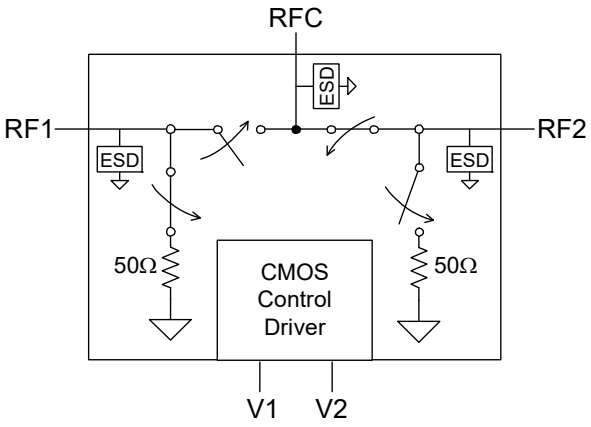


Figure 2. Package Type

8-lead MSOP with exposed paddle

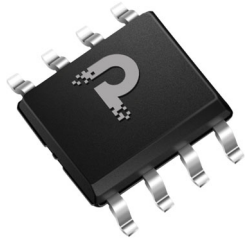


Table 1A. Target Electrical Specifications, Temp = +25 °C, V_{DD} = 3.3V or 5.0V

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency[1]	–	10	–	4000	MHz
Insertion loss (RF1/RF2)	10 MHz	–	0.55	0.60	dB
	1000 MHz	–	0.60	0.70	dB
	2000 MHz	–	0.75	0.85	dB
	3000 MHz	–	0.75	0.90	dB
	4000 MHz	–	1.0		dB
Isolation (RFC to RF1/RF2)	1000 MHz	61	62	–	dB
	2000 MHz	51	53	–	dB
	3000 MHz	42	43	–	dB
	4000 MHz	–	37	–	dB
Return loss	1000 MHz	–	26	–	dB
	2000 MHz	–	23	–	dB
	3000 MHz	–	22	–	dB
	4000 MHz	–	19	–	dB
Input 1dB compression[2]	50–4000 MHz	–	30.5	–	dBm
Input IP3	50–4000 MHz, +18 dBm per tone, 5 MHz spacing	–	59	–	dBm
Switching time	50% CTRL to 10/90% RF	–	150	300	ns

Notes: 1. Device linearity can start to degrade below 10 MHz.
2. Absolute maximum rating of P_{IN} = 27 dBm.

Table 1B. Target Electrical Specifications, Temp = +125 °C, V_{DD} = 3.3V or 5.0V

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency	–	50	–	4000	MHz
Insertion loss (RF1/RF2)	50 MHz	–	0.65	–	dB
	1000 MHz	–	0.75	–	dB
	2000 MHz	–	0.90	–	dB
	3000 MHz	–	1.05	–	dB
	4000 MHz	–	1.2	–	dB
Isolation (RFC to RF1/RF2)	1000 MHz	–	62	–	dB
	2000 MHz	–	52	–	dB
	3000 MHz	–	43	–	dB
	4000 MHz	–	36	–	dB
Return loss	1000 MHz	–	24	–	dB
	2000 MHz	–	23	–	dB
	3000 MHz	–	19	–	dB
	4000 MHz	–	18	–	dB
Input 1dB compression*	50–4000 MHz	–	30.5	–	dBm
Input IP3	50–4000 MHz, +18 dBm per tone, 5 MHz spacing	–	57	–	dBm
Switching time	50% CTRL to 10/90% RF	–	200	–	ns

Note: * Absolute maximum rating of P_{IN} = 22 dBm.

Figure 3. Pin Configuration (Top View)

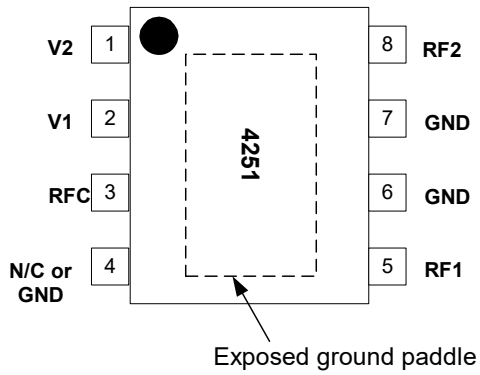


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	V2	This pin supports two interface options: • Single-pin control mode: A nominal 3V supply connection is required. • Complementary-pin control mode: A complementary CMOS control signal to V1 is supplied to this pin.
2	V1	Switch control input, CMOS logic level
3	RFC	RF common port*
4	N/C or GND	No connect or ground
5	RF1	RF1 port*
6, 7	GND	Ground connections. For the best performance, ensure that the traces are physically short and connected to the ground plane.
8	RF2	RF2 port*
Paddle	GND	Exposed ground paddle. Ground for proper device operation.

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} power supply voltage*	3.0 4.5	3.3 5.0	3.6 5.5	V V
I_{DD} power supply current V_{DD} = V_{CNTL}= 3.3V V_{DD} = V_{CNTL}= 5.0V	 – –	 55 75	 60 80	 µA µA
Control voltage high	0.8 × V_{DD}	–	–	V
Control voltage low	–	–	0.2 × V_{DD}	V
P_{IN} RF input power (50Ω) 10 MHz–4 GHz, +85 °C 50 MHz–4 GHz, +125 °C	 – –	 – –	 27 22	 dBm dBm
T_{OP} operating temperature range	–40	+25	+125	°C
T_{ST} storage temperature range	–65	+25	+150	°C

Note: * Customer must choose either the 3.3V or the 5.0V power supply range.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	3	5.5	V
V_I	Voltage on any control input	–0.3	5.5	V
T_{ST}	Storage temperature range	–65	+150	°C
P_{IN}	RF input power (50Ω) 10 MHz–4 GHz, +85 °C 50 MHz–4 GHz, +125 °C	 – –	 27 22	 dBm dBm
V_{ESD}	ESD voltage, HBM ESD voltage, MM (machine model)	 –	4000 250	V V

Note: 1. Human body model (MIL_STD 883 Method 3015).
2. Machine model (JEDEC JESD22-A115).

Exceeding the absolute maximum ratings could cause permanent damage. Restrict operation to the limits in the Operating Ranges table. Operation between the operating range maximum and the absolute maximum for extended periods can reduce reliability.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the specified rating.

Switching Frequency

The PE4251 has a maximum 25-kHz switching rate.

Moisture Sensitivity Level

The moisture sensitivity level (MSL) rating for the PE4251 in the 8-lead MSOP package is MSL1.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 1 (V2) = V_{DD} Pin 2 (V1) = High	RFC to RF1
Pin 1 (V2) = V_{DD} Pin 2 (V1) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 1 (V2) = Low Pin 2 (V1) = High	RFC to RF1
Pin 1 (V2) = High Pin 2 (V1) = Low	RFC to RF2

Control Logic Input

The PE4251 is a versatile RF CMOS switch that supports two operating control modes: single-pin control mode and complementary-pin control mode:

- Single-pin control mode: The switch operates with a single control pin (pin 2) supporting a 3.3V or 5.0V CMOS logic input, and requires a dedicated 3.3V or 5.0V power supply connection (pin 1). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- Complementary-pin control mode: The switch operates using complementary control pins V1 and V2 (pins 2 and 1), that can be directly driven by 3.3V or 5.0V CMOS logic or a suitable microprocessor I/O port. This enables the PE4251 to operate in positive control voltage mode within the PE4251 operating limits.

Evaluation Kit

The SPDT switch evaluation kit board was designed to ease customer evaluation of the PE4251 SPDT switch. The RF common port is connected through a 50Ω transmission line to the bottom SMA connector, J3. Port 1 and Port 2 are connected through 50Ω transmission lines to two SMA connectors on either side of the board, J4 and J2. A through transmission line connects SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.0322." The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.033," trace gaps of 0.010," dielectric thickness of 0.028," copper thickness of 0.0021," and ε_r of 4.3.

J1 provides a means for controlling the DC inputs to the device. The second-to-bottom lower right pin (J1–3) is connected to the device V1 input. The second-to-top upper right pin (J1–7) is connected to the device V2 input. Footprints for decoupling capacitors are provided on both V1 and V2 traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 4. Evaluation Board Layouts

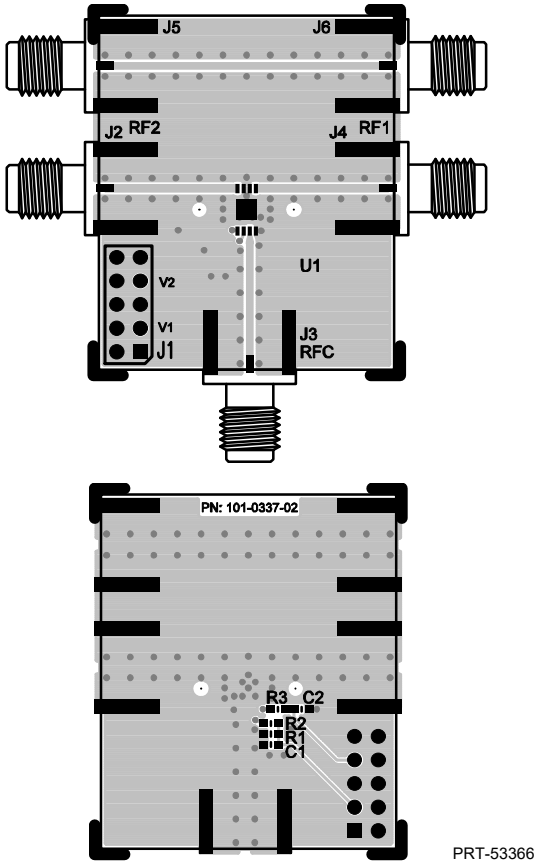
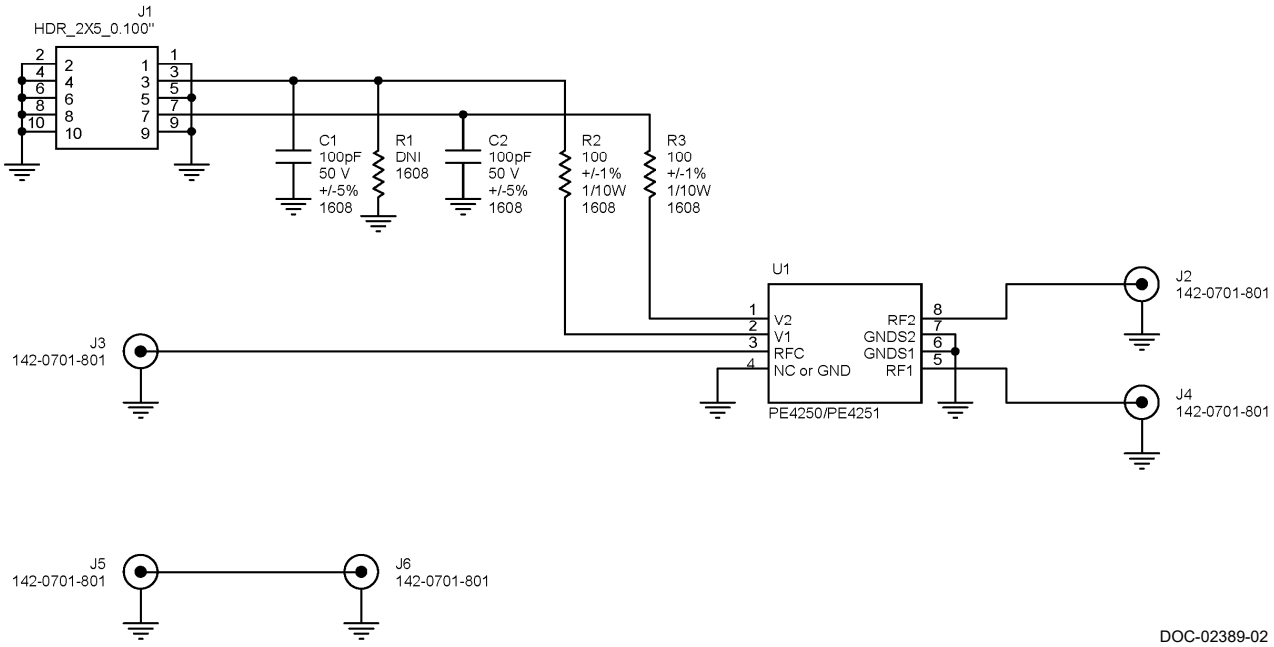


Figure 5. Evaluation Board Schematic



Typical Performance Data

Figure 6. Insertion Loss: RFC–RF @ +25 °C

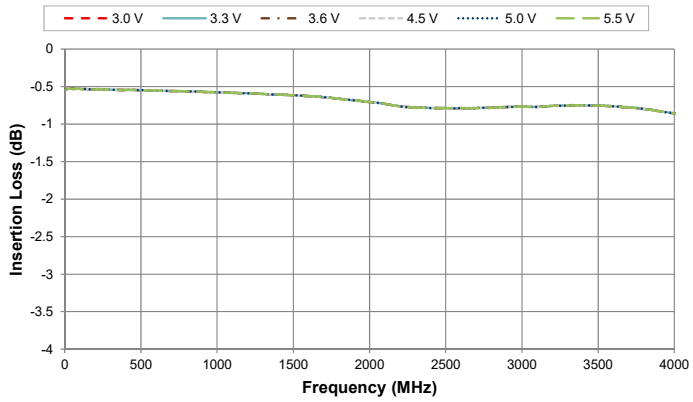


Figure 7. Insertion Loss: RFC–RF @ 3.3V

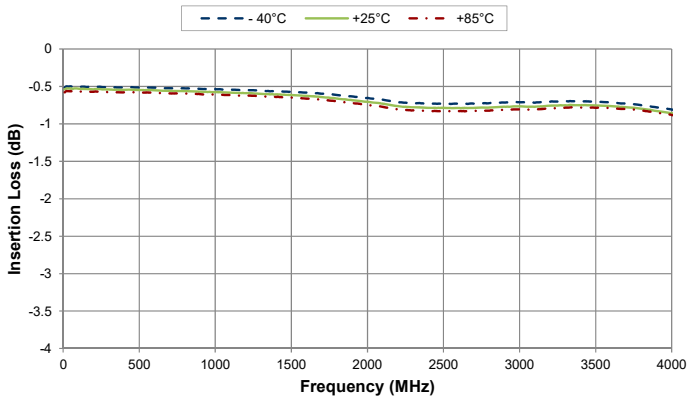


Figure 8. Isolation: RFC–RF @ +25 °C

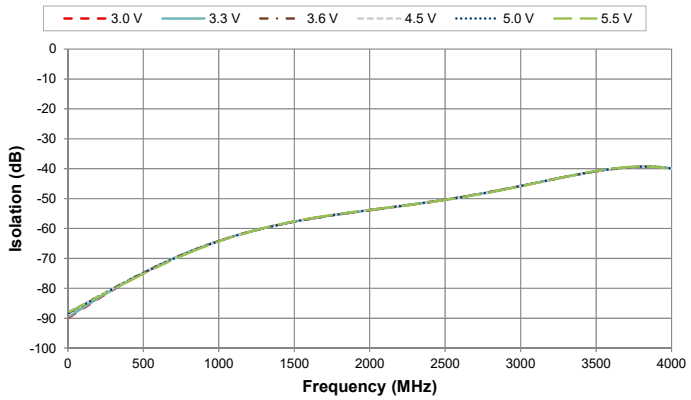


Figure 9. Isolation: RFC–RF @ 3.3V

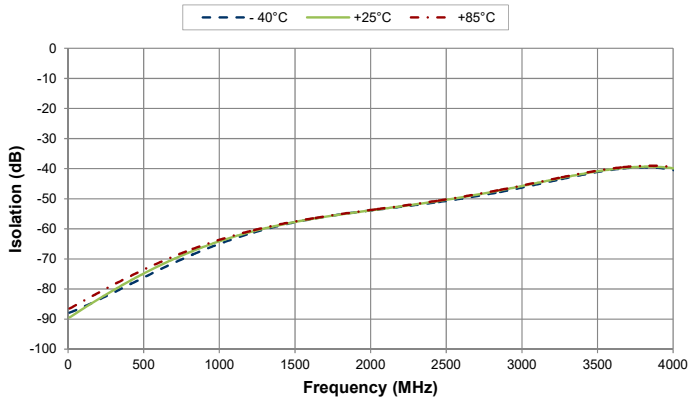


Figure 10. Return Loss at Active Port @ +25 °C

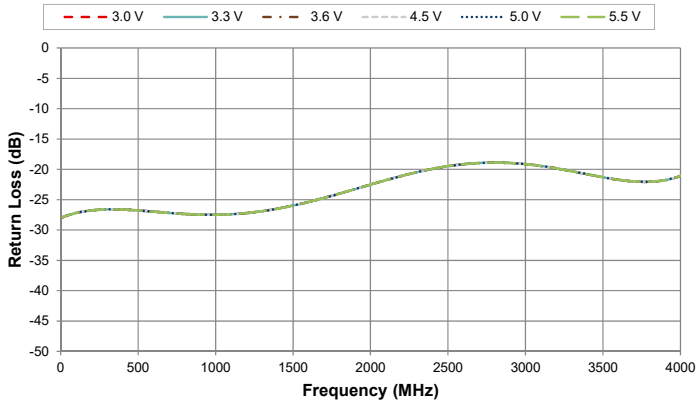


Figure 11. Return Loss at Active Port @ 3.3V

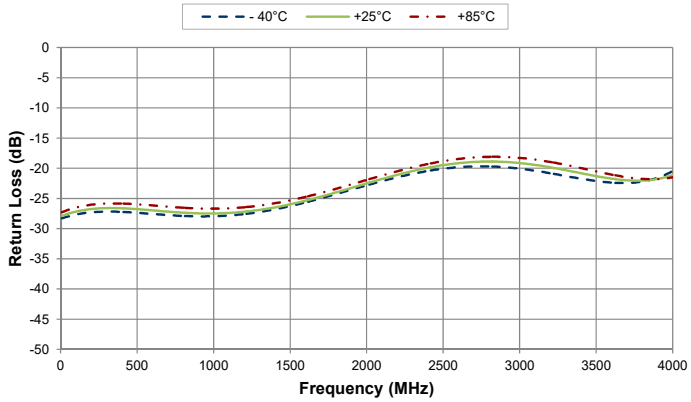


Figure 12. Package Drawing
8-lead MSOP

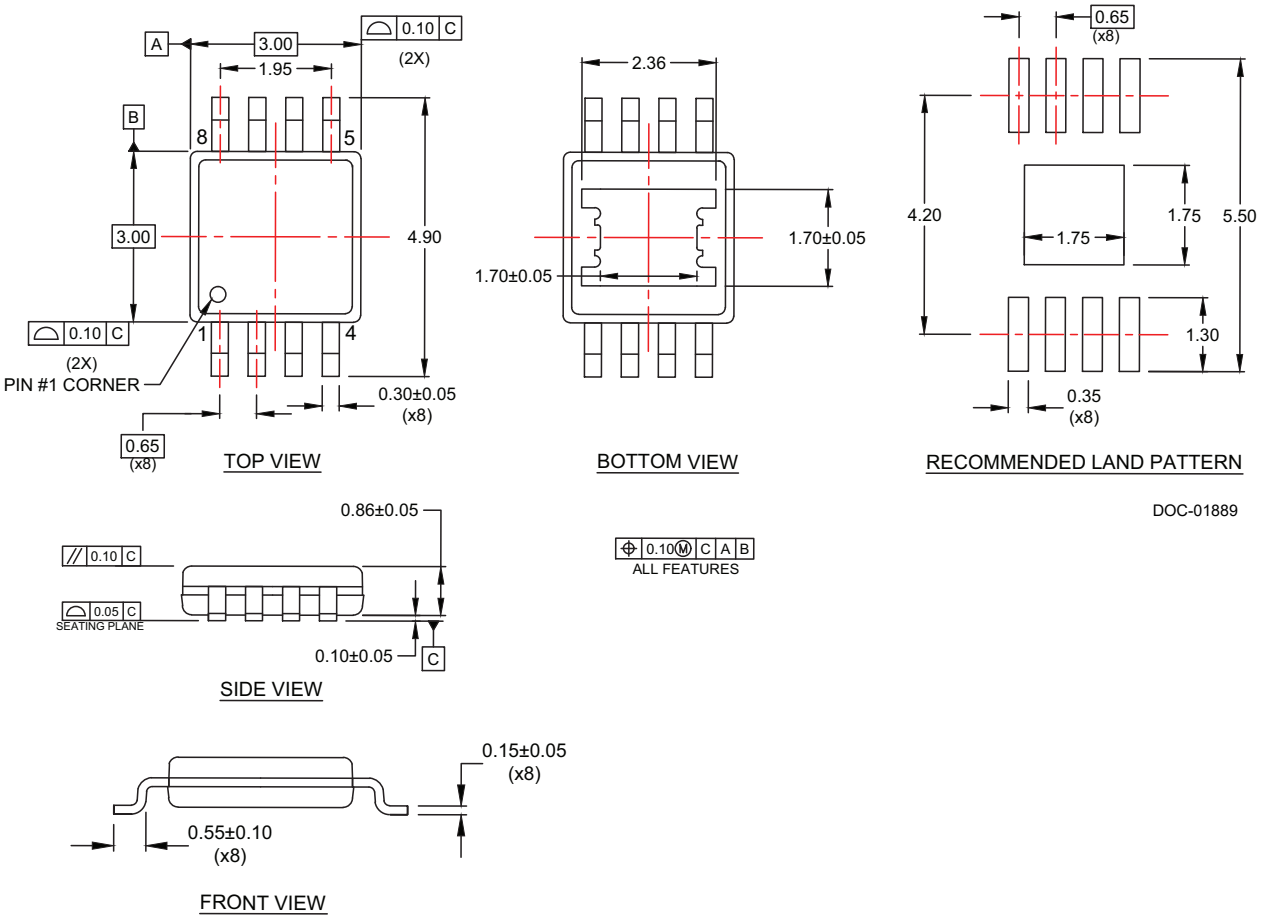
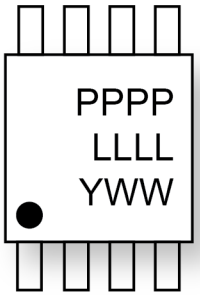
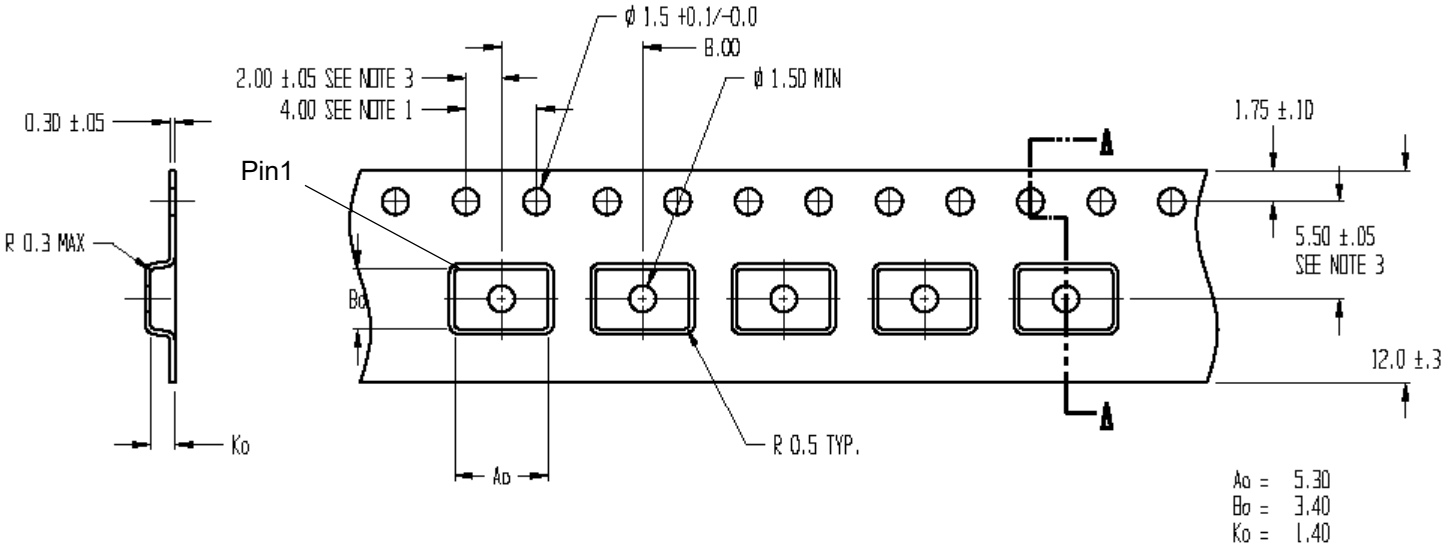


Figure 13. Top-marking Specification



● = Pin 1 indicator
PPPP = Product part number (4251 for PE4251)
LLLL = Last four digits of the assembly lot number
YWW = Date code, last digit of the year, and work week

Figure 14. Tape and Reel Specifications
8-lead MSOP with exposed paddle



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
EK4251-01	PE4251 Evaluation kit	Evaluation kit	1/box
PE4251MLI-Z	PE4251 SPDT RF switch	Green 8-lead MSOP, exposed paddle	2000 units/tape and reel

Sales and Contact Information

For sales and contact information please visit www.psemi.com.