Product Specification

PE613050

UltraCMOS® SP4T Tuning Control Switch, 5–3000 MHz

Product Description

The PE613050 is an SP4T tuning control switch based on pSemi's UltraCMOS® technology. This highly versatile switch supports a wide variety of tuning circuit topologies with emphasis on impedance matching and aperture tuning applications. PE613050 features low on-resistance and insertion loss across key cellular frequency bands from 5 to 3000 MHz.

PE613050 offers high RF power handling and ruggedness, while meeting challenging harmonic and linearity requirements enabled by pSemi's HaRP™ technology. With two-pin low voltage CMOS control, all decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

UltraCMOS tuning devices feature ease of use while delivering superior RF performance. With built-in bias voltage generation and ESD protection, tuning control switches provide a monolithically integrated tuning solution for demanding RF applications.

Features

- Open reflective architecture
- Low on-resistance of 1.6Ω
- Low insertion loss
  - 0.25 dB @ 900 MHz
  - 0.40 dB @ 2200 MHz
- High power handling
  - 35.1 dBm @ 900 MHz
  - 35.1 dBm @ 2200 MHz
- Wide power supply range (2.3V to 5.5V)
- High ESD tolerance of 2 kV HBM on all pins
- Applications include
  - Tunable antennas
  - Tunable matching networks
  - Bypassing applications
  - RFID readers

Figure 1. Functional Diagram

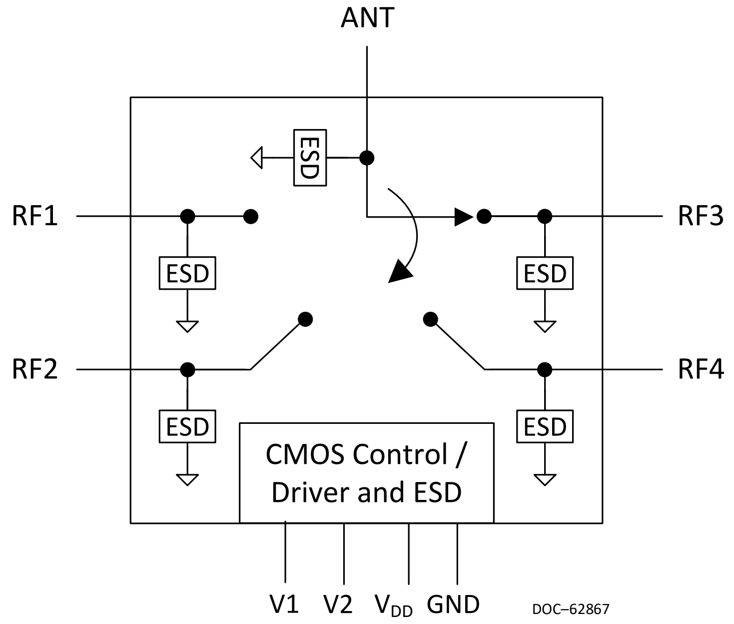


Figure 2. Package Type

12-lead 2 × 2 × 0.5 mm QFN

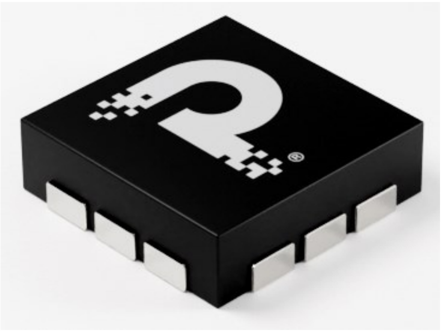


Table 1. Electrical Specifications @ 25°C, V_{DD} = 2.75V

Parameter	Condition	Min	Typ	Max	Unit
Operating Frequency		5		3000	MHz
R_{ON}	RF–ANT, ON state, DC measurement		1.6		Ω
C_{OFF}	RF–ANT, any OFF state		0.14		pF
Insertion Loss[1]	RF–ANT 5–100 MHz		0.17		dB
	RF–ANT 100–698 MHz		0.20	0.30	dB
	RF–ANT 698–960 MHz		0.25	0.35	dB
	RF–ANT 960–1710 MHz		0.35	0.45	dB
	RF–ANT 1710–2170 MHz		0.40	0.50	dB
	RF–ANT 2170–2500 MHz		0.45	0.55	dB
	RF–ANT 2500–2690 MHz		0.50	0.60	dB
Isolation[2]	RF–ANT 5–100 MHz		46		dB
	RF–ANT 100–698 MHz	26	28		dB
	RF–ANT 698–960 MHz	25	27		dB
	RF–ANT 960–1710 MHz	21	23		dB
	RF–ANT 1710–2170 MHz	19	21		dB
	RF–ANT 2170–2500 MHz	18	20		dB
	RF–ANT 2500–2690 MHz	17	19		dB
	RF–ANT 2690–3000 MHz	15	17		dB
Harmonics[3]	RF–ANT (2fo: 5 to 100 MHz; +26 dBm @ TX)		–58		dBm
	RF–ANT (3fo: 5 to 100 MHz; +26 dBm @ TX)		–87		dBm
	RF–ANT (2fo: 698 to 915 MHz; +35 dBm @ TX)		–62	–36	dBm
	RF–ANT (3fo: 698 to 915 MHz; +35 dBm @ TX)		–55	–36	dBm
	RF–ANT (2fo: 1710 to 1910 MHz; +33 dBm @ TX)		–58	–36	dBm
	RF–ANT (3fo: 1710 to 1910 MHz; +33 dBm @ TX)		–55	–36	dBm
	RF–ANT (2fo: 698 to 798 MHz; +26 dBm @ TX)		–80	–36	dBm
	RF–ANT (3fo: 698 to 798 MHz; +26 dBm @ TX)		–82	–36	dBm
	RF–ANT (2fo: 2500 to 2570 MHz; +26 dBm @ TX)		–70	–36	dBm
	RF–ANT (3fo: 2500 to 2570 MHz; +26 dBm @ TX)		–70	–36	dBm
Input IP3	5–100 MHz		80		dBm
	100–3000 MHz		72		dBm
IMD3	Bands I,II,V,VIII, +20 dBm CW @ TX freq, –15 dBm CW @ 2TX–RX freq, 50Ω, SW_{ON}		–120	–105	dBm
Switching Time	50% VCTRL to 90% RF ON or 10% RF OFF		2	5	µs
Start-up Time[3]	Time from V_{DD} within specification to all performances within specification			70	µs

Notes: 1. Tapered transmission lines on evaluation board provide optimal matching; no additional components on evaluation board required to meet specified performance. See *Figure 5* for evaluation board layout.

Figure 3. Pin Configuration (Top View)

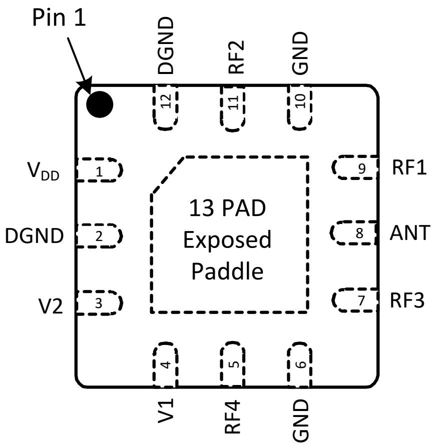


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Supply
2	DGND	Digital Ground
3	V2	Switch control input, CMOS logic level
4	V1	Switch control input, CMOS logic level
5	RF4	RF I/O
6	GND	Ground[1]
7	RF3	RF I/O
8	ANT	RF Common - Antenna
9	RF1	RF I/O
10	GND	Ground[1]
11	RF2	RF I/O
12	DGND	Digital Ground[1]
13	PAD	Exposed Paddle[2]

Notes: 1. All ground pins must be tied together (pins 6, 10, 12).
2. Recommend grounding but can be left floating.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE613050 in the 12-lead 2 × 2 mm QFN package

Table 3. Truth Table

Path	V2	V1
RF1–ANT	0	0
RF2–ANT	1	0
RF3–ANT	0	1
RF4–ANT	1	1

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Supply Voltage	2.30	2.75	5.50	V
I_{DD} Power Supply Current (V_{DD} = 2.75V, +25 °C)		140	200	µA
V_{IH} Control Voltage High	1.2	1.5	3.1	V
V_{IL} Control Voltage Low	0	0	0.5	V
Control Input Current		1	10	µA
Peak Operating RF Voltage[1,2] 5–100 MHz 100 MHz–1 GHz 1 GHz–3 GHz			 10[5] 18[3] 18[4]	 V_{PK} V_{PK} V_{PK}
T_{OP} Operating Temperature Range	−40	+25	+85	°C

Notes: 1. Between all RF ports, and from RF ports to GND.
2. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
3. RF input power of 35.1 dBm, 50Ω.
4. RF input power of 35.1 dBm, 50Ω.

Table 5. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Unit
V_{DD}	Supply Voltage	−0.3	5.5	V
V_{CTRL}	Digital Input Voltage (V1, V2)	−0.3	3.6	V
T_{ST}	Storage Temperature Range	−65	+150	°C
$V_{ESD,HBM}$	HBM ESD Voltage, All Pins*		2000	V

Note: * Human Body Model (MIL_STD 883 Method 3015.7).

Exceeding absolute maximum ratings may cause permanent damage. Operating should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Equivalent Circuit Model Description

The equivalent circuit model shown in *Figure 4* can be used to accurately model the impedance, insertion loss, and isolation of the SP4T tuning wwitch. It provides a very close correlation to measured data and can easily be used in circuit simulation programs.

Table 7 provides the mapping between the desired switch RF state (RF1 thru RF4) and the state variables (SW1 thru SW4).

The equivalent circuit model parameter values can be calculated using equations shown in *Table 6*.

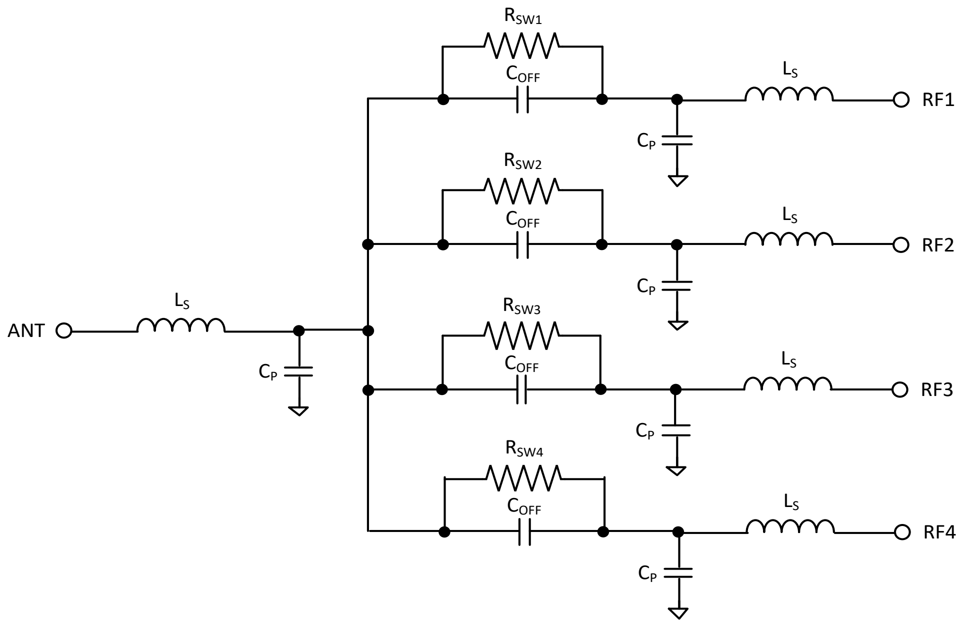
Table 6. Equivalent Circuit Model Parameters

Variable	Equation (SW=0 for OFF and SW=1 for ON)	Unit
C_P	0.25	pF
C_{OFF}	0.14	pF
R_{SW1}	If SW_1 == 1then 1.6 else 400e3	Ω
R_{SW2}	If SW_2 == 1then 1.6 else 400e3	Ω
R_{SW3}	If SW_3 == 1then 1.6 else 400e3	Ω
R_{SW4}	If SW_4 == 1then 1.6 else 400e3	Ω
L_S	0.4	nH

Table 7. Equivalent Circuit Model Variables

RF State			Variable			
Path	**V2**	**V1**	**SW1**	**SW2**	**SW3**	**SW4**
RF1–ANT	0	0	1	0	0	0
RF2–ANT	1	0	0	1	0	0
RF3–ANT	0	1	0	0	1	0
RF4–ANT	1	1	0	0	0	1

Figure 4. Equivalent Circuit Model Schematic

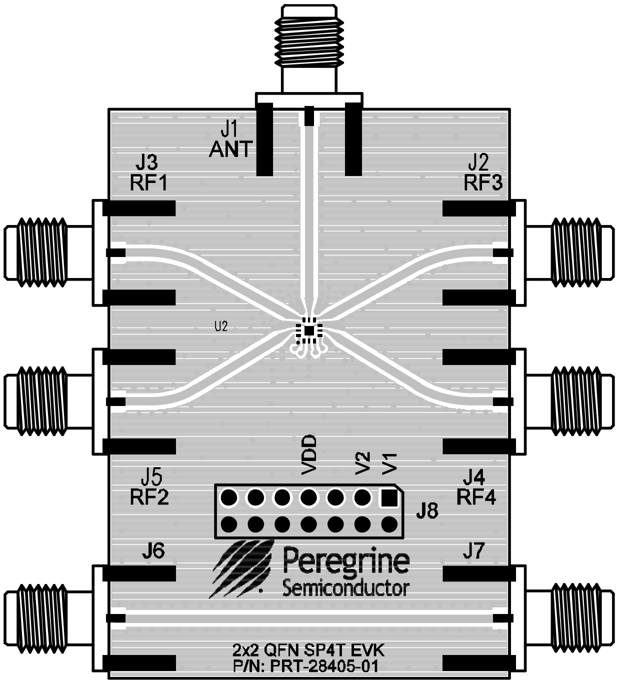


Evaluation Board

The SP4T switch evaluation board was designed to ease customer evaluation of pSemi's PE613050. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via SMA connectors J3, J5, J2 and J4, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B ($\varepsilon_r = 3.48$) and 2 inner layers of FR4 ($\varepsilon_r = 4.80$). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

Figure 5. Evaluation Board Layout



PRT-28405

Figure 6. Evaluation Board Schematic

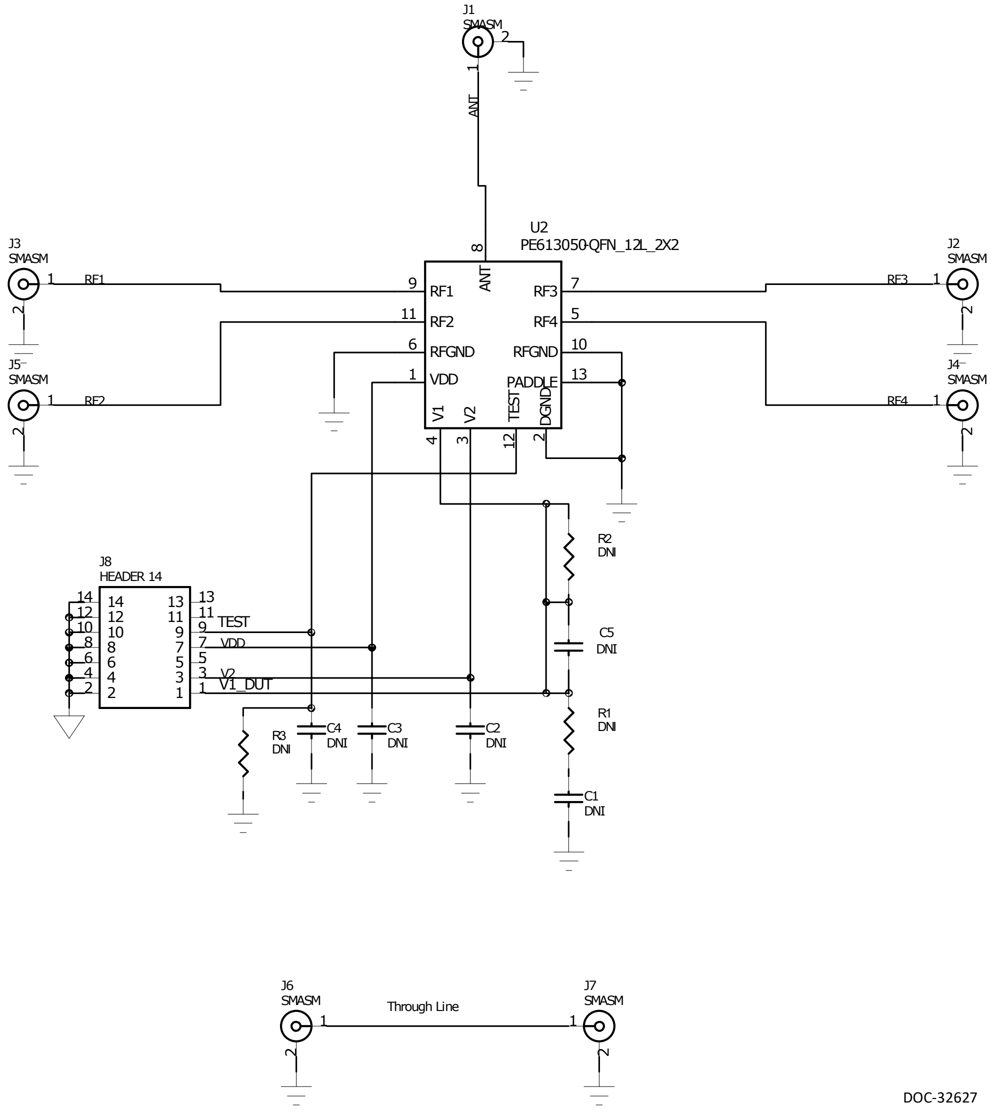
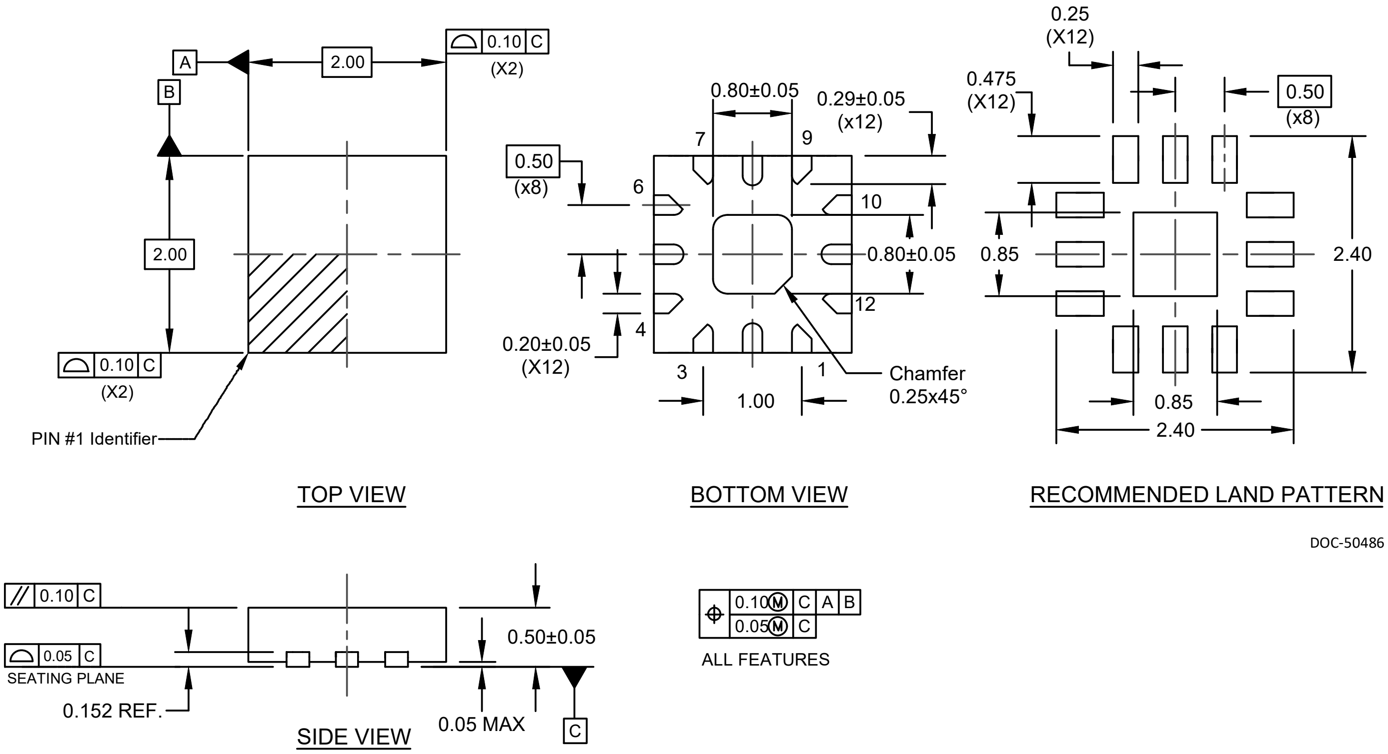


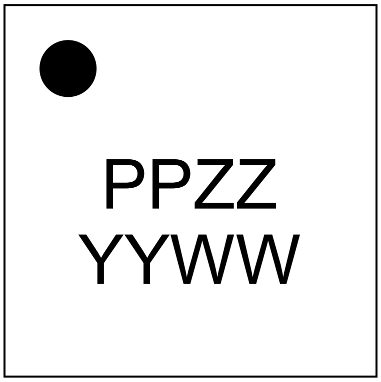
Figure 7. Package Drawing

12-lead 2 × 2 × 0.50 mm



Notes: 1. Dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M, 1994.

Figure 8. Top Marking Specifications

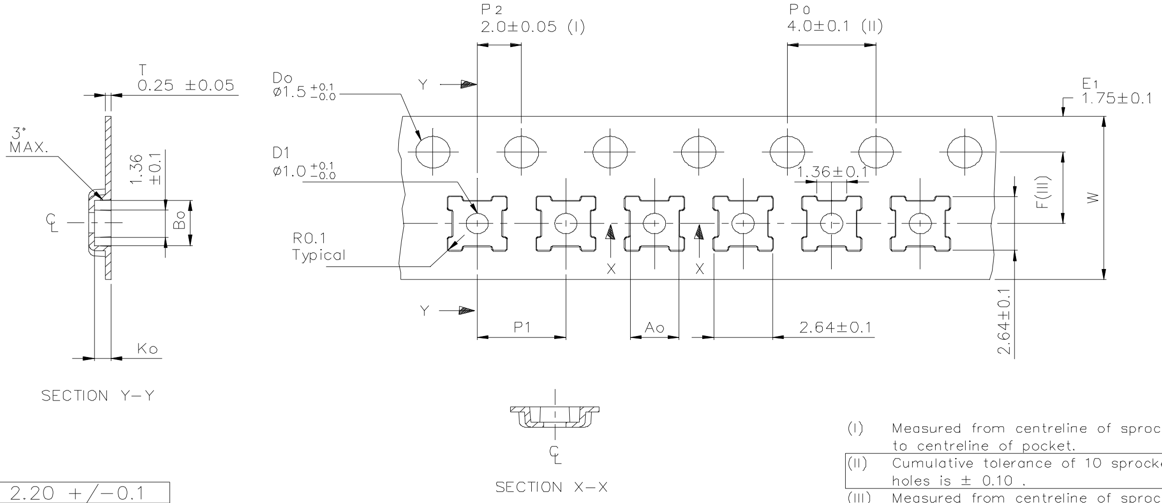


DOC-51207

Marking Spec Symbol	Package Marking	Definition
PP	DS	Part number code for PE613050
ZZ	00–ZZ	Last two characters of lot code
YY	0–9	Last two digits of year, starting from 2010 (0 for 2010, 1 for 2011, etc.)
WW	01–53	Work week

Note: (PP), the package marking specific to the PE613050, is shown in the figure instead of the standard pSemi package marking symbol (P).

Figure 9. Tape and Reel Specifications

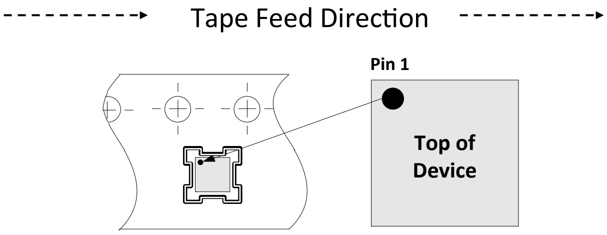


Ao	2.20 +/−0.1
Bo	2.20 +/−0.1
Ko	0.75 +/−0.1
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +/−0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.10 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

This part shall not contain any banned substance as Sony standard SS–00259

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.



Device Orientation in Tape

Table 8. Ordering Information

Order Code	Package	Description	Shipping Method
PE613050A-Z	12-lead QFN 2 × 2 × 0.50 mm	Package Part in Tape and Reel	3,000 units / T&R

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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