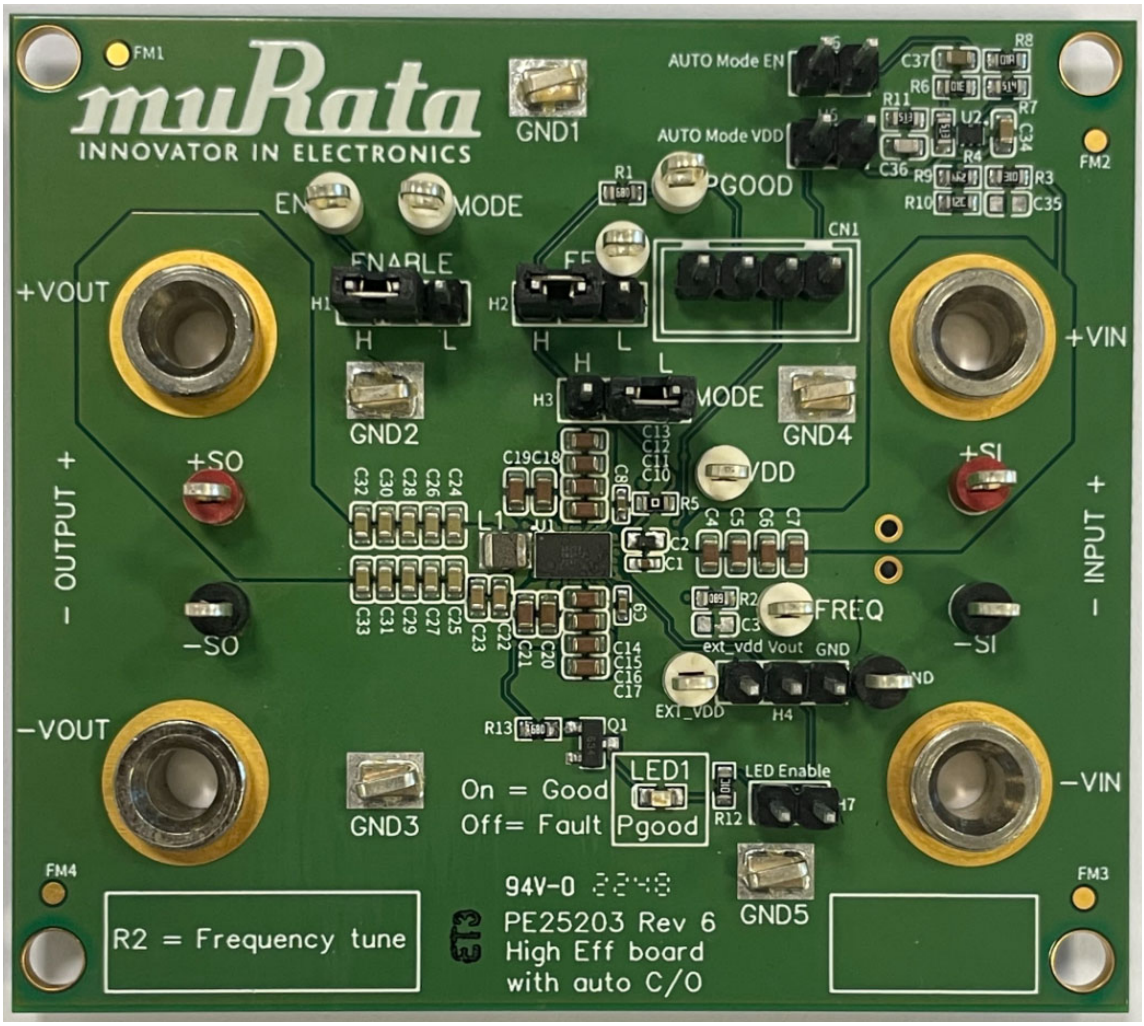
PE25203

Evaluation Kit User's Manual

Divide-by-2 and -3, 4A Charge Pump, Capacitor Divider



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Introduction

The **PE25203** is an ultra-high efficiency charge pump capacitor divider that you can configure to divide down an input voltage by two or three and deliver up to 4A output at up to 99% peak efficiency. The PE25203 supports the following input voltage ranges and is available in a WLCSP package:

- 5.7V–10V in divide-by-2 mode
- 8.4V–15V in divide-by-3 mode

The PE25203 evaluation kit (EVK) is intended and made available for evaluation and testing purposes only.

Evaluation Kit Overview

The PE25203 evaluation kit (EVK) is a hardware platform that allows you to easily test the charge pump converter. The PE25203 EVK can be operated in different modes. Table 1 lists the electrical parameters of the PE25203 EVK. For more information, see the *PE25203 Data Sheet*.

Table 1. PE25203 EVK Electrical Parameters

Reference	Description	Condition	Min	Max	Unit
V_{IN}+	Input voltage in divide-by-3 mode	–	8.4	15	V
V_{IN}+	Input voltage in divide-by-2 mode	–	5.7	10	V
I_{OUT}	Output current	–	4	–	A
+V_{EXT}	V_{DD} external	–	3.4	5	V
F_{SW}	Switching frequency	Fixed frequency	200	1000	kHz
		Cycle skip	3.3	1000	kHz
–	Efficiency	200 kHz	–	99	%

Document Overview

This *PE25203 Evaluation Kit (EVK) User's Manual* includes information about the hardware required to control and evaluate the charge pump converter functionality.

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EVK Contents and Requirements

Kit Contents

Table 2 lists the hardware required for evaluation.

Table 2. EVK Contents

Quantity	Description	Part Number
1	PE25203 DC-DC converter evaluation board assembly	EK25203-01

Hardware Requirements

To evaluate the performance of the evaluation board, the following equipment is required:

- Bench DC power supply
- DC load (power resistors or an electrical load)
- Four high-accuracy digital multimeters
- Four-channel oscilloscope with probes (optional to view waveforms)
- DC test leads

Warning: The PE25203 EVK contains components that could be damaged by exposure to voltages higher than the maximum specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals, or to signal inputs and outputs.

Before you connect the EVK to the source power supply, verify that the power supply is off. Connecting the EVK to a live power supply could induce failures.

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Quick Start Guide

The evaluation board is designed to ease your evaluation of the PE25203. This section guides you through the hardware configuration and the start-up procedures.

Evaluation Board Overview

The evaluation board contains the following:

- Input/output terminals
- PCB headers
- Sense points

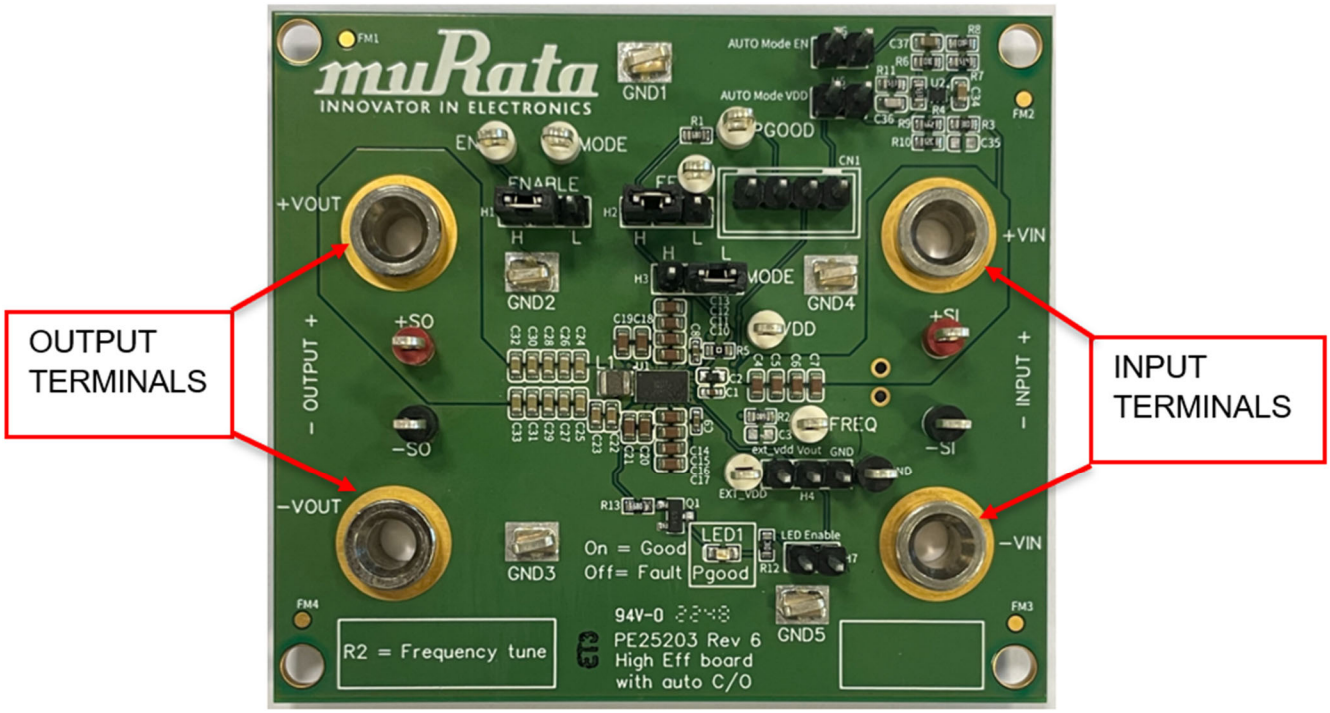

Figure 1. PE25203 Evaluation Board Assembly

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PCB Headers

The PE25203 EVK has two types of PCB headers:

- Three-way PCB headers configure the EVK.
- Two-way PCB headers enhance the EVK functionality.

Configuration PCB headers

Before you apply power to the EVK, fit the jumper sockets on the H1 and H2 PCB headers. The settings are loaded at IC power-up. If you change H2 during operation, disable the system and then enable it to allow the IC to load the new settings. You can change H3 during operation as needed.

Table 3 lists information about each three-way PCB header.

Table 3. Three-way PCB Headers Information

Header	Signal Name	Function	High	Low
H1	ENABLE	IC enable pin. Logic high enables the IC, and logic low disables the IC.	Enable	Disable
H2	FF/CS	Selects the charge pump clock mode (logic high = fixed frequency, logic low = cycle skip). Read at IC power up. The value in this pin can be changed when EN = logic low.	Fixed frequency	Cycle skip
H3	MODE	Selects the charge pump voltage division ratio. This pin must not be allowed to float. MODE = logic high or V_{IN} or 3.6V for divide-by-2 mode. MODE = logic low for divide-by-3 mode	Divide-by-2	Divide-by-3
H4	EXT VDD	External V_{DD} input pin. In this mode, the IC is powered from the external V_{DD} instead of the internally generated V_{DD}. The part does not need this to be supplied to operate, but if externally applied, it can increase the system efficiency. This pin can also be connected to the VOUT pin. Iif not used, connect it to GND.	V_{OUT}	GND

Figure 2 shows how to use a jumper to set the three-way PCB header in the HIGH or LOW position.

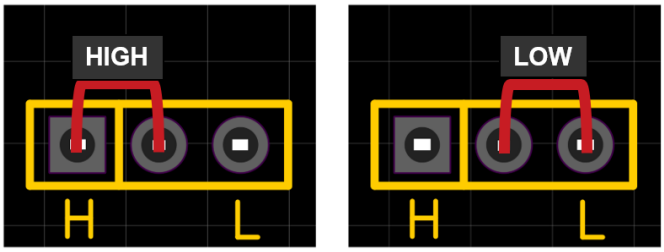

Figure 2. Three-way PCB Header Configuration Settings

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PCB Header Functionality

Some extra functions are added to the EVK. Two-way PCB headers are optional to use. Table 4 lists the two-way PCB headers. To use any of the functions described in Table 4, a jumper should be used to ensure the extra function is enabled. If the H5 and H6 jumpers are in use, do not fit a jumper socket in H3.

Table 4. Two-way PCB Header Information

Header	Signal Name	Function
H5	AUTO Mode VDD	Connects the U2 comparator to the PE25203 VDD pin.
H6	AUTO Mode EN	Connects the comparator output to the MODE pin.
H7	LED enable	LED1 lights ON when the PE25203 allows PGOOD to be pulled high and to indicate that the charge pump is ready to support the full load current.

Sensing Points

Table 5 lists all test points (TPs) found in the PE25203 EVK. Use the TPs to easily monitor the waveforms of critical signals.

To make accurate measurements of the input and output voltages, use the SO and SI test points included in the PE25203 EVK.

Table 5. Test Point Descriptions

Test Point	Description
EN	Status of the enable signal
MODE	Status of the mode signal
FF	Status of the charge pump clock mode (fixed frequency or cycle skip).
PG	Status of the PGOOD signal
VDD	V_{DD} generated by the IC. Typically, 3.6V is generated on this pin.
FREQ	See the voltage set at this pin.
+SO	Positive TP to measure V_{OUT}
-SO	Negative TP to measure V_{OUT}
+SI	Positive TP to measure V_{IN}
-SI	Negative TP to measure V_{IN}
EXT VDD	Positive TP to measure EXT VDD
GND	0V reference TP
GND1–GND5	0V reference TP

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EVK Connection

Connect the EVK and the measuring equipment as shown in Figure 3.

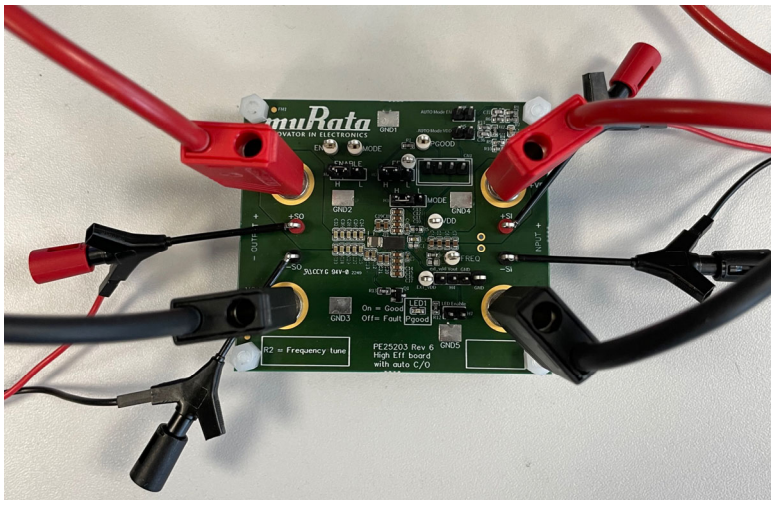

Figure 3. EVK Connection Example

Figure 4 shows the connections for voltage-only measurements.

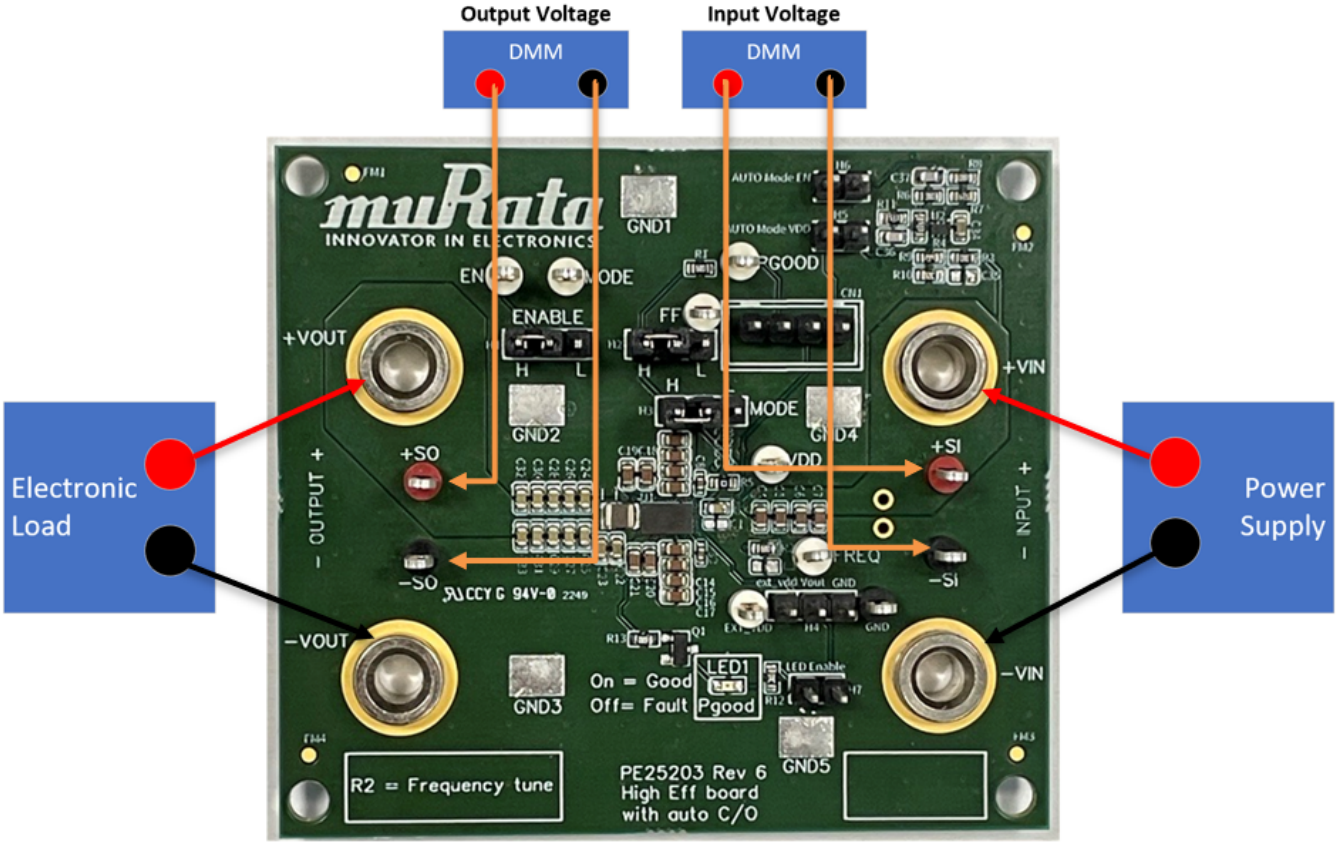

Figure 4. PE25203 EVK Connections to Measure Voltage

If the power supply has remote sense capability, use the +SI and -SI pins to sense the input voltage at the VIN IC pins.

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Figure 5 shows the connections for voltage and current measurements

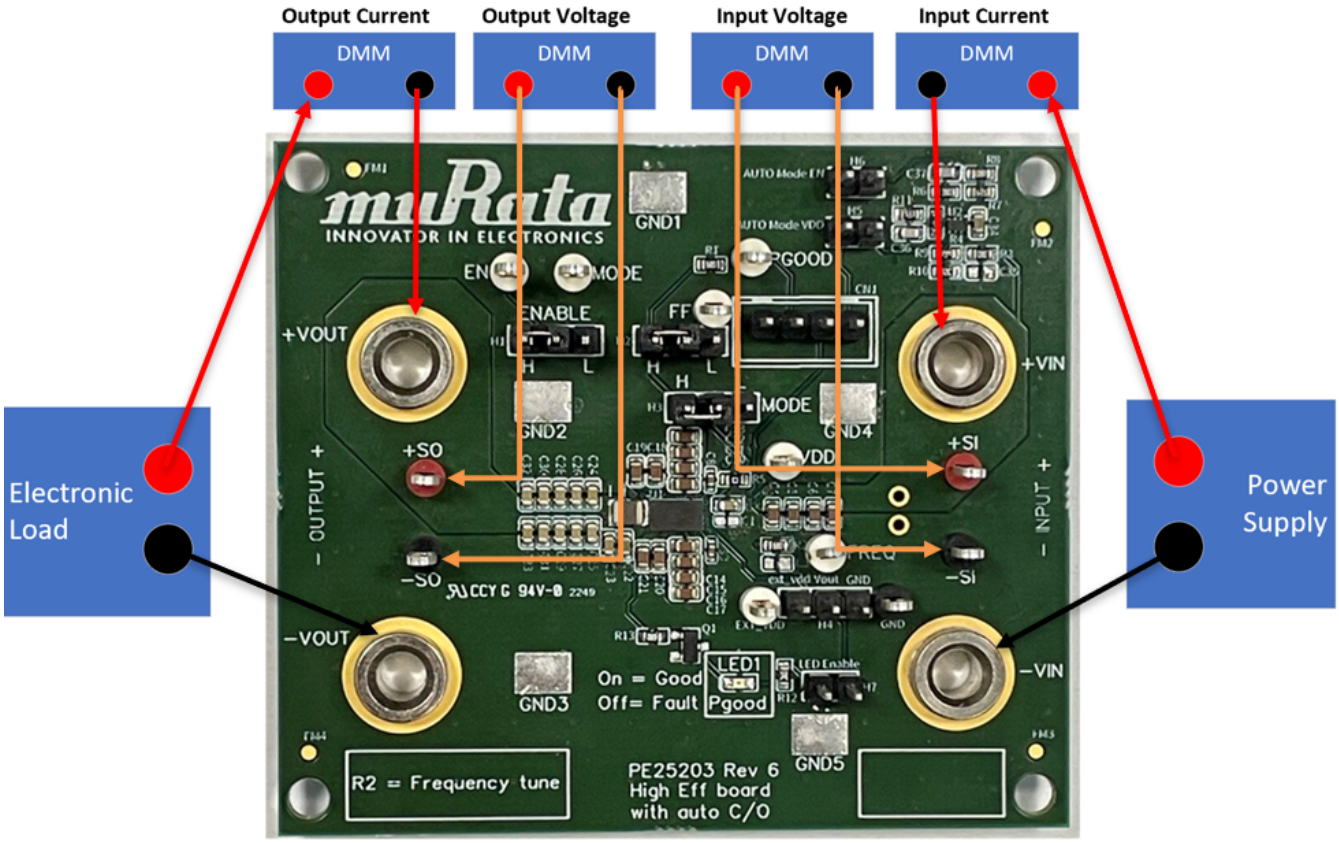

Figure 5. PE25203 EKV Connections to Measure Voltage and Current

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Hardware Operation

This section includes the general guidelines for operating the EVK. To configure the EVK and achieve optimal performance, follow these steps:

1. Before you power-up the EVK, set the H1 and H2 PCB headers by fitting the jumper sockets. In Figure 6, H1 is in the enable position and H2 is in fixed-frequency mode.
2. H3 sets the EVK division ratio. In Figure 6, H3 is set to divide-by-2 mode, and all the other extra functions are NOT implemented. If the H3 header is left unused, the EVK powers up in divide-by-3 mode by default. Do not leave H3 without a jumper in the HIGH or LOW position.
3. Verify that all power and sensing connections are made correctly. Minimize the wire lengths.
4. Apply the input voltage.
5. After the EVK starts up successfully, apply the load current.

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EVK Startup

When starting the EVK, start it with no load.

If the EVK is started with a load, it might not start due to the soft-start current limit.

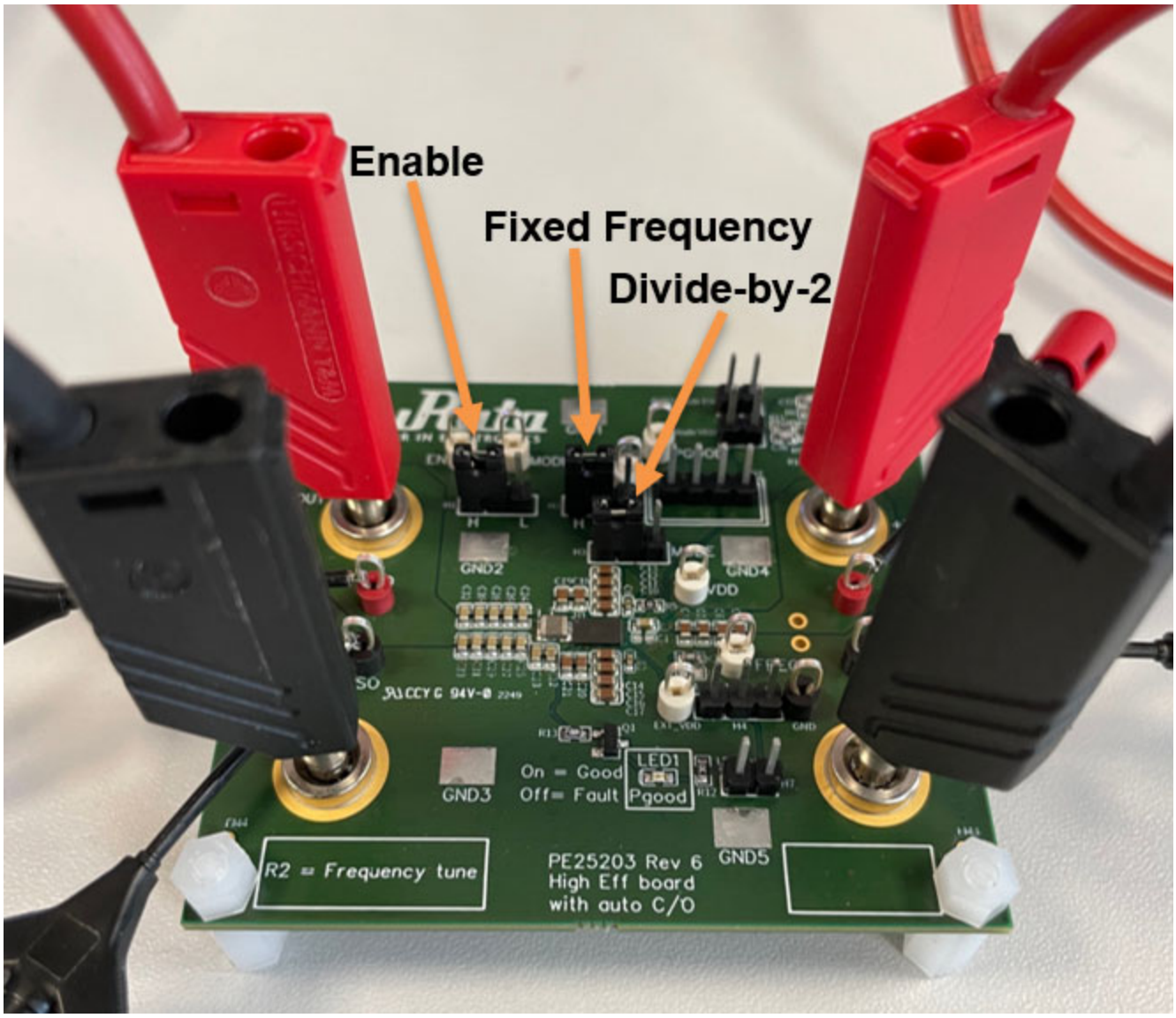

Figure 6. Jumper Configuration

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Set the Operating Frequency

Use the FREQ pin to set the PE25203 operating frequency. To save a resistor, you can also connect the FREQ pin to GND to oscillate at a nominal 200 kHz. This is the oscillation frequency at the VX pin and the charge pump frequency per phase switches at 50% of this value.

To adjust the frequency, connect a resistor between 82.5 KΩ and 505 KΩ between the FREQ pin and GND. Use the following equation to find the required VX switching period in µs:

VX switching period = (0.0093 * resistance value in kΩ) + 0.2254

Using a resistor value of 499 KΩ in the equation above,

VX switching period = (0.0093 * 499) +0.2254 = 4.87µs (205 kHz)

Figure 7 shows the VX switching period vs. the resistance value set at the FREQ pin.

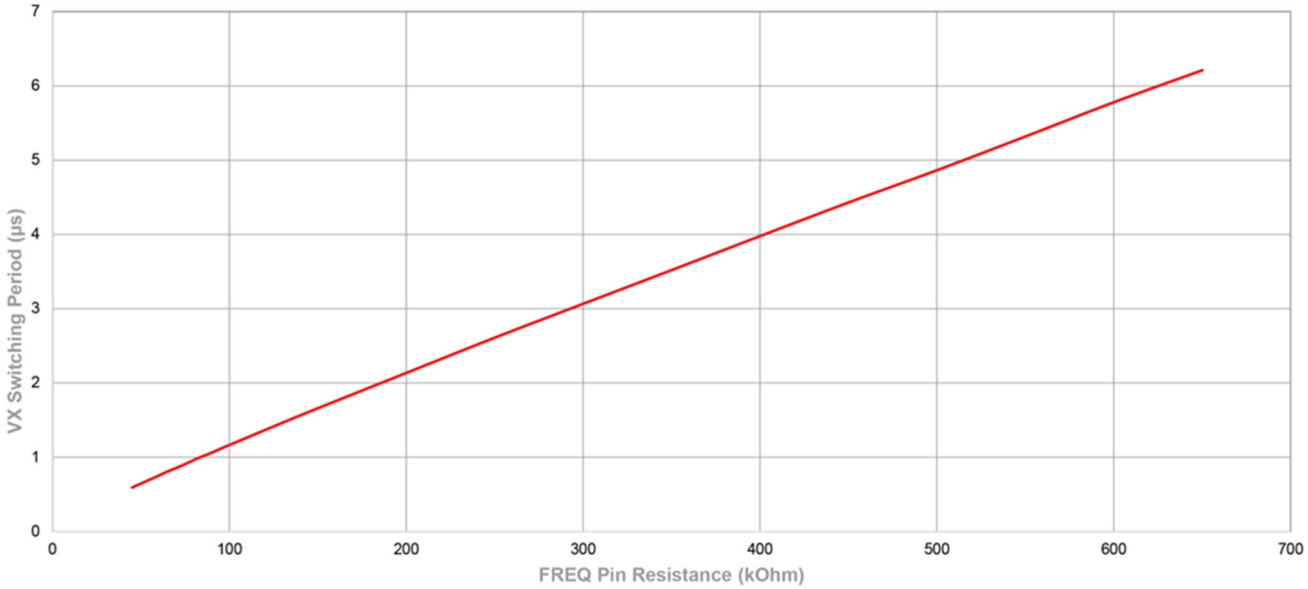

Figure 7. VX Switching Period vs. Resistance Value on the FREQ Pin

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Figure 8 shows the location of FREQ resistor R2. The PE25203 EVK uses a 499 KΩ resistor for R2.

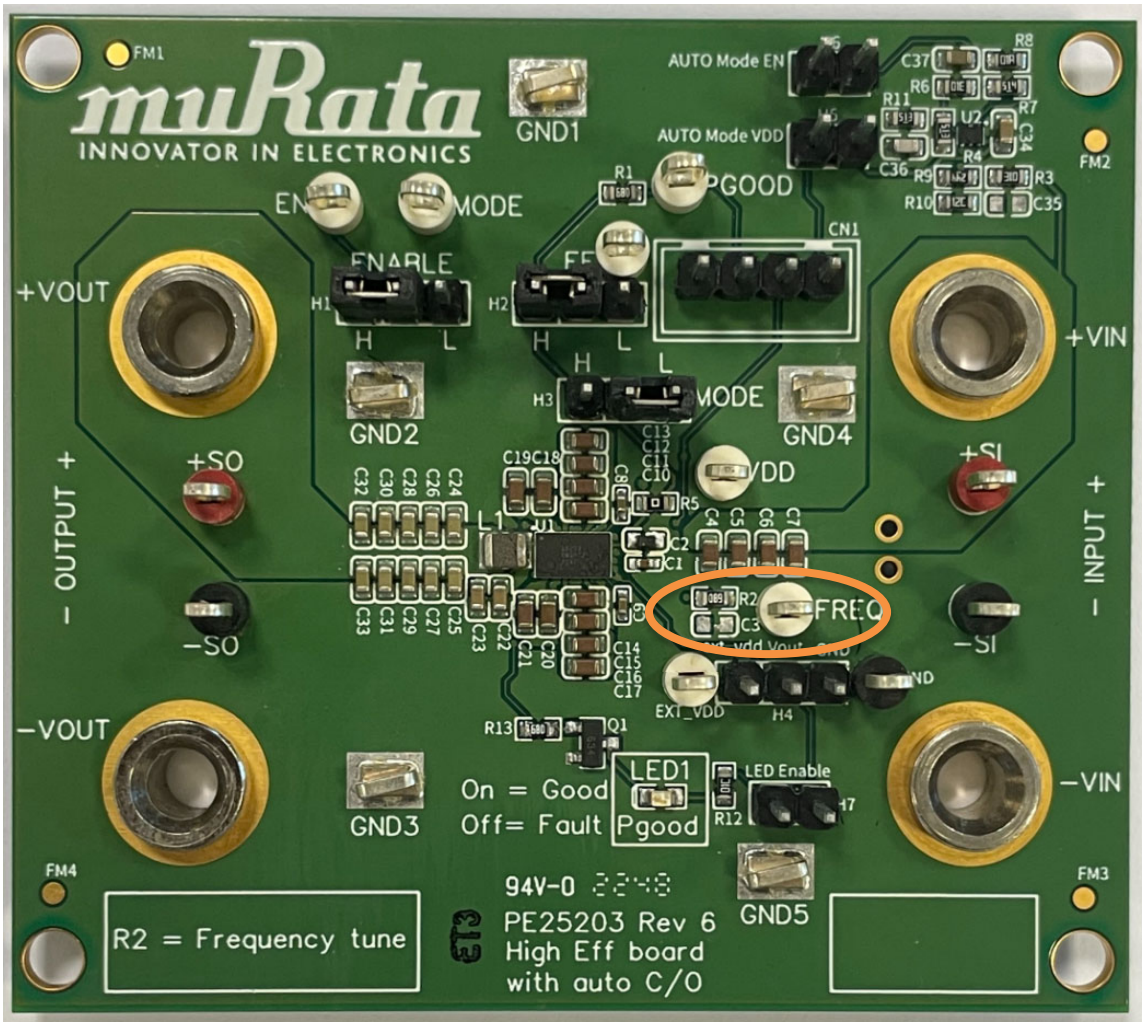

Figure 8. R2 Location

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Test Results

Figure 9 and Figure 10 show the typical performance of the PE25203 evaluation board at the following nominal voltages:

- 7.7V for divide-by-2 mode
- 11.55V for divide-by-3 mode

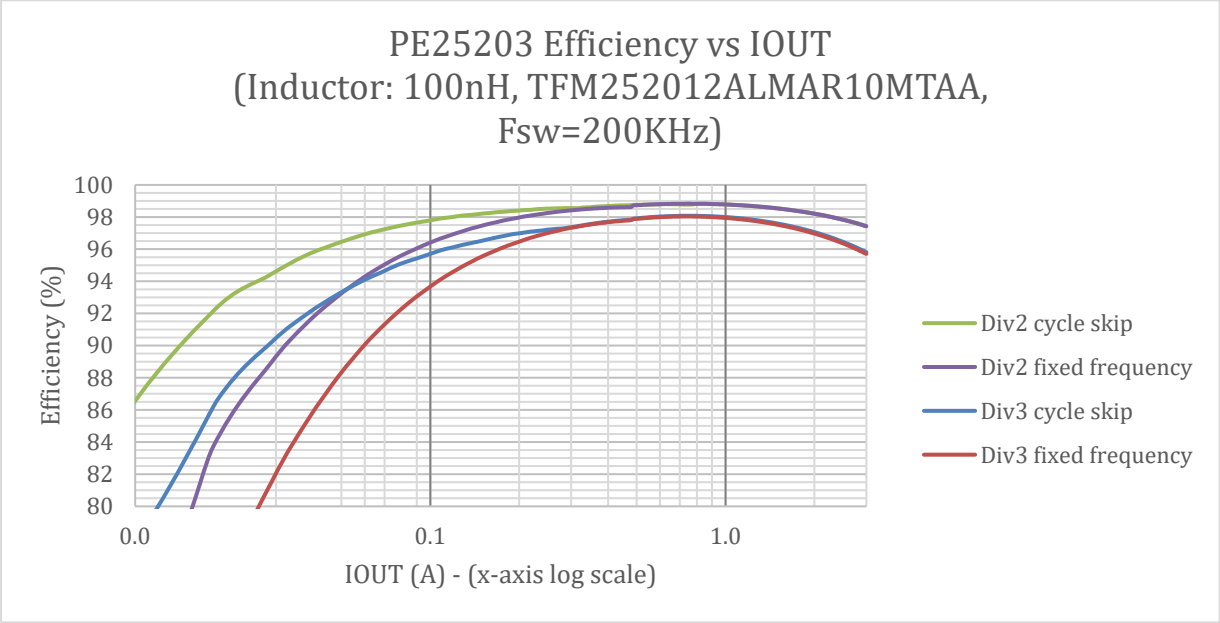

Figure 9. PE25203 Efficiency Plots

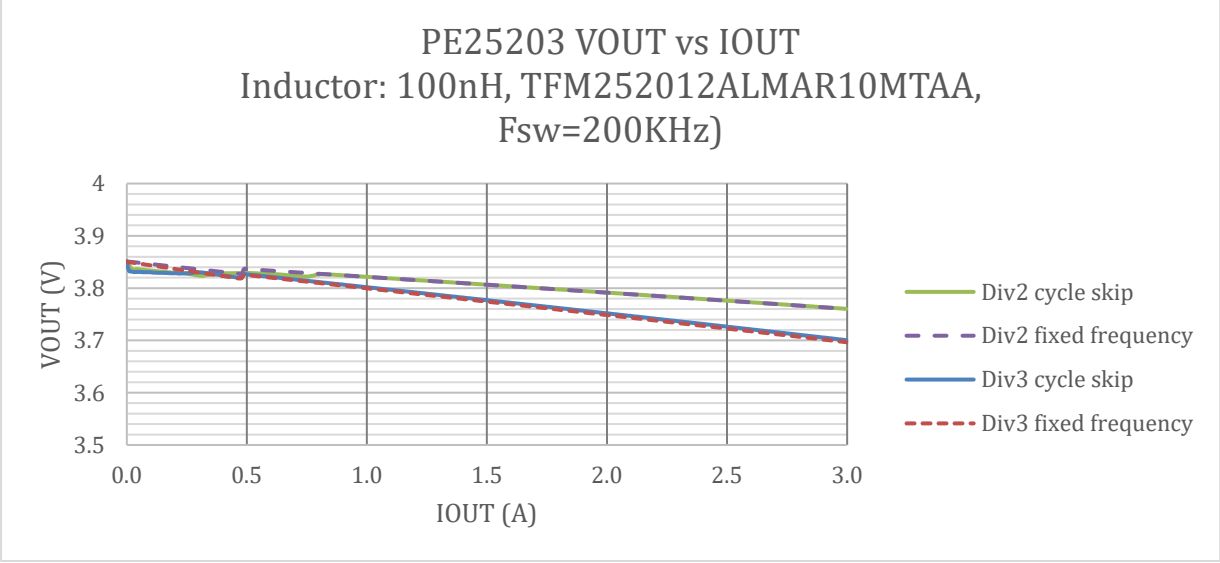

Figure 10. Line Regulation (V_{OUT}) vs. I_{OUT}

For more waveforms and test data, see the *PE25203 Data Sheet*.

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Auto-switch Mode

Auto-switch mode allows the EVK to automatically change the division ratio by measuring the input voltage. An inverting comparator with hysteresis shown in Figure 11 is implemented to achieve the auto-switch mode of the PE25203 EVK.

The hysteresis is used to improve stability against noise, and it also can be used to set two different threshold voltages:

- Vtrigger_low to change from div3 to div2 division ratio
- Vtrigger_high to change from div2 to div3 division ratio

Resistors R6, R7, R9, and R10 can be adjusted to achieve specific voltage trigger points.

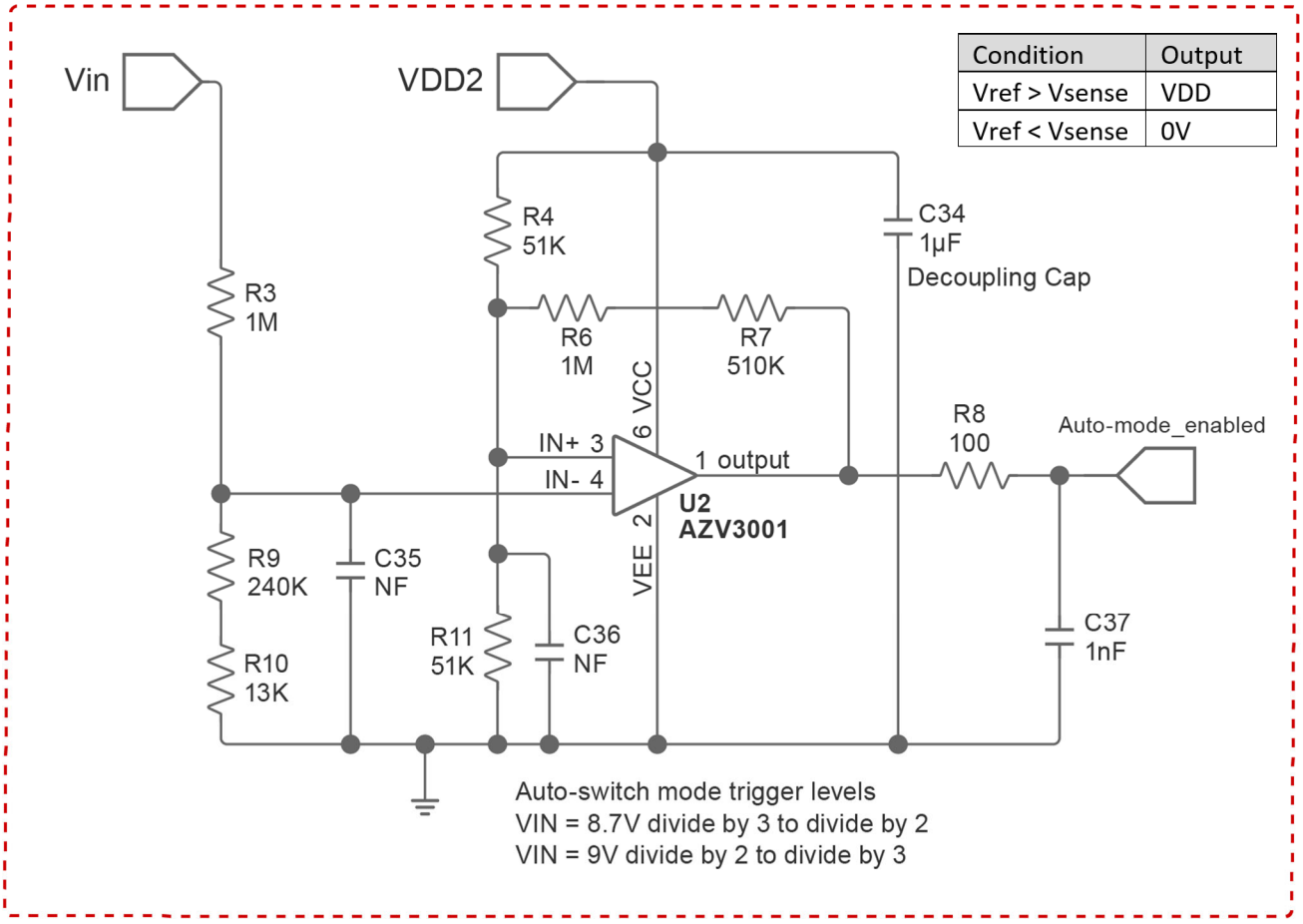

Figure 11. Auto-switch Mode Circuit Tuning Resistors

pSemi created an Excel file to calculate the values of resistors R6, R7, R9, and R10. See the Excel File Instructions on page 17.

R9 and R10 control the voltage seen by the negative terminal (V-) of the comparator. R6 and R7 decrease or increase the hysteresis voltage, which can set two different voltage trigger points. The larger the values of resistors R6 and R7, the smaller the hysteresis voltage.

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Auto-switch Mode Implementation

To implement the auto-switch mode function, place a jumper socket on the H5 and H6 PCB headers and remove the jumper socket from H3. If not using the EVK in auto-switch mode, the H3 header is used for the fixed-division ratio (divide-by-2 (HIGH position) or divide-by-3 (LOW position)). Do not power up the EVK if the jumper sockets are placed on H3 and H6. To avoid damage to the EVK, set only one PCB header.

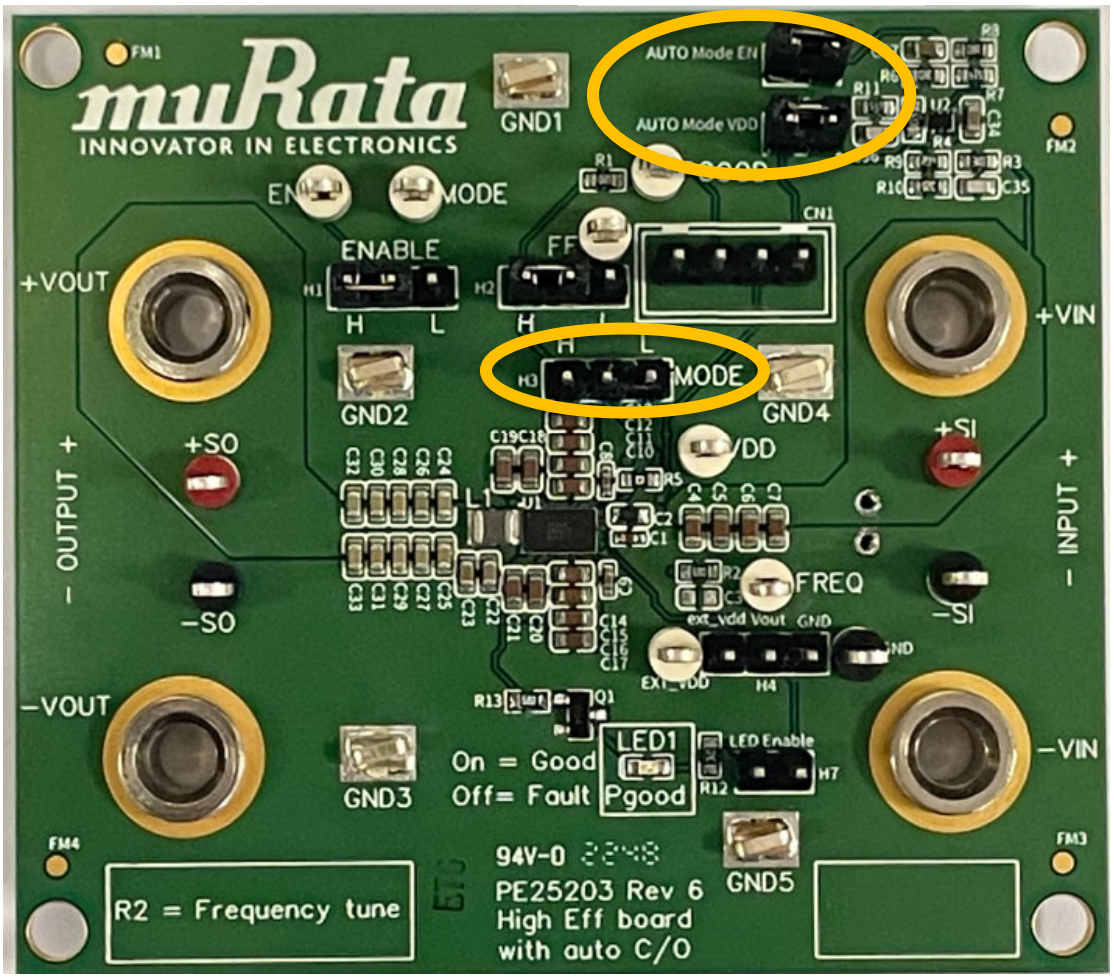

Figure 12. PE25203 EVK with Auto-switch Mode Circuit

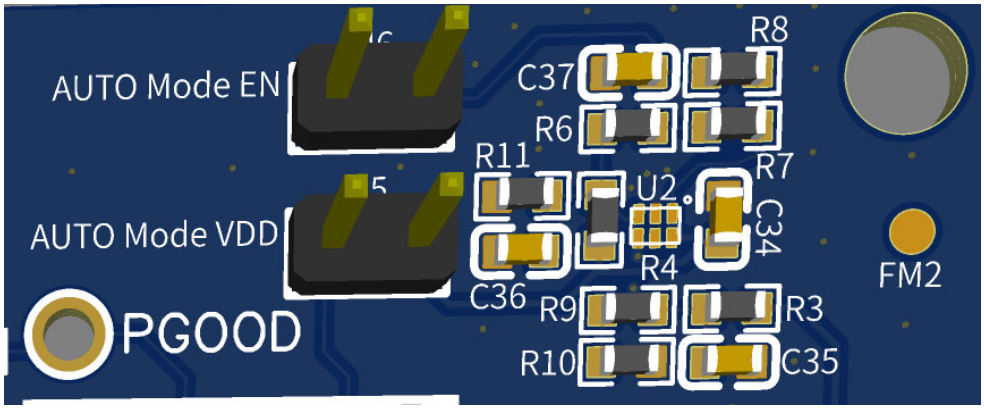

Figure 13. 3D Image from Auto-switch Mode Circuit

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Excel File Instructions

Table 6 lists the indications in the Excel file, as shown in Figure 14.

Table 6. Excel File Indications

Color	Indication
Yellow	User interface
Blue	The V_{REF} and V_{SENSE} voltages are within range.
Green	Low percentage of error between the calculated resistor values and the implemented resistor values. Low percentage of error between the V_{REF} and V_{SENSE} voltages.
Red	Large percentage of error between the V_{REF} and V_{SENSE} voltages.

Tune the circuit until all V_{REF} and V_{SENSE} values are shown in blue, and all percentage of error values are shown in green.

STEP1	User Voltage Inputs							
	VDD	3.6	V		Measure from EVK			
	Vtrigger_low	8.7	V		User specification			
	Vtrigger_high	9	V		User specification			
STEP2	Vsense resistor							% error
	R9	240000	Ω		R9 & R10_calculated	255319	Ω	-0.91%
	R10	13000	Ω					
STEP3	Hystereses Resistor							% error
	R7	510000	Ω		R7 & R6_calculated	1504500	Ω	0.37%
	R6	1000000	Ω					
	Voltage outputs							% error
	Vref_low	1.770	V		Vsense_low	1.757	V	0.77%
	Vref_high	1.830	V		Vsense_high	1.817	V	0.70%

Figure 14. Excel File Example

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Step 1: Measure the VDD voltage from the EVK

Use the VDD test point to measure the VDD voltage from the EVK. Enter this value in the Excel file.

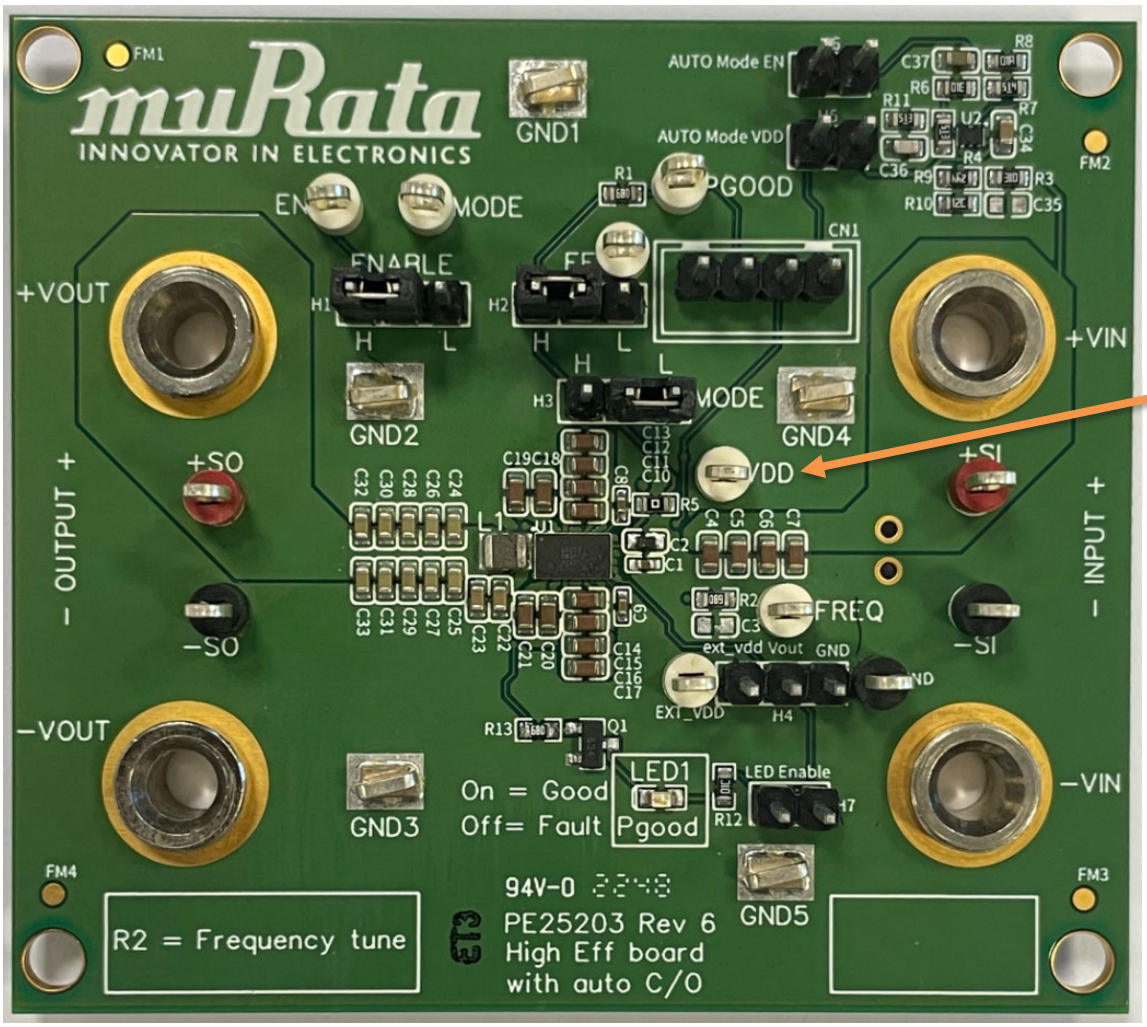

Figure 15. VDD Test Point

Set the voltage trigger levels

Set the voltage levels where the charge pump is required to automatically change the division ratio:

- Vtrigger_low: The charge pump changes from divide-by-3 mode to divide-by-2 mode.
- Vtrigger_high: The charge pump changes from divide-by-2 mode to divide-by-3 mode.

To avoid taking the charge pump system into under-voltage lockout (UVLO) conditions while under heavy load operations, do not set Vtrigger_low below 8.6V.

After setting the Vtrigger_low and Vtrigger_high voltages, enter them in the Excel file, as shown in Figure 16.

STEP1	User Voltage Inputs			
	VDD	3.6	V	Measure from EVK
	Vtrigger_low	8.7	V	User specification
	Vtrigger_high	9	V	User specification

Figure 16. Step 1 Excel File Example

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Step 2: Tune the Vsense Resistor

Using the Excel file, modify the R9 and R10 values to match their calculated values.

R9 and R10 are in series to achieve more resistor values than by using only one resistor at the bottom of the voltage divider network. If the calculated value can be achieved with only one resistor, install a 0Ω resistor for the unused resistor.

In Figure 17, the calculated value was achieved by using two different resistor values. Always aim to achieve the lowest percentage error possible.

STEP2	Vsense resistor							% error
	R9	240000	Ω		R9 & R10_calculated	255319	Ω	-0.91%
	R10	13000	Ω					

Figure 17. Step 2 Excel File Example

Step 3: Tune the Hysteresis Resistor

After you define the R9 and R10 values, use the Excel file to modify the R7 and R6 values to match their calculated values.

As mentioned before, resistors R7 and R6 decrease or increase the hysteresis voltage.

In Figure 18, the calculated value for R7 and R6 was 1504500Ω, R6 was set 1MΩ, and R7 was set to 510KΩ. The percentage of error achieved is low. R6 is set to 1MΩ to start the tuning process. If required, modify the R6 value if R7 cannot achieve the calculated value.

STEP3	Hystereses Resistor							% error
	R7	510000	Ω		R7 & R6_calculated	1504500	Ω	0.37%
	R6	1000000	Ω					
	Voltage outputs							% error
	Vref_low	1.770	V		Vsense_low	1.757	V	0.77%
	Vref_high	1.830	V		Vsense_high	1.817	V	0.70%

Figure 18. Step 3 Excel File Example

From the voltage outputs, there is very low percentage of error between V_{REF} and V_{SENSE}.

If the device is held in the transition region for a long time at high load currents, it could reach the over-temperature threshold and switch off in a fault mode. During the transition, limit the maximum load to 1.5A.

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Layout Considerations

Figure 19 shows the critical components required to implement the PE25203. The highlighted red lines are the high-power nodes in the design. Pay close attention to the parasitic resistance and inductance at these nodes.

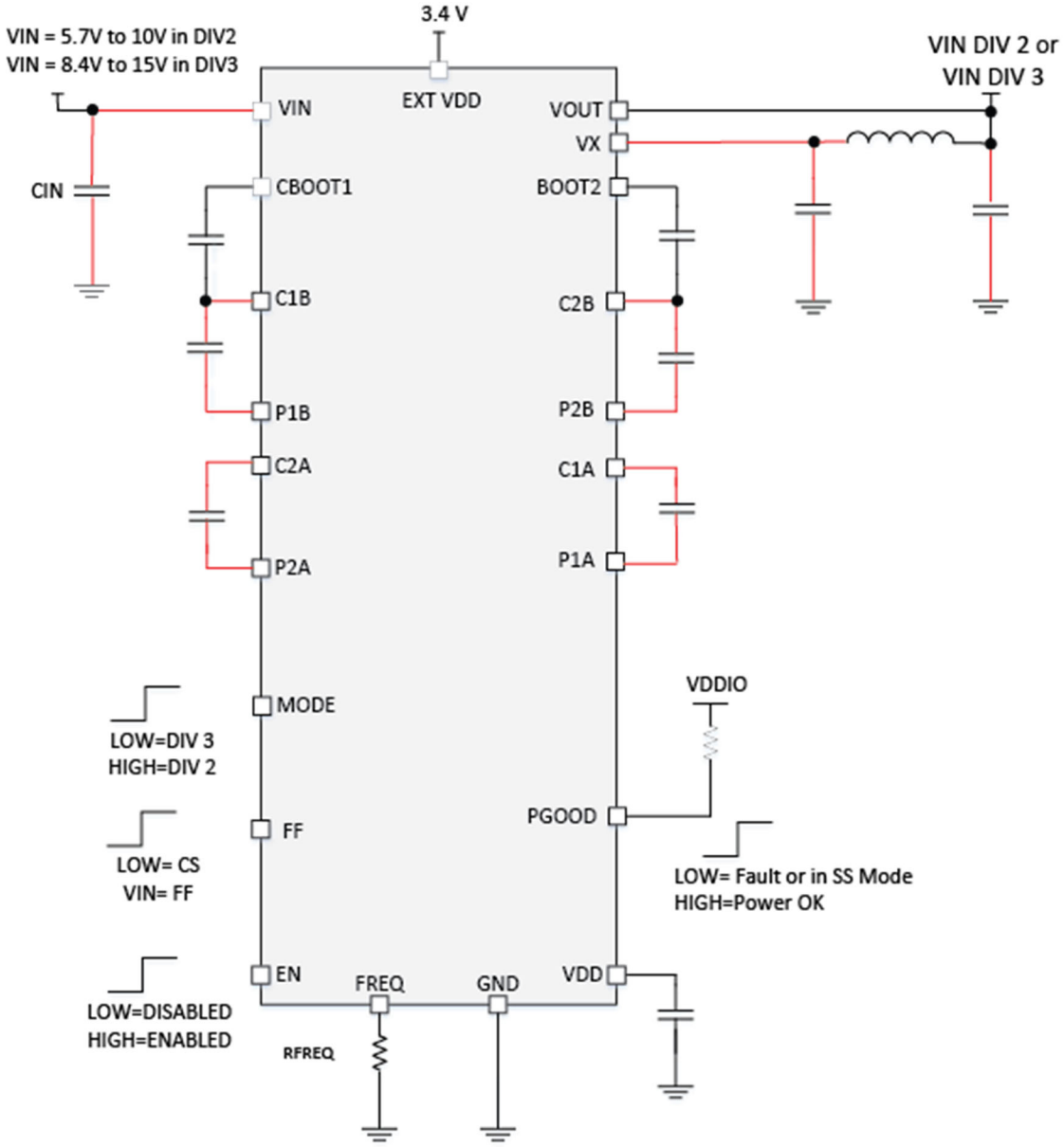

Figure 19. PE25203 Simplified Application Schematic

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Component Placement

Figure 20 shows the PE25203 pin map for the WLCSP. Figure 21 shows a 3D image of the placement of the most critical components required to implement the PE25203. All components are placed on the top layer of the PCB. In the PE25203 EVK, the IC is placed as shown in Figure 21 where the V_{IN} voltage is on the right side and the VX voltage (the IC output voltage that must be filtered) is on the left side. Similarly, for other designs, the PE25203 can be placed in the opposite direction, but the components must be placed as close as possible to the PE25203, as shown in Figure 21.

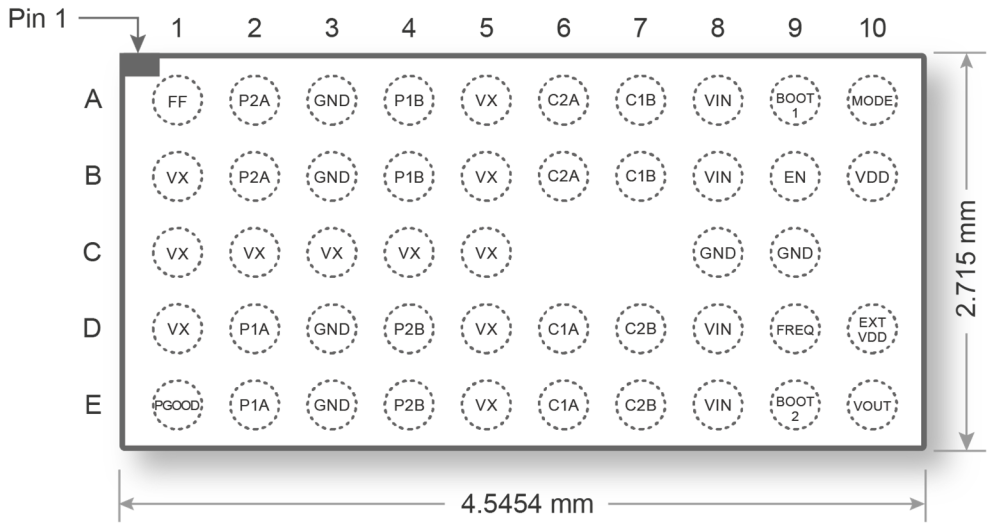

Figure 20. PE25203 Pin Configuration Top View (Bumps Down)

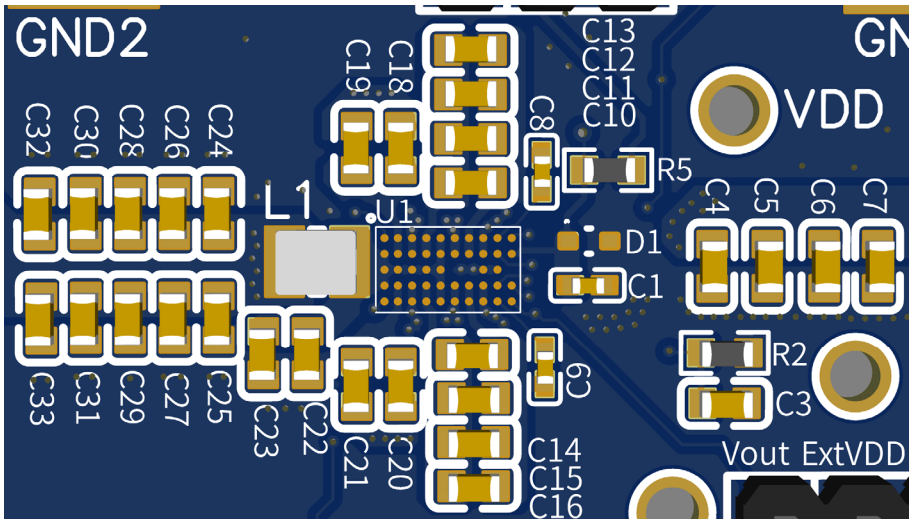

Figure 21. PE25203 Critical Component Layout Example

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PCB Layout Information

Figure 22 shows the PCB routing of the IC. Wide traces reduce the resistance and multiple vias connect the different layers, thus improving the vertical connection and reducing the parasitic inductance.

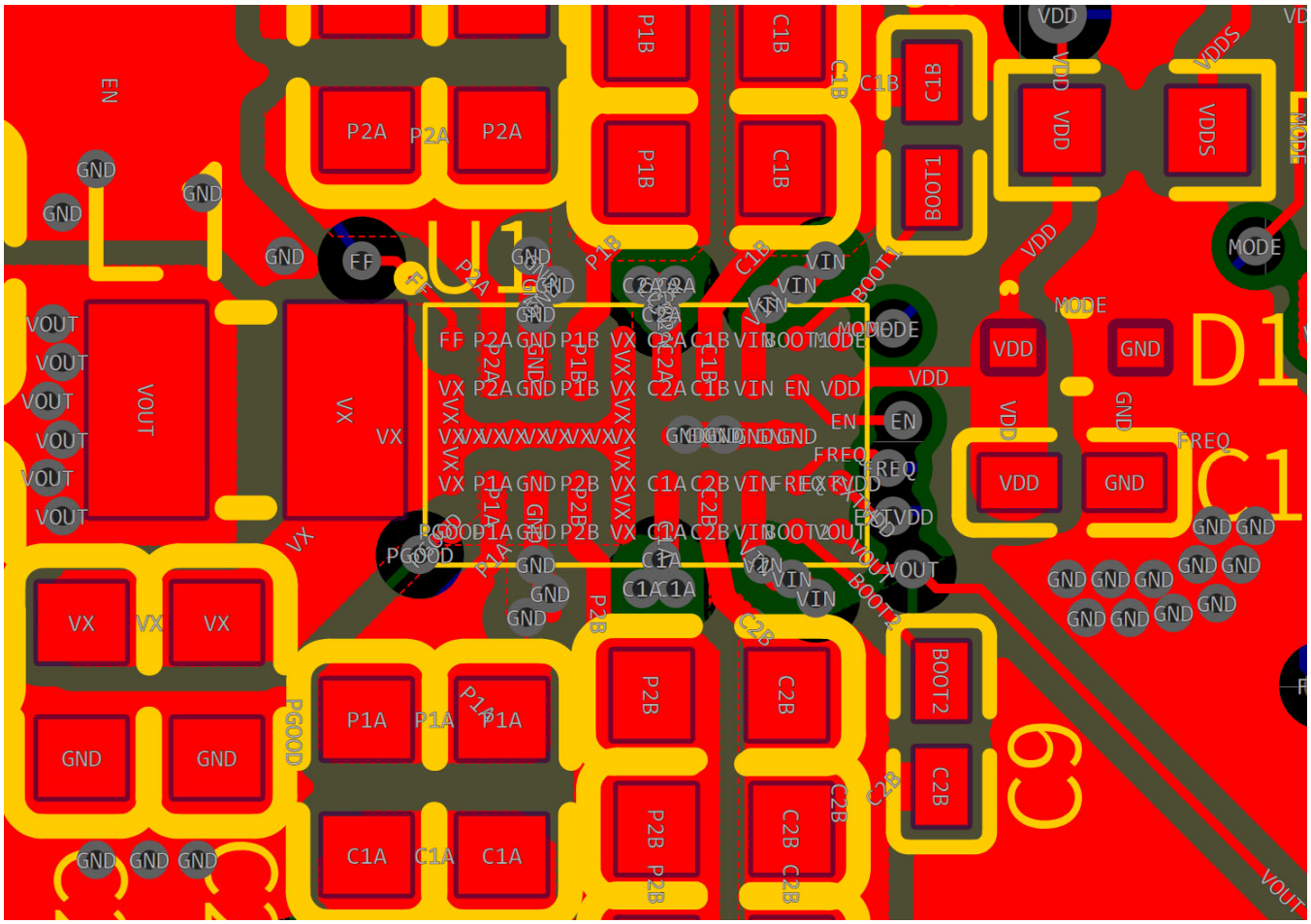

Figure 22. PE25203 PCB Routing Example

Figure 23–Figure 27 show a Type-III PCB layout example using a 4-layer board. The trace width and spacing is 0.1mm/0.1 mm. The via sizes are 0.2-mm holes with 0.1-mm pads.

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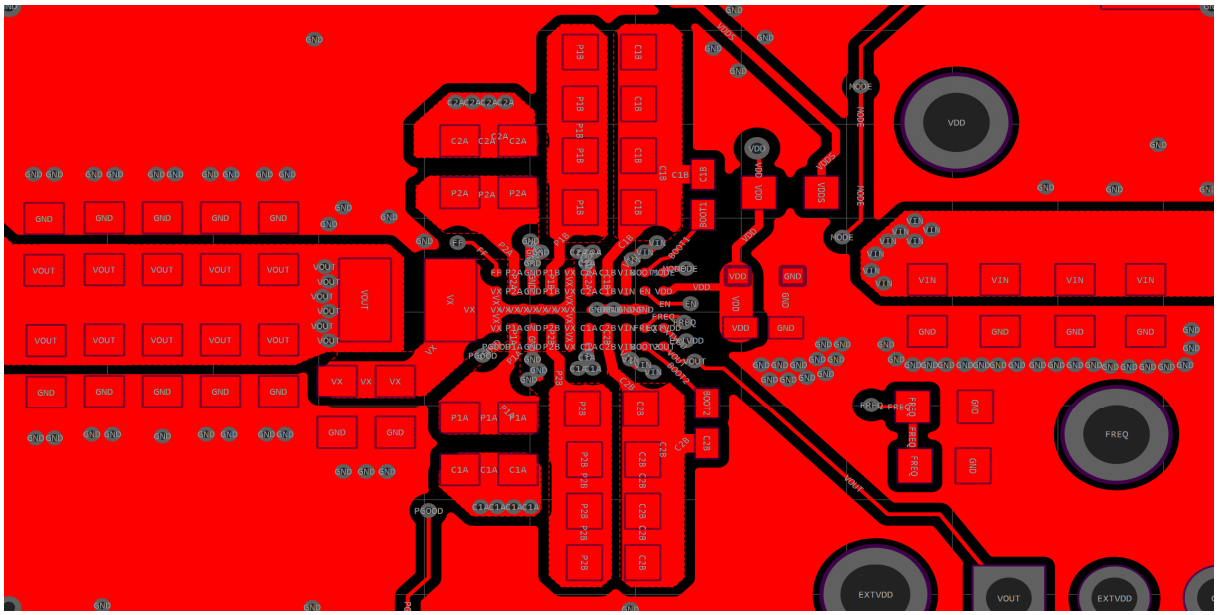

Figure 23. Top Layer

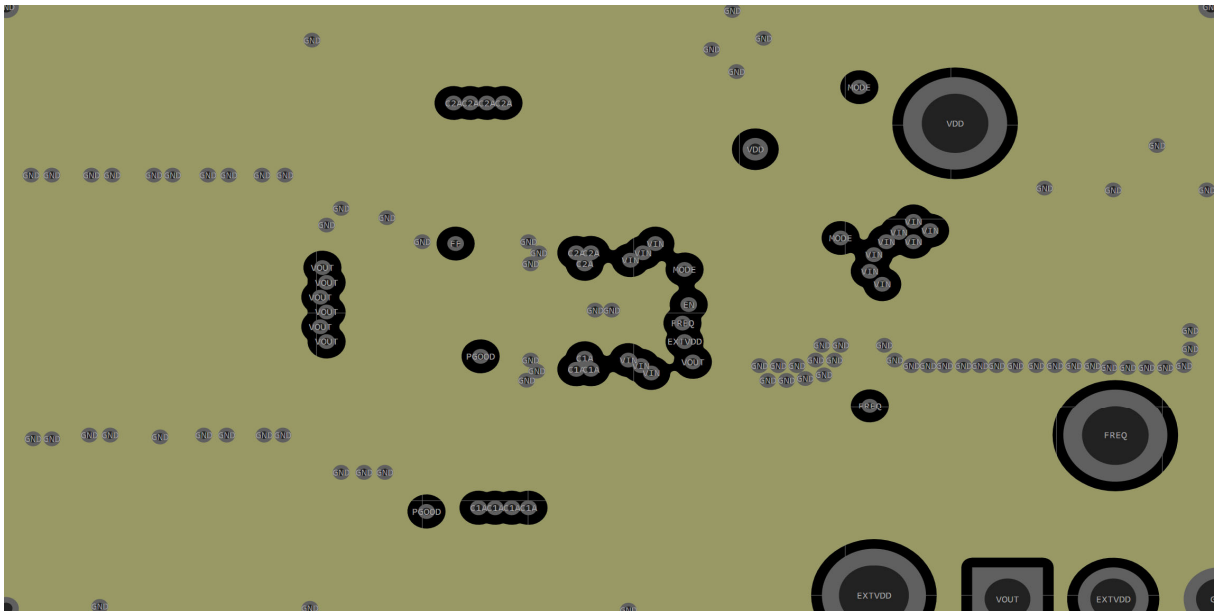

Figure 24. Inner Copper Layer 1

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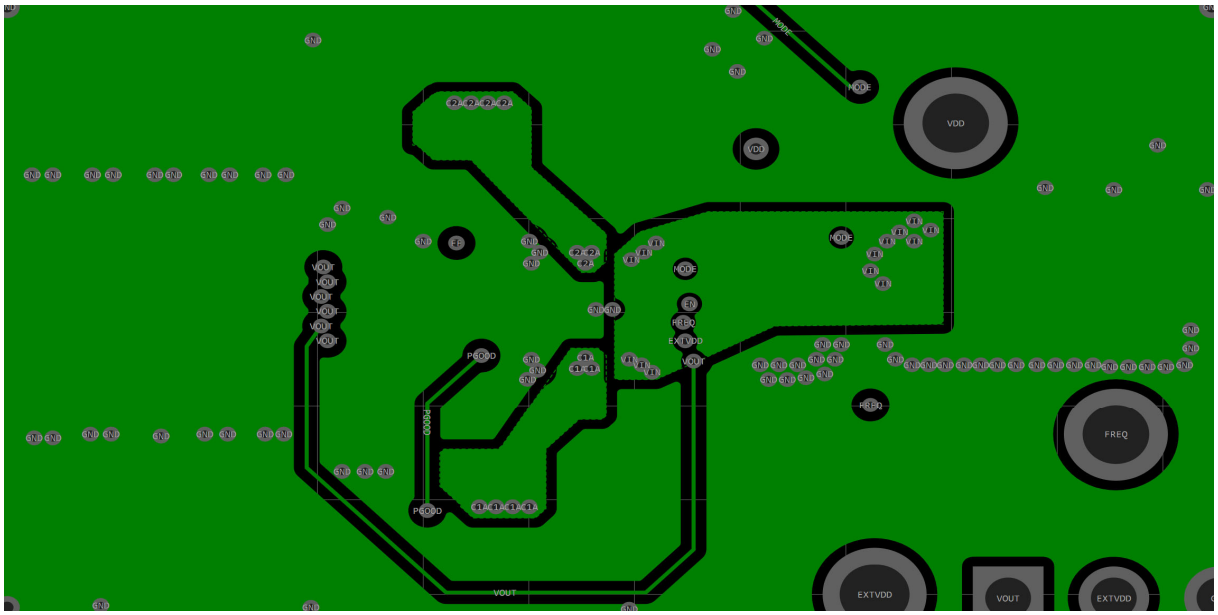

Figure 25. Inner Copper Layer 2

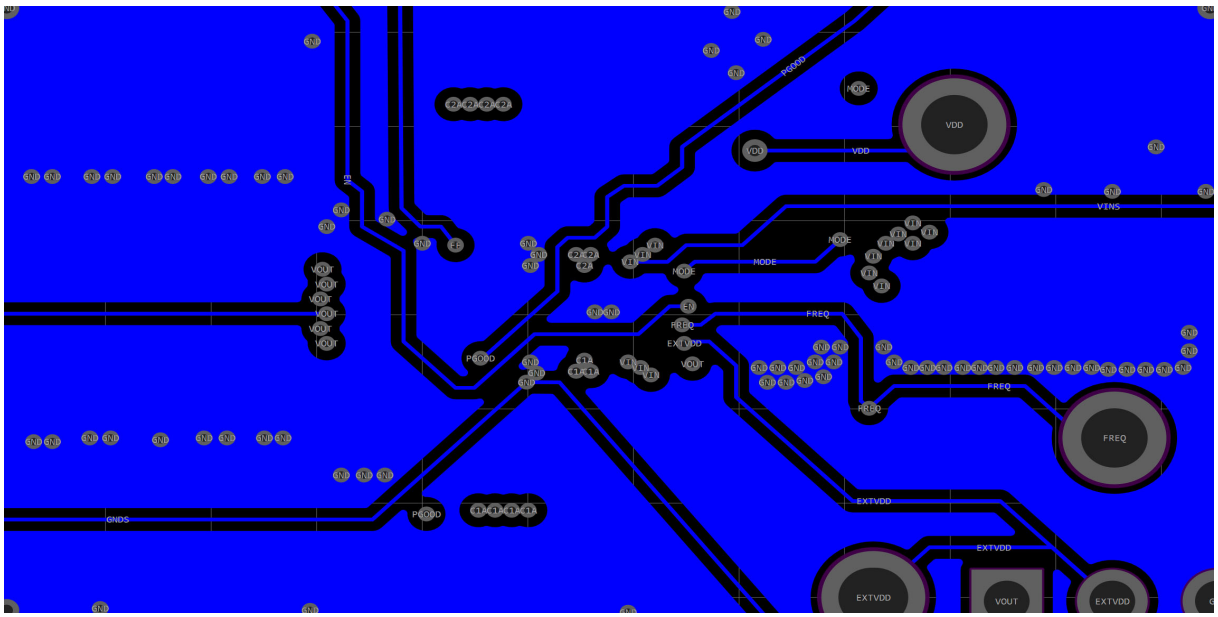

Figure 26. Bottom Copper Layer

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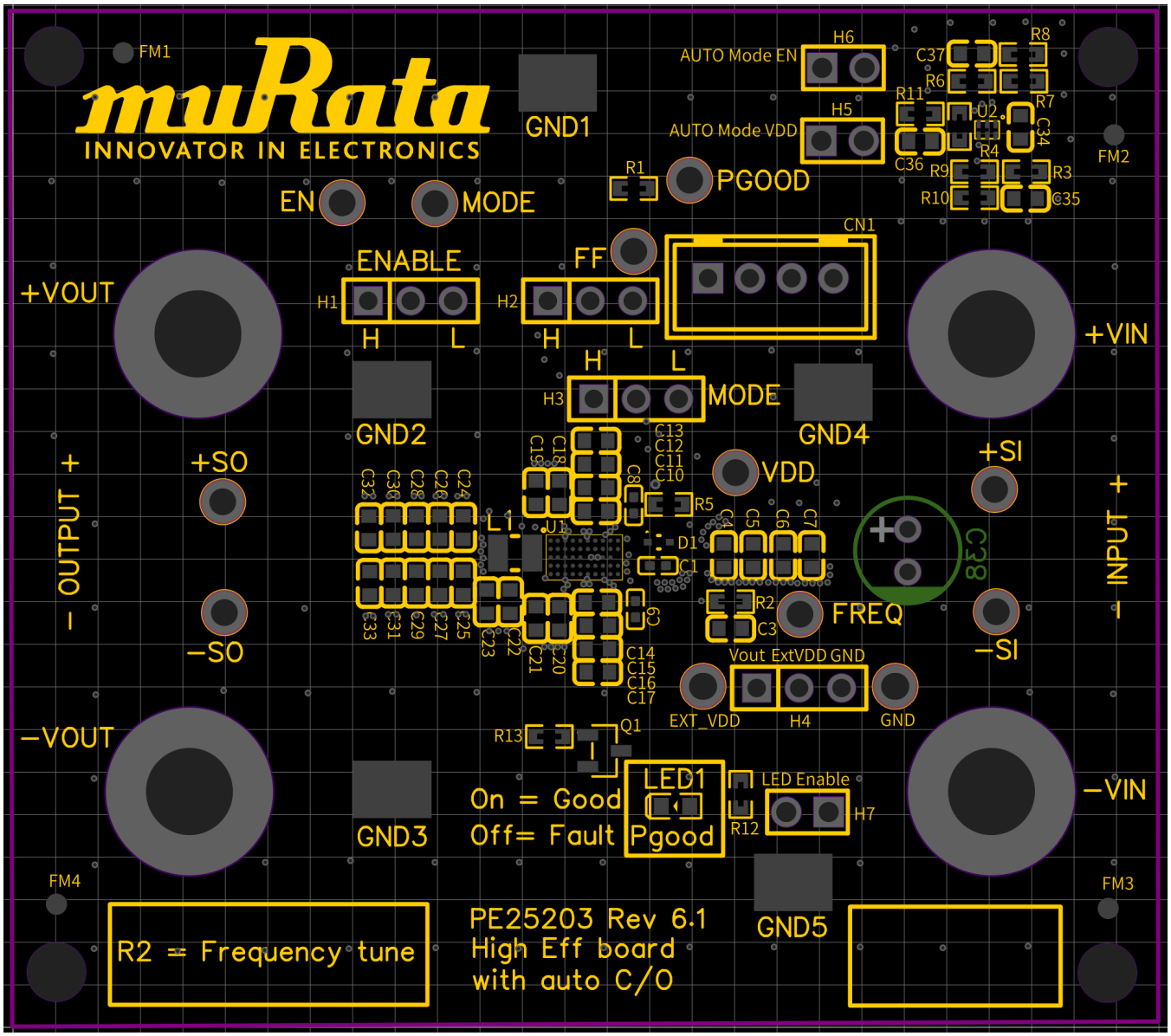

Figure 27. Top Layer Silkscreen

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Functional Block Diagram

Figure 28 shows the PE25203 functional block diagram.

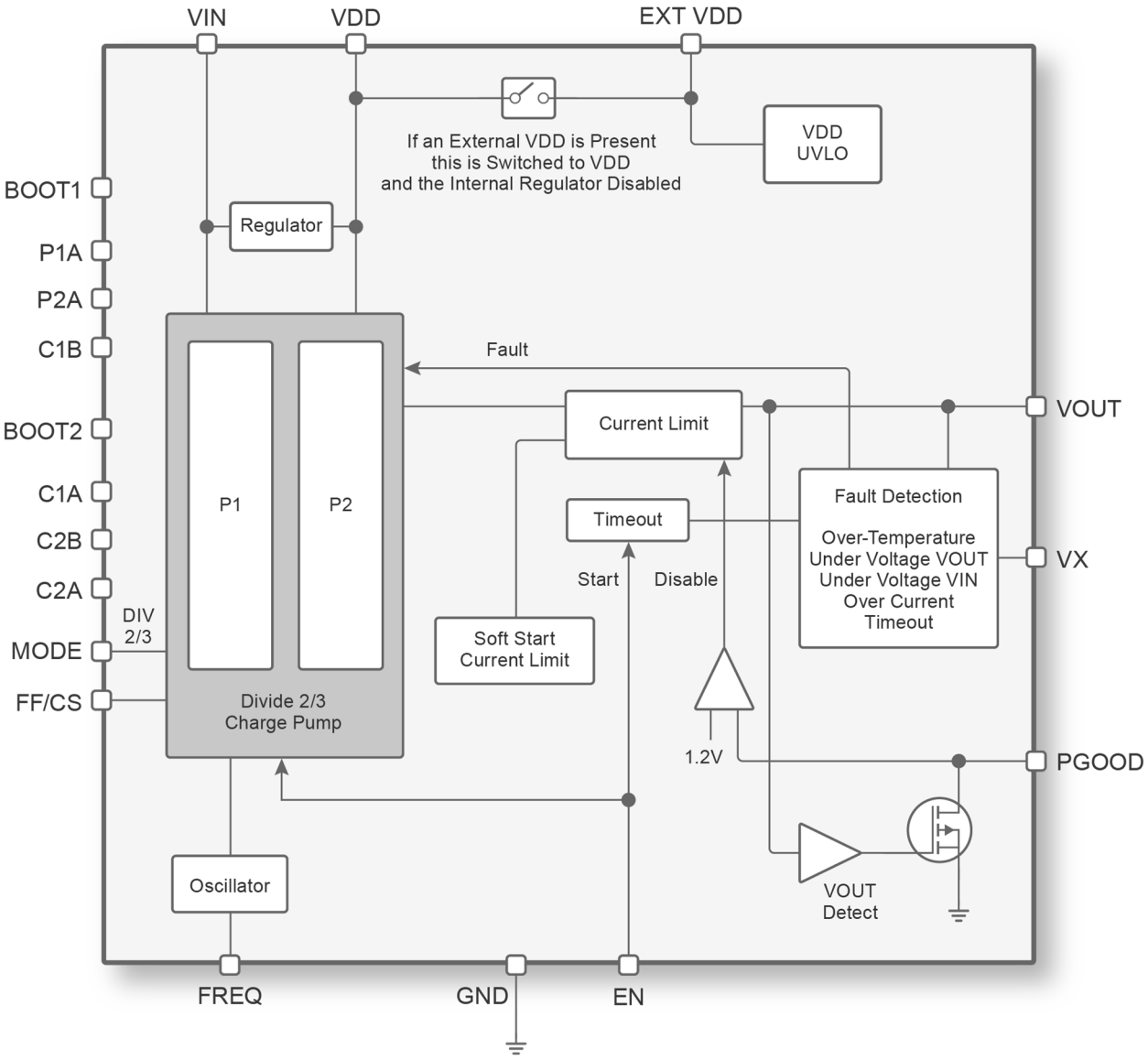

Figure 28. PE25203 Functional Block Diagram

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EVK PCB Schematics

Figure 29 shows the EVK PCB schematic.

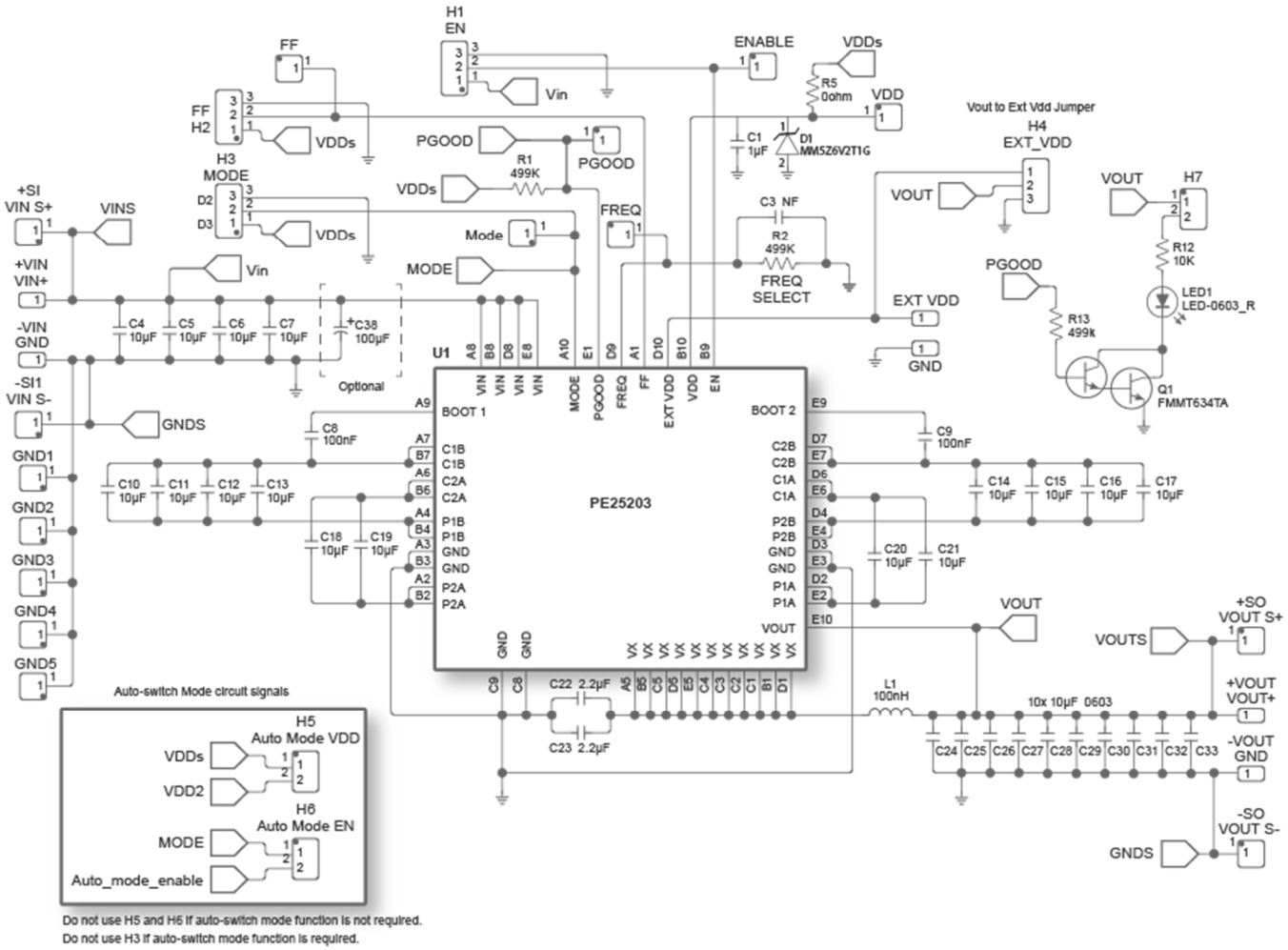

Figure 29. Charge Pump Circuit Schematic without Auto-switch Mode Circuit

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Figure 30 shows the auto-switch mode circuit schematic.

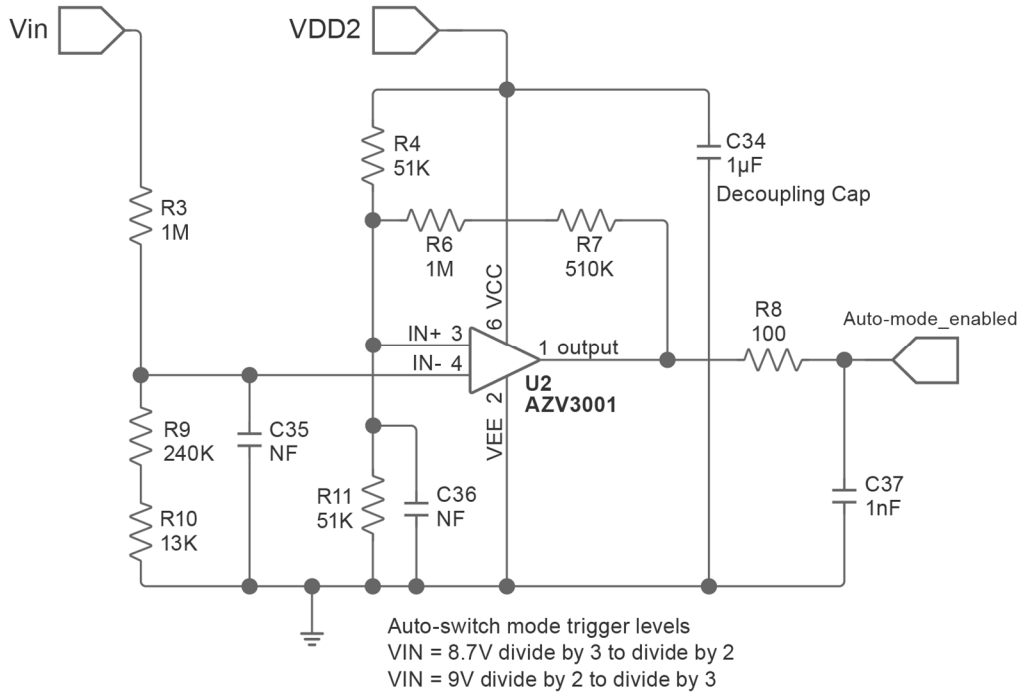

Figure 30. Auto-switch Mode Circuit Schematic

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Application Circuit Part List

Table 7 lists the recommended components.

Table 7. Recommended Components

Reference	Value	Description	Part Number
Required components			
C1	1 µF	CAP CER 1UF 6.3V X7R 0402	GRM155R70J105KA12D
C4,C5,C6,C7,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21	10 µF	CAP CER 10UF 25V X5R 0603	GRM188R61E106KA73D
C8,C9	100 nF	CAP CER 0.1UF 100V X5R 0402	GRM155R62A104KE14D
C22,C23	2.2 µF	CAP CER 2.2UF 16V X6S 0402	GRM155C81C225ME15D
		CAP CER 2.2UF 25V X5R 0402	GRM155R61E225KE11D
C24,C25,C26,C27,C28,C29,C30,C31,C32,C33	10 µF	CAP CER 10UF 6.3V X5R 0603	GRM188R60J106ME47D
D1	–	DIODE ZENER 6.2V 500MW SOD523	MM5Z6V2T1G
L1	100 nH	IND, SMD, Thin Film Inductor, AEC-Q200, 100 nH, 9000 µohm, 12 A, 2.5 mm x 2 mm x 1.2 mm, TFM-ALMA	TFM252012ALMAR10MTAA
R1,R2	499k	RES 499K OHM 1% 1/10W 0603	RC0603FR-07499KL
U1	PE25203	PE25203 Divide-by-2 and -3, 4A Charge Pump, Capacitor Divider	PE25203
Optional components for evaluation purposes			
C34	1 µF	CAP CER 1UF 6.3V X7R 0402	GRM155R70J105KA12D
R13	499 kΩ	RES 499K OHM 1% 1/10W 0603	RC0603FR-07499KL
C35,C36	33 0pF	CAP CER 330PF 50V C0G/NP0 0402	GRM1555C1H331JA01D
C37	1 nF	CAP CER 1000PF 50V C0G/NP0 0402	GRM1555C1H102JA01D
C38	100 µF	CAP ALUM 100UF 20% 25V RADIAL	EEUHD1E101B
R3,R6	1M	RES 1M OHM 1% 1/10W 0603	RC0603FR-071ML
R4,R11	51K	RES 51K OHM 1% 1/10W 0603	RC0603FR-0751KL
R5	0Ω	RES 0 OHM JUMPER 1/10W 0603	RC0603FR-070RL
R7	510K	RES 510K OHM 1% 1/10W 0603	RC0603FR-07510KL
R8	100	RES 100 OHM 1% 1/10W 0603	RC0603FR-07100RL
R9	240K	RES 240K OHM 1% 1/10W 0603	RC0603FR-07240KL
R10	13K	RES 13K OHM 1% 1/10W 0603	RC0603FR-0713KL
R12	10k	RES 10K OHM 1% 1/10W 0603	RC0603FR-0710KL
U2	–	IC COMPARATOR X2-DFN1410-6	AZV3001FZ4-7
LED1	–	LED RED CLEAR SMD	150060SS75020
Q1	–	TRANS NPN DARL 100V 0.9A SOT23-3	FMMT634TA
VIN +,VIN -, VOUT+,VOUT-	TERMINAL	CONN BANANA JACK SOLDER	575-4
H1,H2,H3,H4	HEADER	CONN HEADER VERT 3POS 2.54MM	PREC003SAAN-RC
H5,H6,H7	HEADER	CONN HEADER VERT 2POS 2.54MM	PREC002SAAN-RC

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SI -, SO -, GND	TP	PC TEST POINT MULTIPURPOSE BLACK	5011
EN,MODE,PGOOD,FF,VDD,FREQ,EXT_VDD	TP	PC TEST POINT MULTIPURPOSE WHITE	5012
GND1,GND2,GND3,GND4,GND5	TP SMT	PC TEST POINT COMPACT SMT	5016
CN1	–	CONN HEADER VERT 4POS 2.5MM	DF1BZ-4P-2.5DSA

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Technical Resources

Additional technical resources are available for download in the Products section at www.psemi.com. These include the product specification datasheet, S-parameters, zip file, evaluation kit schematic, bill of materials, material declaration form, and PC-compatible software file.

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