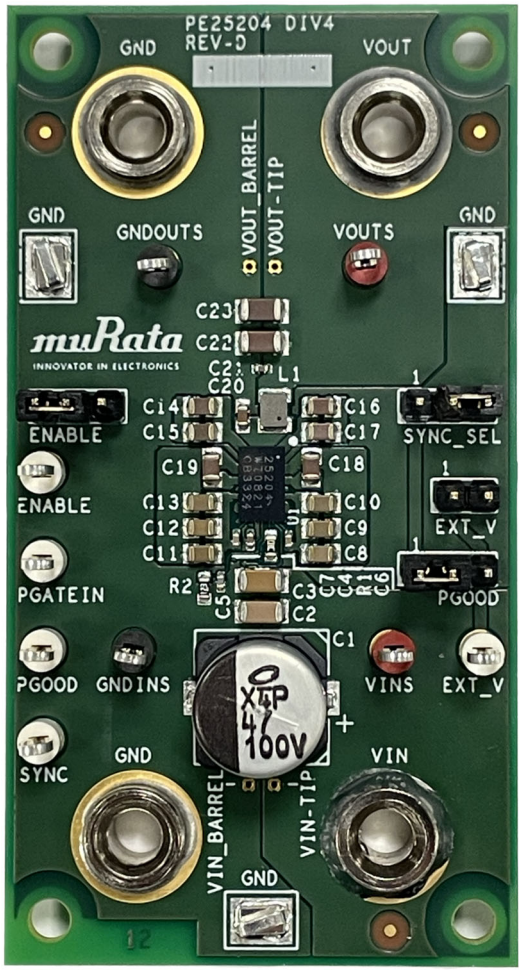
PE25204

Evaluation Kit User's Manual

48 V_{IN}, Divide-by-4, 6A Charge Pump, Capacitor Divider



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Introduction

The **PE25204** is an ultra-high-efficiency charge pump solution that divides down an input voltage by four and delivers up to 72W output at up to 96.8% peak efficiency. The PE25204 can also be used in parallel to increase output power. The PE25204 supports an input voltage range of 18V to 60V and is available in a WLCSP package.

Evaluation Kit Overview

The PE25204 evaluation kit (EVK) is a hardware platform that allows customers to easily test the step-down DC-DC converter. The PE25204 EVK can be operated with an 18V to 60V input voltage, and the input is divided by four and delivers up to 6A.

By default, the EVK is equipped with a 10KΩ resistor R2, which sets the minimum operating input voltage to 18V. To raise the minimum operating input voltage, change the value of resistor R2 as described in Changing the UVLO Value on page 11.

Table 1 lists the PE25204 EVK electrical parameters. For more information, see the *PE25204 Data Sheet*.

Table 1. PE25204 Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max(1)	Unit
Input voltage range	V_{IN}	–	18	48	60	V
Nominal output voltage	V_{OUT}	I_{OUT} = 0A	–	V_{IN}/4	–	V
Output power delivered(1)	P_{OUT}	V_{IN} = 48V	72	–	–	W
Output current delivered	–	SYNC_SEL=GND	6	–	–	A
Nominal clock frequency	–	Divided by 2 internally for charge pump frequency.	–	545	–	kHz
Input SYNC frequency	f_{SYNC}	TA = +25 °C ILOAD = 6A(2)	300	–	600	kHz
Peak efficiency	–	–	–	96.8	–	%

Notes:
1. The maximum output power depends on the system thermal solution and the ambient temperature.
2. External component changes are necessary if operating outside default switching frequency.

Evaluation Kit User's Manual Overview

This *PE25204 Evaluation Kit (EVK) User's Manual* includes information about the hardware required to control and evaluate the functionality of the DC-DC converter.

Evaluation Kit Contents and Requirements

Kit Contents

Table 2 lists the hardware required to evaluate the DC-DC converter.

Table 2. EVK Contents

Quantity	Description	Part Number
1	PE25204 DC-DC converter evaluation board assembly	EK25204-01

Hardware Requirements

To evaluate the performance of the evaluation board, the following equipment is required:

- Bench DC power supply capable of providing up to 60V at up to 3A
- DC load (power resistors or electrical load)
- Four high-accuracy digital multimeters
- DC power and sense leads
- Optional: Four-channel oscilloscope with probes to view waveforms

Warning: The PE25204 DC-DC converter EVK contains components that could be damaged by exposure to voltages higher than the maximum specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals, or to signal inputs and outputs.

Before you connect the EVK to the source power supply, verify that the power supply is off. Connecting the EVK to a live power supply could induce failures.

Quick Start Guide

Quick Start Overview

The evaluation board is designed to ease your evaluation of the PE25204 DC-DC converter. This section guides you through the hardware configuration and the startup process.

Evaluation Board Overview

The evaluation board includes the following:

- Input and output terminals
- PCB jumpers
- Sense points

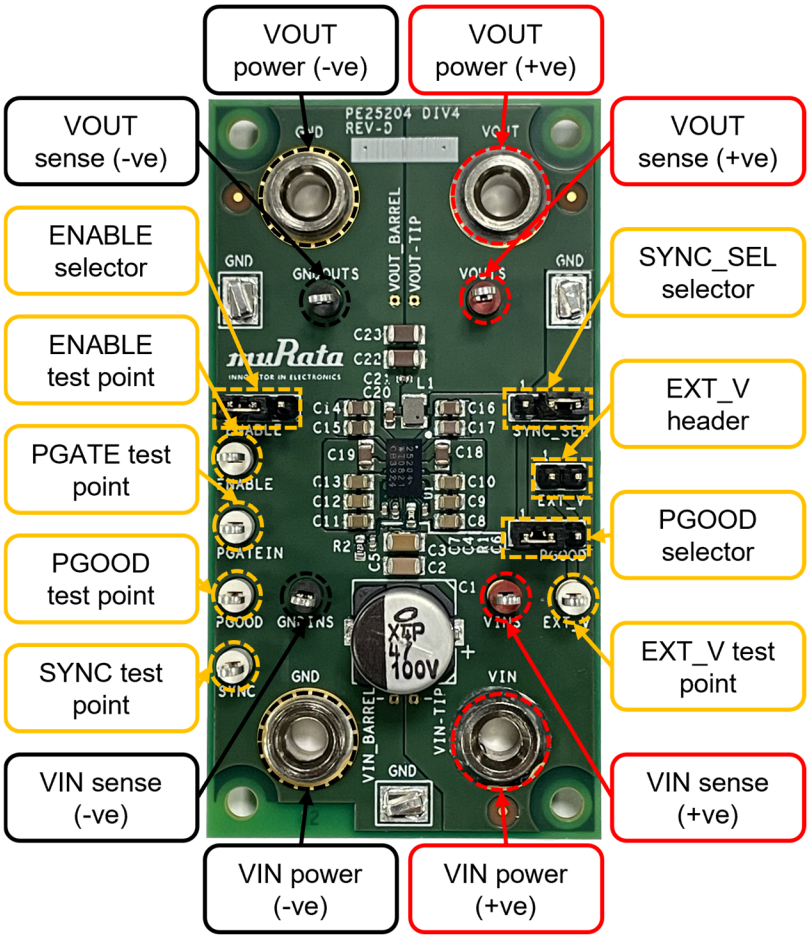

Figure 1. PE25204 Evaluation Board Assembly

Input and Output Terminals

The PE25204 EVK includes the following terminals, as shown in Figure 1:

- Input terminals VIN power (+ve) and VIN power (-ve), which receive input power from a connected bench DC power supply.
- Output terminals VOUT power (+ve) and VOUT power (-ve), which supply output power to a DC load.

PCB Headers

The PE25204 EVK has two types of PCB headers:

- Supply (2-pin) header, which supplies an external voltage to the EVK.
- Configuration (3-pin) headers, which configure the EVK.

Supply Header

The PE25204 EVK has a supply (2-pin) header EXT_V, as shown in Figure 1. The EXT_V header supplies an external pull-up power good (PGOOD) voltage between 3.3V and 5V to the EVK. Table 3 lists the EXT_V header functions and how to properly connect its pins to supply an external pull-up PGOOD voltage.

To successfully pull up the PGOOD pin of the PE25204 with the supplied external pull-up PGOOD voltage, follow these steps.

1. Connect and supply an external pull-up PGOOD voltage to the EVK before you power up the EVK.
2. Verify that the PGOOD selector, as indicated in Figure 1, is fitted with a jumper configured to short pin 2 and pin 3.

Do not use a jumper to short the pins of the EXT_V header.

Table 3. Supply (2-pin) Header Functions

Header	Function	Pin Function	
		Pin 1	Pin 2
EXT_V	Supplies an external pull-up PGOOD voltage to the PE25204 EVK(*)	Connect pin 1 to the positive terminal of the external pull-up PGOOD voltage.	Connect pin 2 to the negative terminal of the external pull-up PGOOD voltage.
Note: * Before you supply an external voltage, power off the EVK.			

Configuration Headers

Before you apply power to the EVK, verify that the ENABLE, SYNC_SEL, and PGOOD selectors shown in Figure 1 are properly fitted with the jumpers for your preferred configuration. Table 4 lists the configuration headers, the associated jumper configurations, and the recommended jumper configurations for a quick evaluation. Before you change any jumper configurations, always remove the input power.

Table 4. 3-Pin Configuration Jumper Functionalities, Configurations, and Recommendations

Jumper	Function	Jumper Configuration			
		Short pins 1 and 2	Short pins 2 and 3	Open all pins	Recommendation
ENABLE	Enables or disables the PE25204 through its EN input pin. Logic high enables the PE25204. Logic low disables the PE25204.	Enabled. EN pin is tied to V_{IN}.	Disabled. EN pin is tied to GND.	N/A	Short pins 1 and 2.
SYNC_SEL	Sets the PE25204 SYNC pin as an output for the internal clock signal or an input for an applied external clock signal.	N/A	Internal clock output. SYNC_SEL pin is tied to GND.	External clock input. SYNC pin is open for input	Short pins 2 and 3.
PGOOD	Pulls up the PE25204 PGOOD pin to the internal VDD or an applied external PGOOD pull-up voltage.	PGOOD is pulled up to VDD.	PGOOD is pulled up to EXT_V.	N/A	Short pins 1 and 2.

Sense Points

To ensure accurate measurement of the input and output voltages, use the PE25204 EVK sense (+ve) and sense (-ve) test points for the VIN and VOUT voltages, as shown in Figure 1.

Table 5 lists the PE25204 EVK test point information. These test points make it easy to capture the waveforms of critical signals.

Table 5. Test Point Descriptions

Test Point (TP)	Description
VIN sense (+ve) (VINS)	Positive input voltage TP to measure V_{IN}
VIN sense (-ve) (GNDINS)	Negative or ground input voltage TP to measure V_{IN}
VOUT sense (+ve) (VOUTS)	Positive output voltage TP to measure V_{OUT}
VOUT sense (-ve) (GNDVOUTS)	Negative or ground output voltage TP to measure V_{OUT}
ENABLE	Status of the enable (EN) signal from the PE25204 EN pin
PGOOD	Status of the power good (PGOOD) signal from the PE25204 PGOOD pin
EXT_V	External pull-up PGOOD voltage TP to measure external voltages between 3.3V and 5V to successfully pull-up PGOOD.
SYNC	Status of the SYNC internal clock output signal from the PE25204 SYNC pin. Apply and measure an external clock input signal to the PE25204 SYNC pin.
PGATEIN	External P-type FET's gate drive voltage TP to measure the PE25204 PGATEIN gate drive voltage of an optional external P-type input disconnect FET switch.
GND (GND, GND, GND)	0V ground reference TPs

EVK Connection

Connect the EVK and the DC power and sense leads as shown in Figure 2.

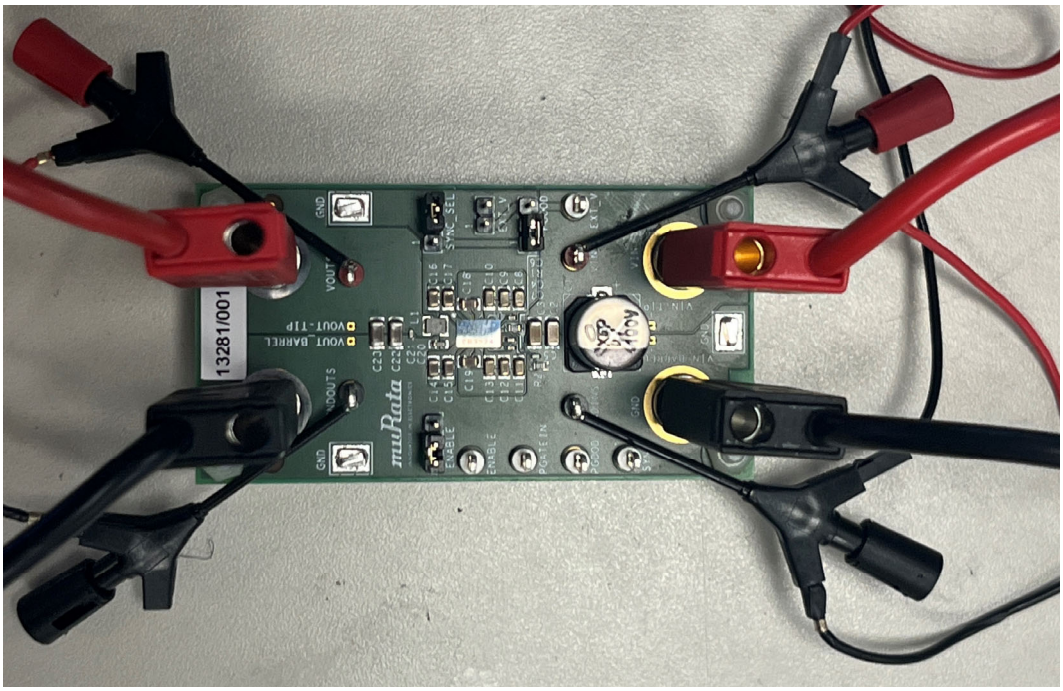

Figure 2. EVK Lead Connections

Voltage-only Measurement Connections

To only measure the voltage, connect the EVK to the equipment as shown in Figure 3.

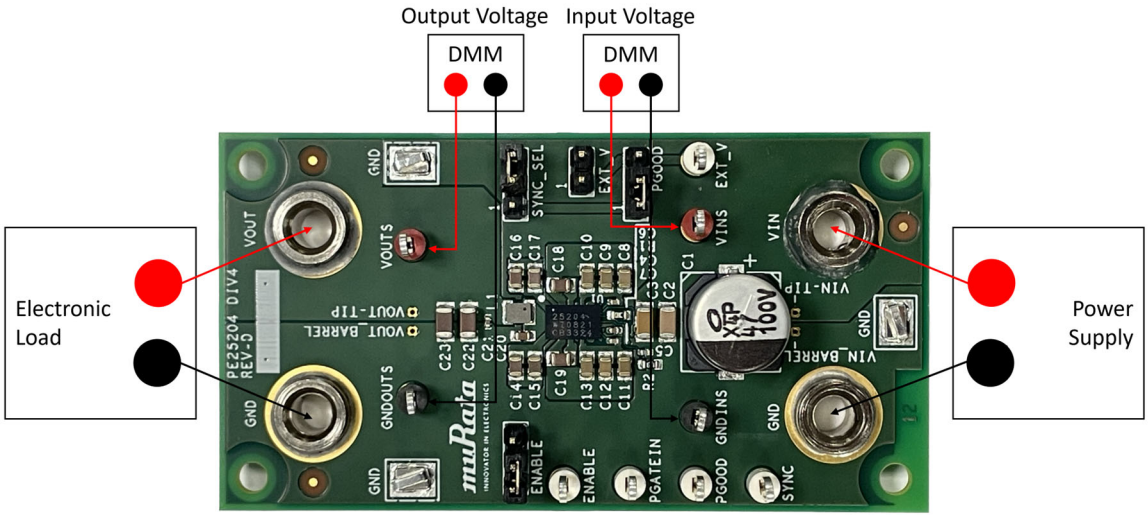

Figure 3. Voltage-only Measurement Connections

If the power supply is capable of 4-wire sense, use the VINS and GNDVINS to sense the input voltage at the power supply.

Voltage and Current Measurement Connections

To measure the voltage and current, connect the EVK to the equipment as shown in Figure 4.

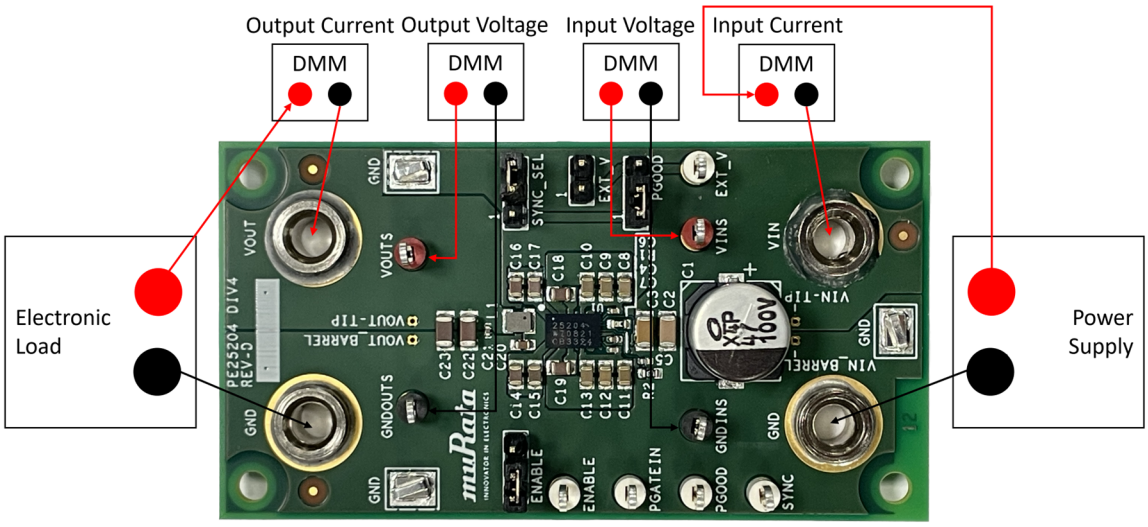

Figure 4. Voltage and Current Measurement Connections

External Pull-up of PGOOD Voltage Connections

An external voltage can be supplied to the EVK to pull up the PE25204 PGOOD pin rather than the internal VDD through the EXT_V supply header. To supply and measure the external pull-up of the PGOOD voltage, connect the EVK to the equipment as shown in Figure 5 and configure the PGOOD selector with the jumper as shown.

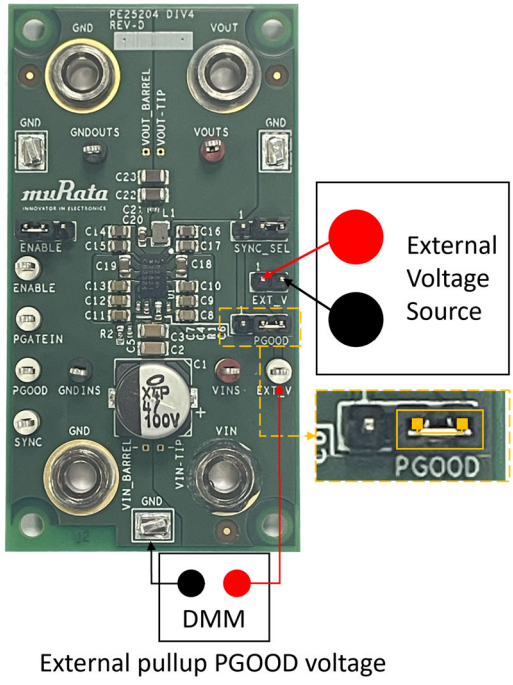

Figure 5. EVK Equipment Connections for External Pull-up PGOOD Voltage Supply and Measurement

Hardware Operation

The section describes the general guidelines for operating the hardware evaluation board. To configure the EVK to achieve optimal performance, follow these steps:

1. Before you power up the EVK, configure the ENABLE, SYNC_SEL, and PGOOD selectors by fitting the jumpers in the recommended position shown in Figure 6 and listed in Table 3.
2. Optional: If you prefer, supply and measure an external voltage between 3.3V and 5V to pullup the PGOOD pin of PE25204 instead of using the internal VDD of the IC by connecting the EVK as shown in Figure 5 and reconfiguring the PGOOD selector as shown in Figure 5.
3. Connect the DC power and sense leads to the EVK as shown in Figure 2, then connect the EVK to the power and measuring equipment as shown in Figure 4. Minimize the length of the connections.
4. Apply an input voltage to the EVK through the connected DC bench power supply.
5. Apply a load current to the EVK after it successfully starts up through the connected electronic load.

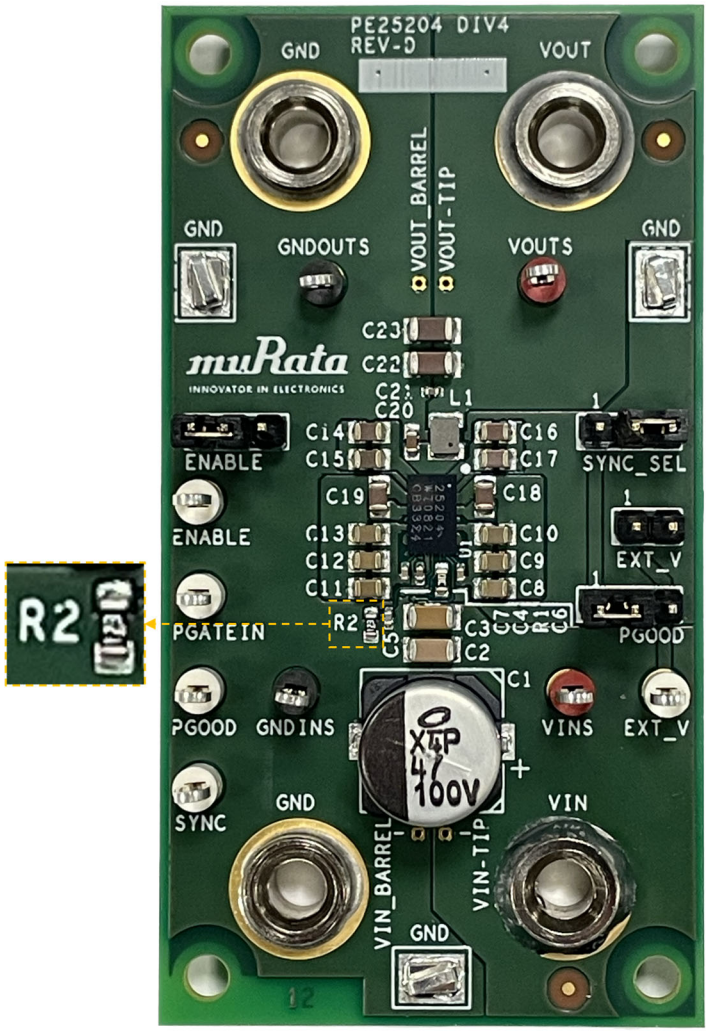

Figure 6. Recommended Jumper Positions

EVK Startup

When you start the EVK, start it with no load.

If you start the EVK with a load, it might not start due to the soft-start current limit.

Changing the UVLO Value

Resistor R2 sets under-voltage lockout of the device. The reference number is labeled in white text. See Figure 7.

UVLO (V) = RUV (KΩ) × 1.51.

Below is an example of implementing the above formula when RUV (or R2) = 10KΩ:

UVLO (V) = 10 × 1.51 ⇒ UVLO (V) = 15.1V.

Recommended resistors must be 1% or better of the resistance value of the E96 series. Use the closest resistor value needed between 10KΩ to 38.3KΩ. The current fitted value is 10KΩ.

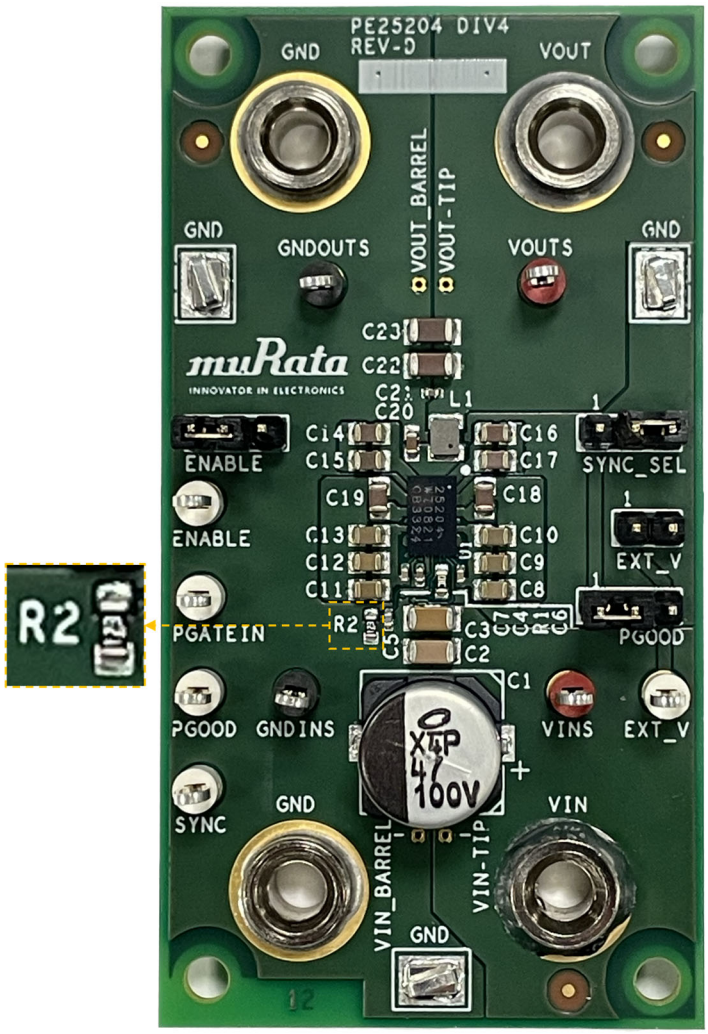

Figure 7. Resistor R2 Location

Test Results

Figure 8–Figure 11 show the typical performance of the PE25204 evaluation board.

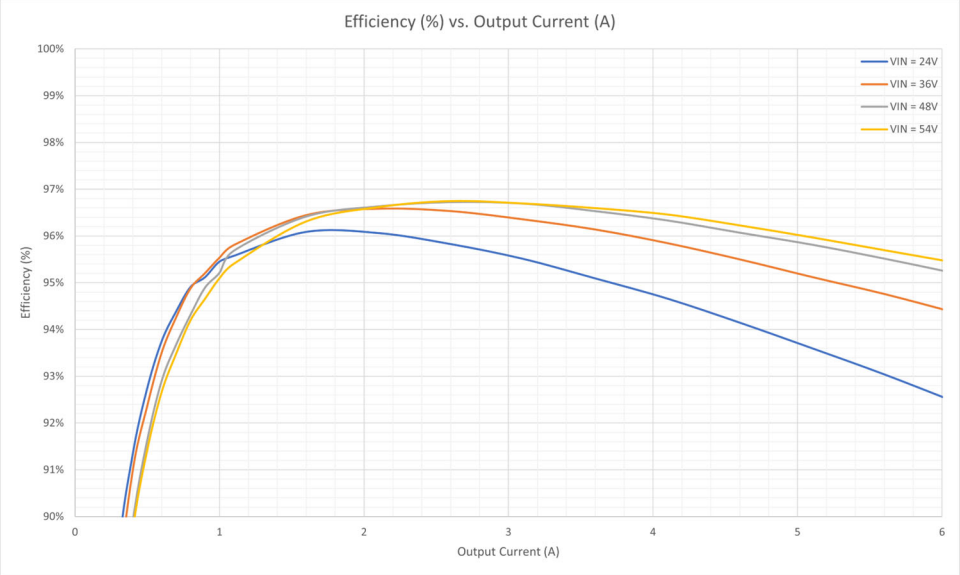

Figure 8. Efficiency (%) vs. Output Current (A)

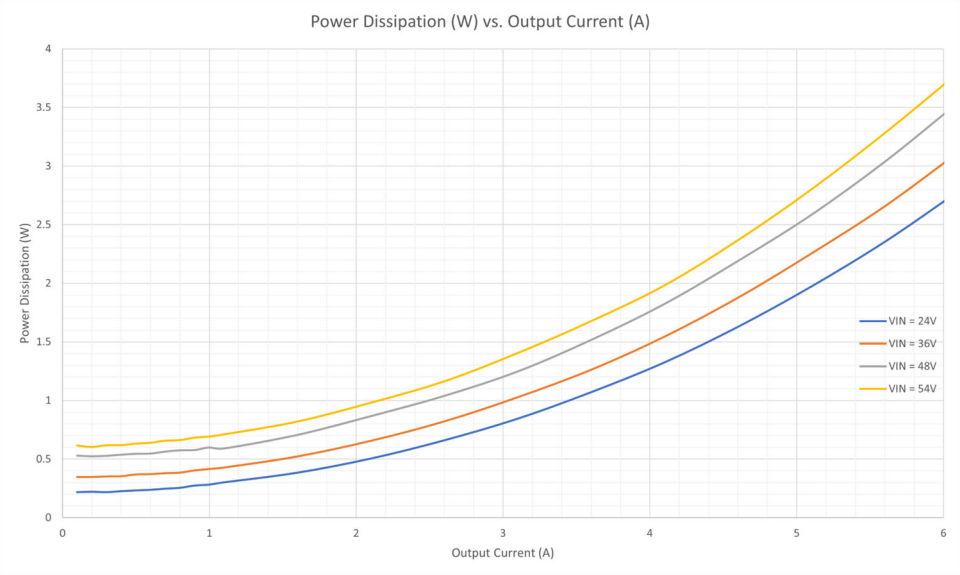

Figure 9. Power Loss/Dissipation (W) vs. Output Current (A)

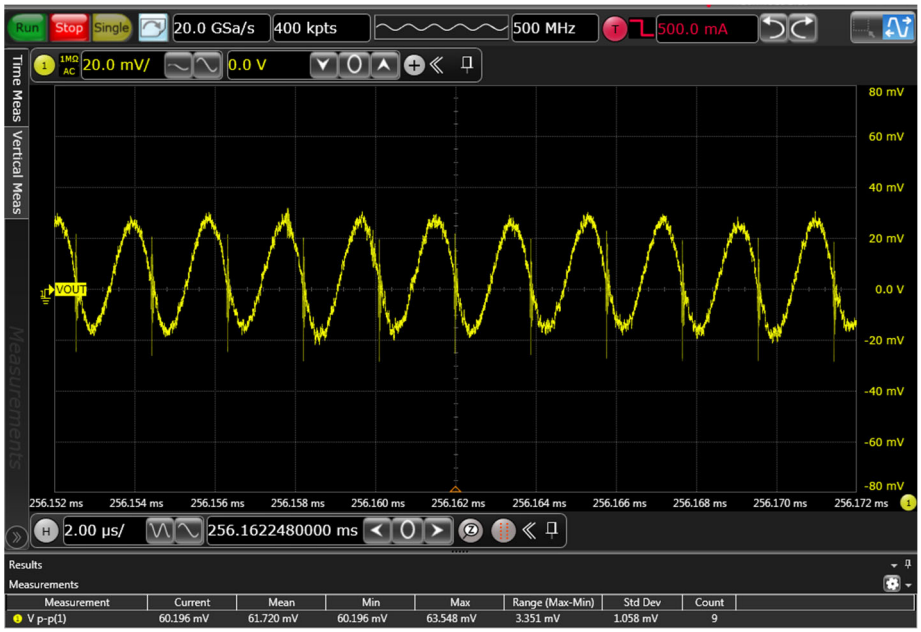

Figure 10. Output Ripple (VIN=48V, IOUT=6A) with Added 44 µF Output Capacitance through 2×22 µF Capacitors

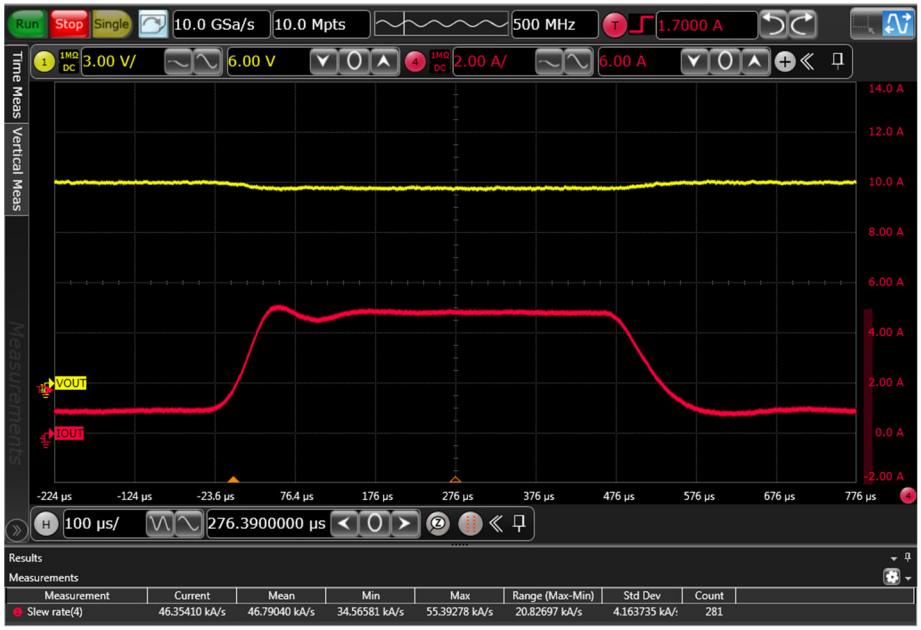

Figure 11. Load Transient Response (VIN=48V, 1 – 5A Load Step, 50A/ms) with Added 44 µF Output Capacitance through 2×22 µF Capacitors

Information

PE25204 EVK PCB Layout

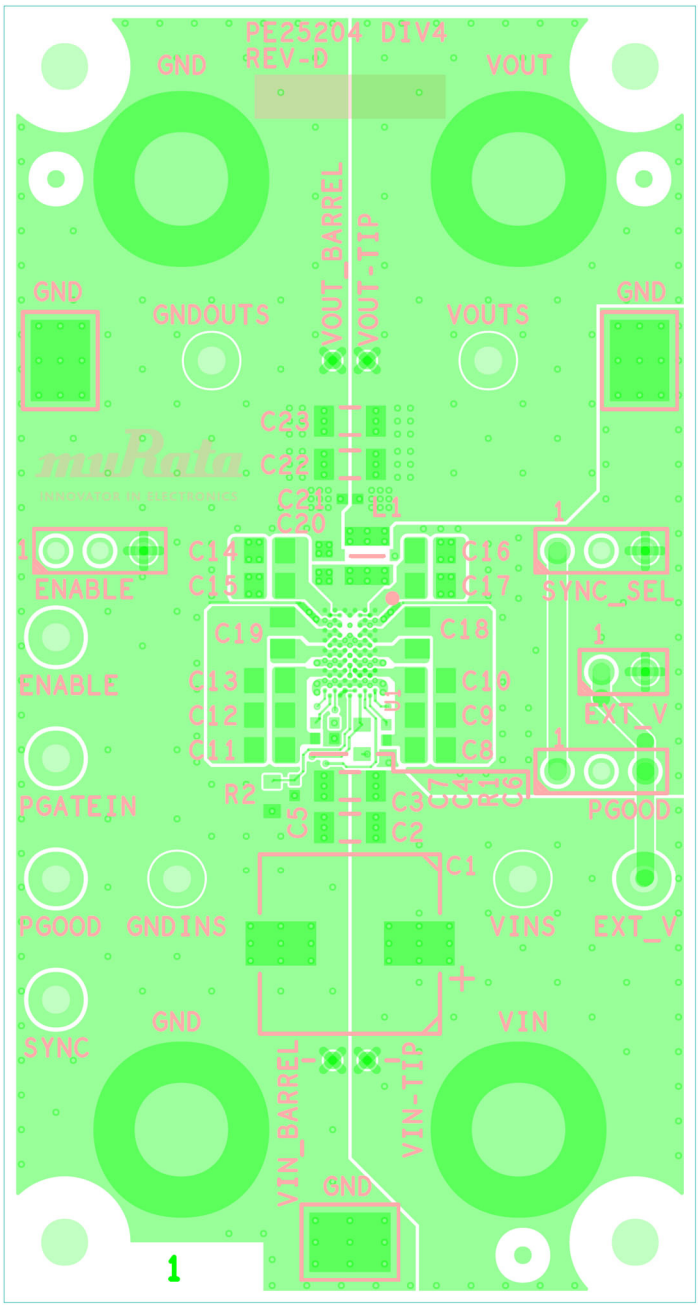

Figure 12. Evaluation Board Layout (Top Layer)

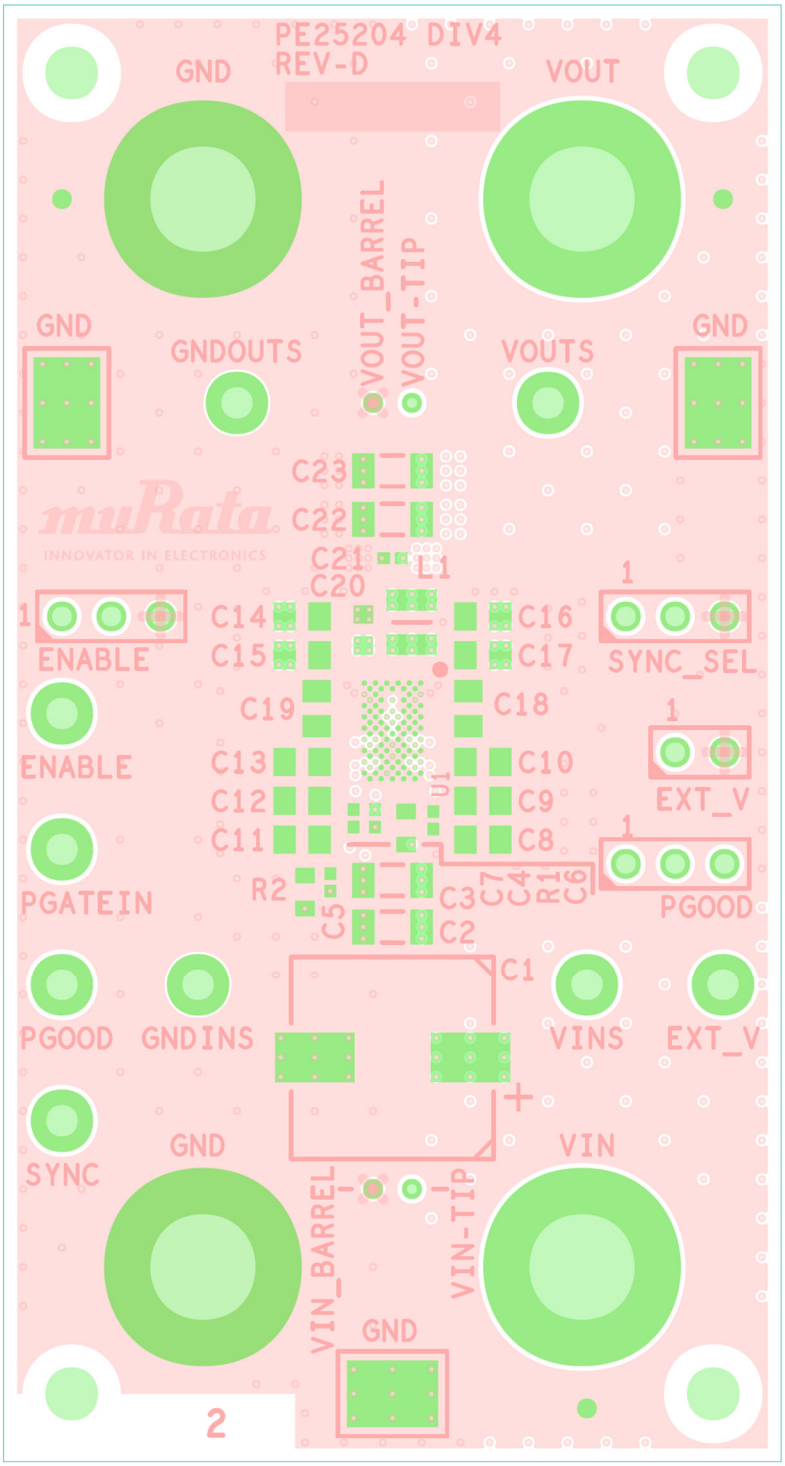

Figure 13. Evaluation Board Layout (Inner Layer 1)

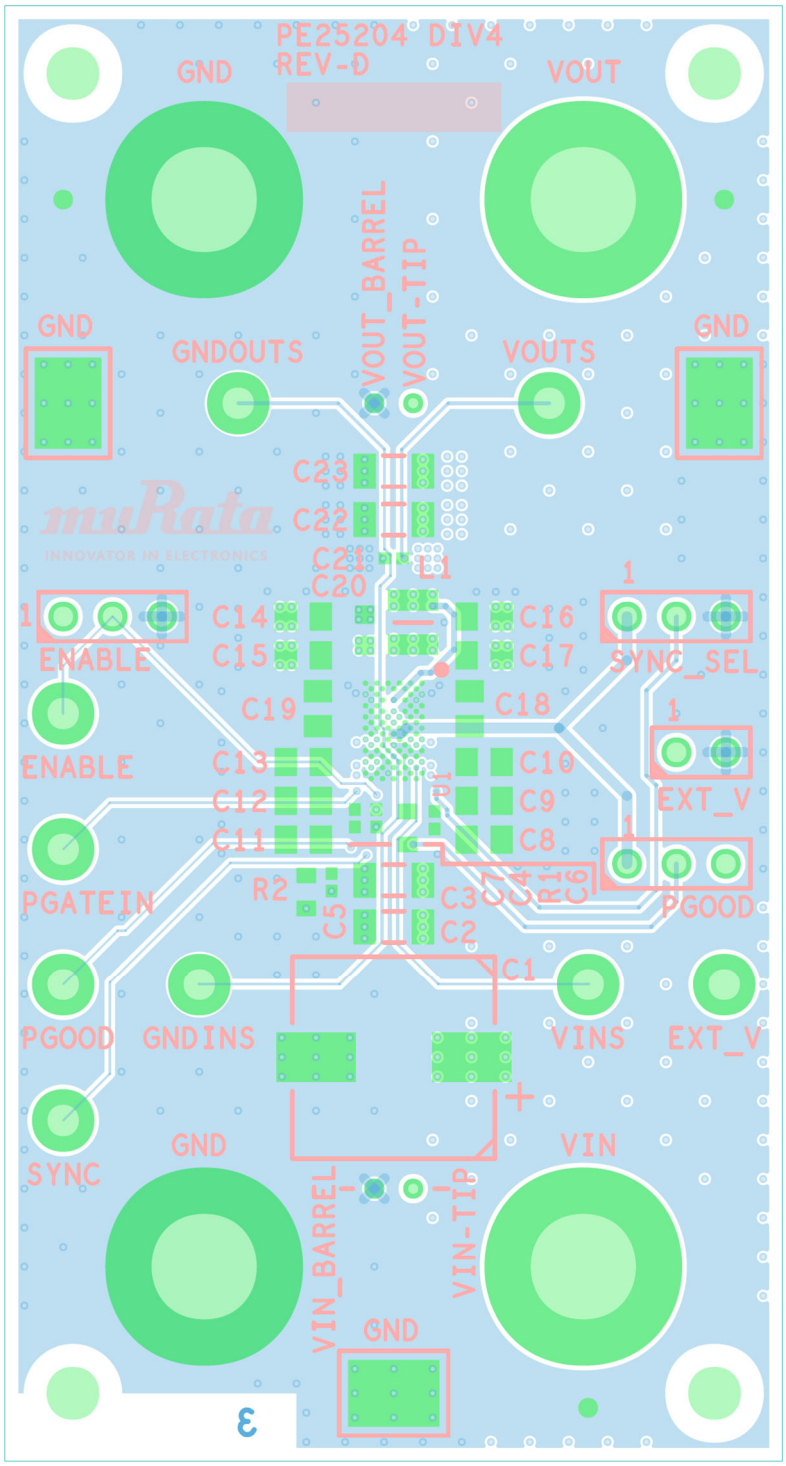

Figure 14. Evaluation Board Layout (Inner Layer 2)

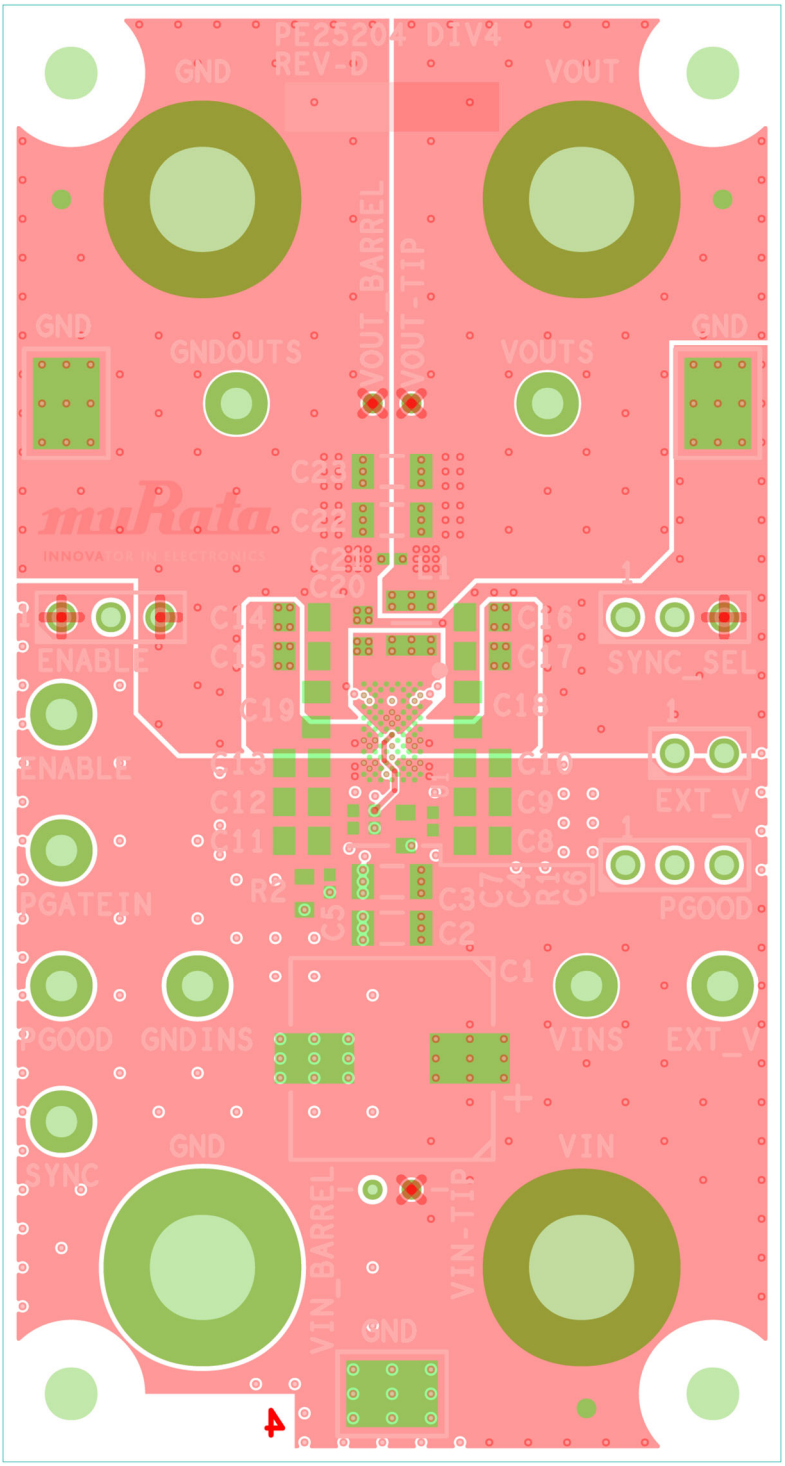

Figure 15. Evaluation Board Layout (Bottom Layer)

PE25204 Functional Block Diagram

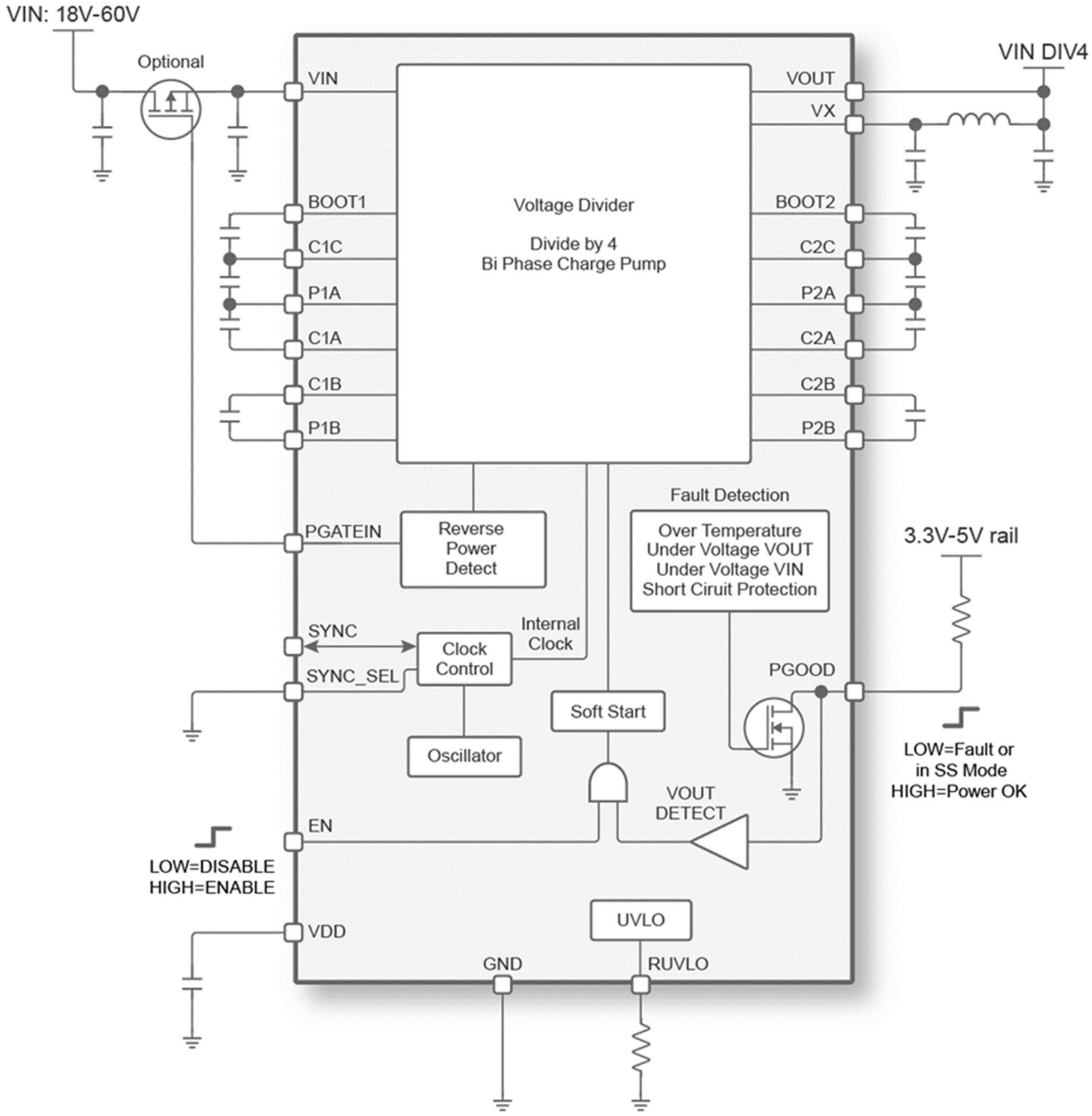

Figure 16. PE25204 Functional Block Diagram

PE25204 EVK PCB Schematic

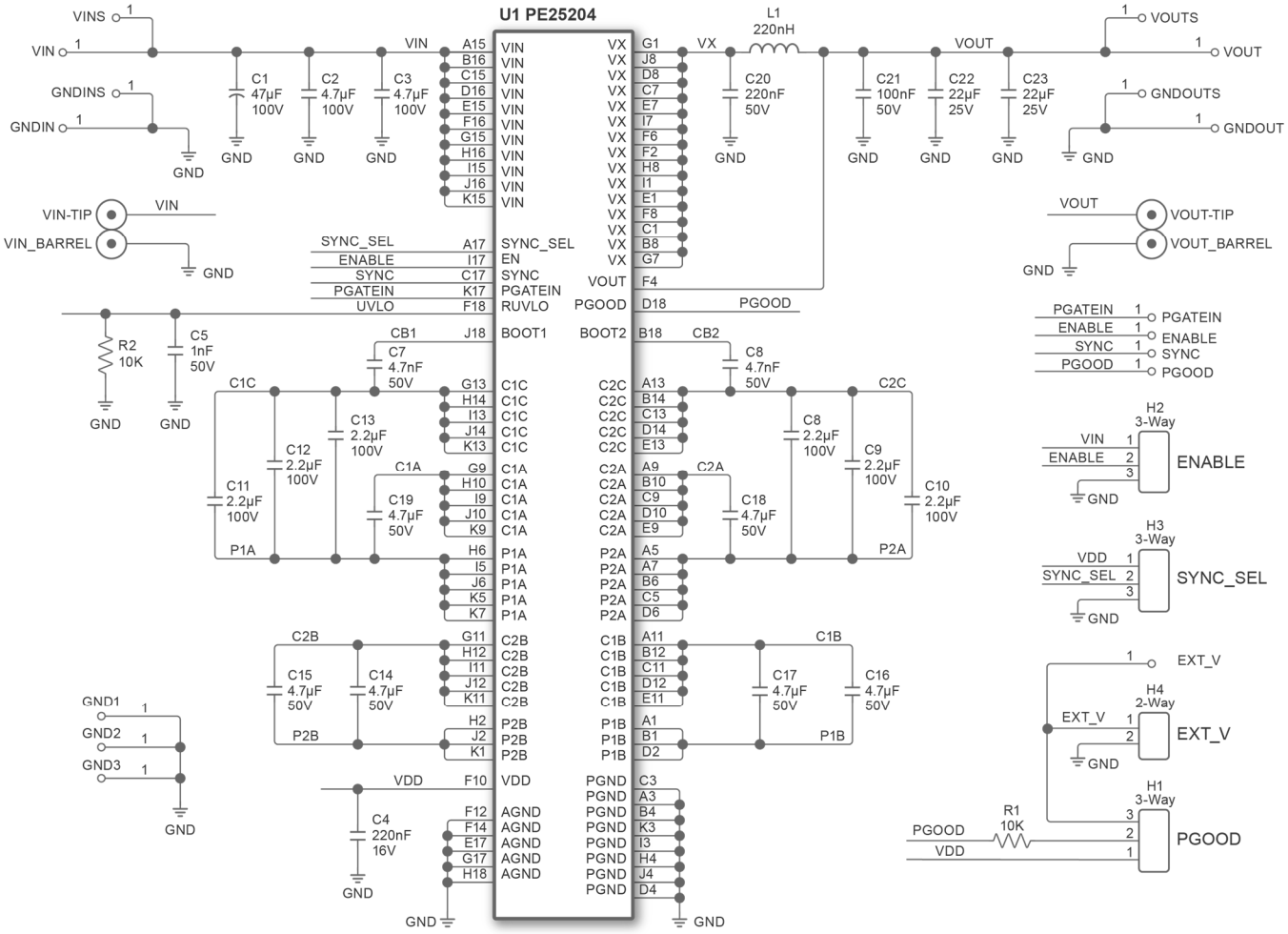

Figure 17. PE25204 Evaluation Board Schematic

PE25204 EVK BOM

Table 6. PE25204 EVK BOM

Reference	Value	Description	Part Number
C1	47 µF	CAP ALUM 47µF 20% 100V SMD	UUX2A470MNL1GS
C2, C3	4.7 µF	4.7 µF ±20% 100V Ceramic Capacitor X7R 1206 (3216 Metric)	GRM31CZ72A475ME11L
C4	220 nF	0.22 µF ±10% 16V Ceramic Capacitor X7R 0402 (1005 Metric)	GRM155R71C224KA12D
C5	1 nF	CAP CER 1000pF 50V C0G/NP0 0402	GRM1555C1H102JA01D
C6, C7	4.7 nF	CAP CER 4.7nF 50V R 0402	GRM155R11H472KA01D
C8, C9, C10, C11, C12, C13	2.2 µF	CAP CER 2.2µF 100V X7T 0805	GRM21BD72A225KE01L
C14, C15, C16, C17, C18, C19	4.7 µF	CAP CER 4.7µF 50V X7S 0805	GRM21BC71H475KE11L
C20	220 nF	0.22 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	GRM188R71H224KAC4D
C21	100 nF	0.1 µF ±10% 50V Ceramic Capacitor X7R 0402 (1005 Metric)	GRM155R71H104KE14D
C22, C23	22 µF	CAP CER 22µF 25V X7S 1206	GRM31CC71E226ME15L
L1	220 nH	IND, SMD, fixed inductors 220 nH, 6000 mA, 10 mΩ, 1008 (2520 Metric)	HMLQ25201B-R22MSR-01
		Power Inductor (SMD), Wirewound, 220 nH, 5 A, Shielded, 7.2 A, DFE252010F	DFE252010F-R22M=P2
U1	PE25204	PE25204 IC, PE25204, WLCSP-BGA, pSemi IC	PE25204
R1, R2	10 KΩ	10K RES, SMD, thick film, 10K, +/-1%, 1/10W, 0603	RC0603FR-0710KL
H1, H2, H3	HEADER	CONN HEADER VERT 3POS 2.54MM	PREC003SAAN-RC Alternative: 61300311121
H4	HEADER	CONN HEADER VERT 2POS 2.54MM	PREC002SAAN-RC Alternative: 61300211121
GNDOUTS, GNDINS	TP	PC TEST POINT MINIATURE BLACK	5011
VOUTS, VINS	TP	PC TEST POINT MINIATURE RED	5010
PGATEIN, EN, SYNC, PGOOD, EXT_V	TP	PC TEST POINT MINIATURE WHITE	5012
GNDOUT, GNDIN, VOUT, VIN	TERMINAL	CONN BANANA JACK SOLDER	575-4
GND1, GND2, GND3	TP SMT	PC TEST POINT COMPACT SMT	5016

PE25204 Parallel Operation Pin Connections

Multiple PE25204 devices can be operated in parallel. The pin connections for parallel operation are slightly different from single operation, as shown in Figure 18.

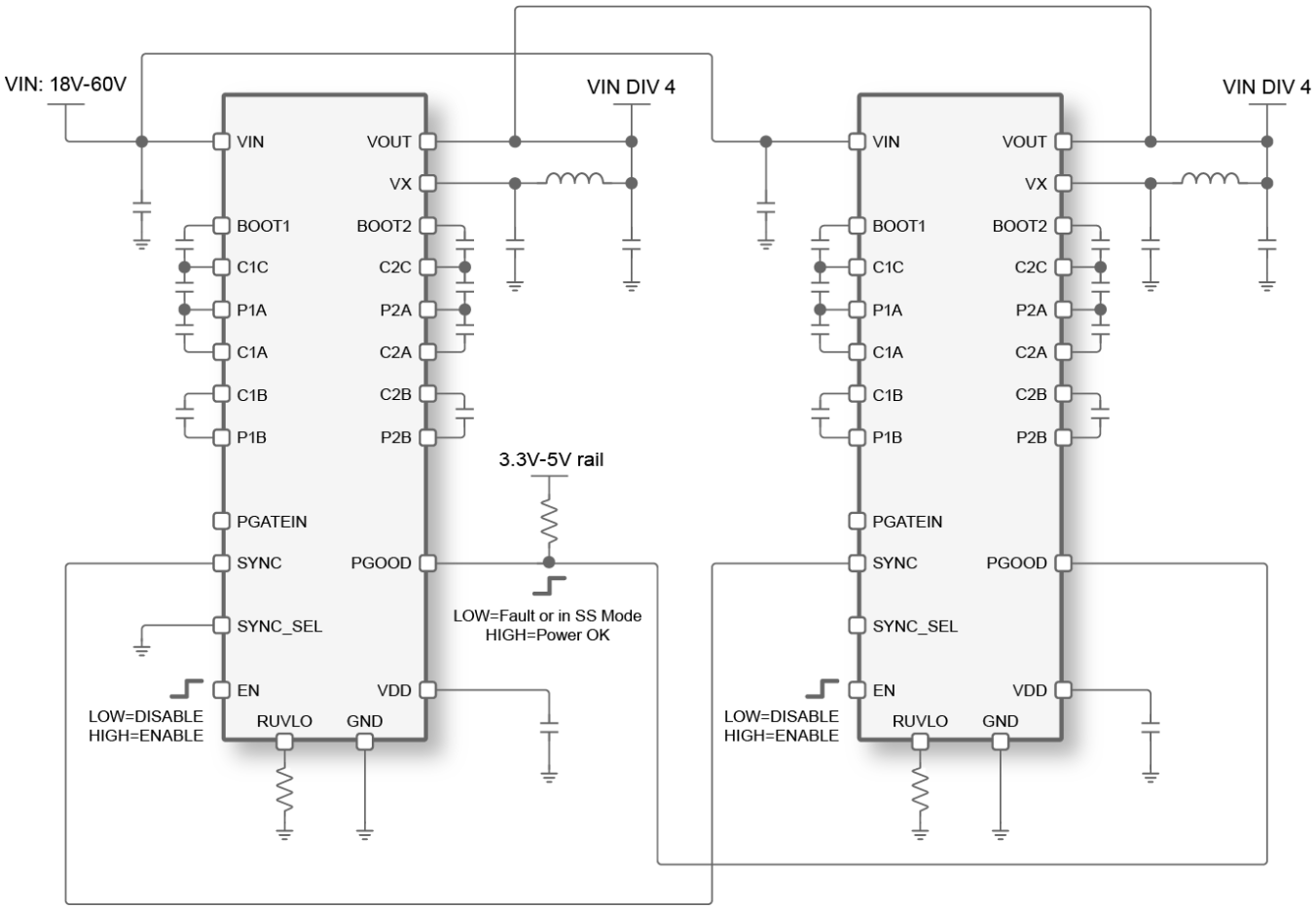

Figure 18. Master and Slave Operation in Parallel

Combine the PGOOD outputs of all PE25204 devices in a wired OR configuration. Do not switch on the load following the charge pumps until the common PGOOD signal goes high. Immediately switch off the load if any of the PGOOD outputs switch low after startup.

Leave the SYNCSEL pin(s) on all but the first PE25204 device floating. On the first PE25204 device, connect the SYNCSEL pin to GND so that this PE25204 device provides the clock to the other PE25204 devices connected in parallel.

The resistor connected to the RUVLO pins of all the PE25204 devices must be the same and equal.

Technical Resources

Additional technical resources are available for download in the Products section at www.psemi.com. These include the product specification datasheet, S-parameters, zip file, evaluation kit schematic, bill of materials, material declaration form, and PC-compatible software file.

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