PE25208

Parallel Evaluation Kit User's Manual

48 V_{IN} Divide-by-2 and -3, 15A Charge Pump, Capacitor Divider

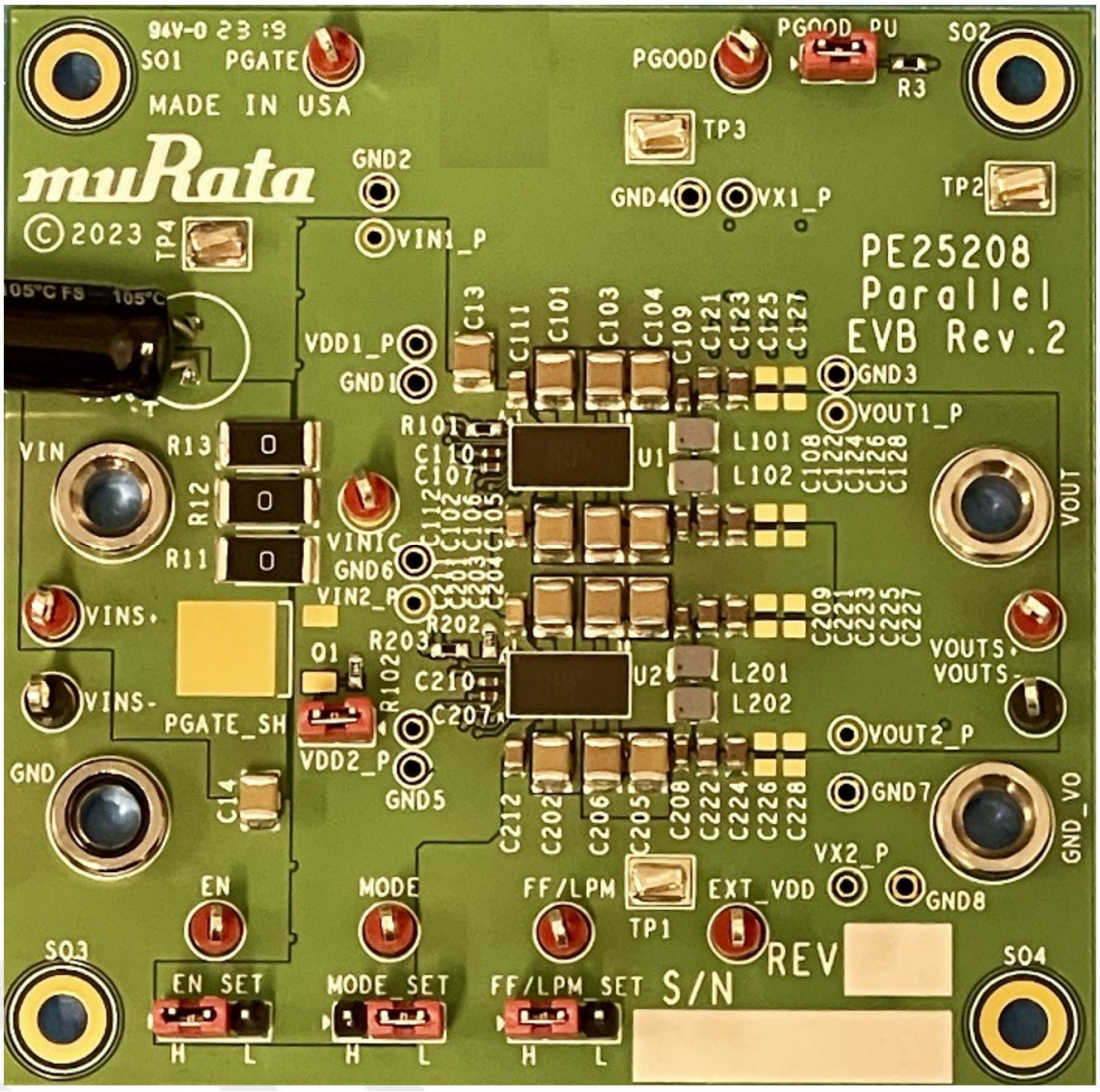

Table of Contents

Introduction

The PE25208 parallel evaluation kit (EVK) is a hardware platform designed to easily test two PE25208 devices operating in parallel.

The PE25208 is an ultra-high efficiency charge pump and capacitor divider that you can configure to divide an input voltage by 2 or 3 and operates in parallel with an additional PE25208. In parallel operation, the two PE25208 devices can collectively deliver up to 240W output at up to 98.2% peak efficiency. The PE25208 is available in a wafer-level chip scale package (WLCSP) and supports the following input voltage ranges:

- 18V to 45V in divide-by-2 mode
- 18V to 60V in divide-by-3 mode

Evaluation Kit Overview

The EVK provides the following:

- Mounted input and output capacitors to accommodate the entire range of input and output voltages
- Test and sense points to provide accurate measurement and monitoring of efficiency, power dissipation, load regulation, and primary signals
- Control headers and jumpers and unfitted component footprints to easily configure the PE25208 and implement an optional input disconnect P-channel FET switch

For more PE25208 application information, see the *PE25208 Data Sheet*.

Document Overview

This *PE25208 Parallel Evaluation Kit (EVK) User's Manual* includes information on the correct use of the parallel EVK and describes the featured terminals, test points, and jumpers. The EVK features two PE25208 devices operating in parallel, which you can configure for divide-by-2 or divide-by-3 modes. You can also configure the EVK for fixed-frequency or low-power mode operations. The EVK operates across the entire PE25208 input voltage range.

This document describes the *parallel* PE25208 EVK. Do not reference it for the single PE25208 EVK.

Performance Summary

Table 1 lists the electrical parameters of the PE25208 parallel EVK and only applies to two PE25208 devices operating in parallel. For details about single PE25208 operation, see the *PE25208 Data Sheet*.

Table 1. Performance Summary for Two PE25208 Devices Operating in Parallel

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input voltage range	V_{IN}	Divide-by-3 mode (DIV3)	18	48	60	V
		Divide-by-2 mode (DIV2)	18	36	45	V
Nominal output voltage	V_{OUT}	DIV3, I_{OUT} = 0A	–	$V_{IN}/3$	–	V
		DIV2, I_{OUT} = 0A	–	$V_{IN}/2$	–	V
Maximum output power(*)	P_{OUT}	V_{IN} = 48V, DIV3	240	–	–	W
		V_{IN} = 36V, DIV2	180	–	–	W
Maximum output current	I_{OUT}	DIV3	15	–	–	A
		DIV2	10	–	–	A
Switching frequency	f_{SW}	–	–	300	–	kHz
Minimum switching frequence in low-power mode (LPM)	–	LPM, I_{LOAD} = 0A	–	$f_{SW}/4$	–	kHz
Peak efficiency	–	DIV2	–	98.2	–	%

Note: * The maximum output power depends on the system thermal solution and the ambient temperature.

Parallel Evaluation Kit Contents and Hardware Requirements

Kit Contents

Table 2 lists the PE25208 parallel EVK box contents, as shown in Figure 1. Due to the high power (240W) required for USB-PD EPR application, even a 1% loss in efficiency results in a power dissipation of 2.4W. This is a high-power dissipation for the two PE25208 devices to handle without thermal solutions; therefore, heatsinks are provided to draw out heat from the devices as practically as possible.

Table 2. EVK Box Contents

Quantity	Description
1	Parallel PE25208 DC-DC converter evaluation board assembly
1	Thermal pads, to connect the devices to the heatsinks
1	Heatsinks, which require thermal glue to attach the thermal pads
1	P-channel MOSFET, for a PGATE input disconnect switch

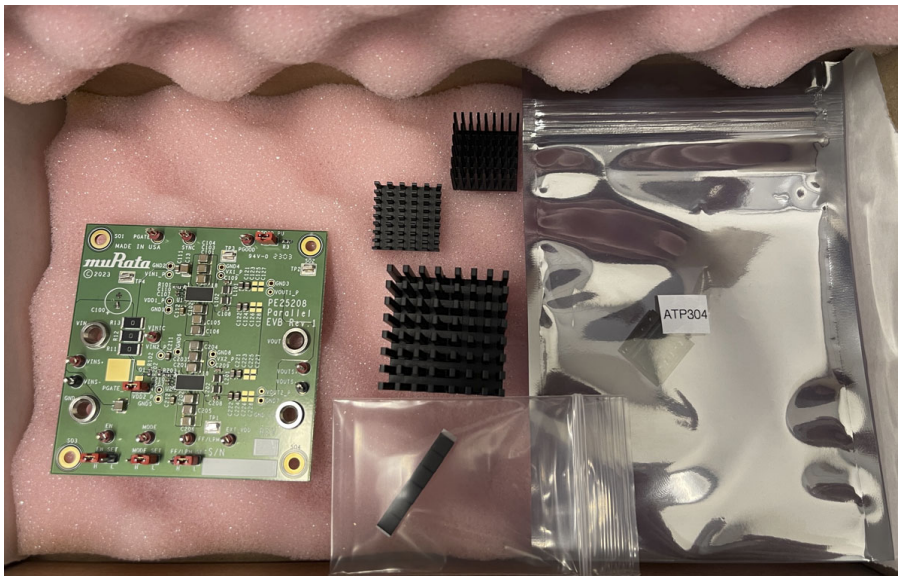

Figure 1. EVK Box Contents

Hardware Requirements

To evaluate the performance of the EVK board, the following equipment is required:

- Bench DC power supply capable of providing up to 60V at up to 5.5A
- DC load (power resistors or electric load)
- Four high-accuracy digital multimeters
- DC power and sense leads
- Optional: Bench DC power supply capable of supplying 5V for EXT_VDD to provide power to the PE25208 internal circuit while bypassing the PE25208 internal VDD LDO. This helps to reduce the VDD LDO loss, which further reduces the PE25208 power consumption, especially in low-power conditions.
- Optional: Four-channel oscilloscope with probes to view waveforms

Warning: The PE25208 parallel EVK contains components that could be damaged by exposure to voltages higher than the maximum specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals, or to signal inputs and outputs.

Before you connect the parallel EVK to the source power supply, verify that the power supply is off. Connecting the parallel EVK to a live power supply could induce failures.

Quick Start Guide

Quick Start Overview

The evaluation board is designed to ease your evaluation of the two PE25208 DC-DC converters operating in parallel. This section guides you through the hardware interfaces, various hardware configurations, EVK connections, and the startup procedure to operate the PE25208 parallel EVK.

Evaluation Board Overview

The parallel EVK is designed with accessible components for easy customer evaluation and contains the following:

- Power input and output terminals
- PCB headers
- Test and sense points

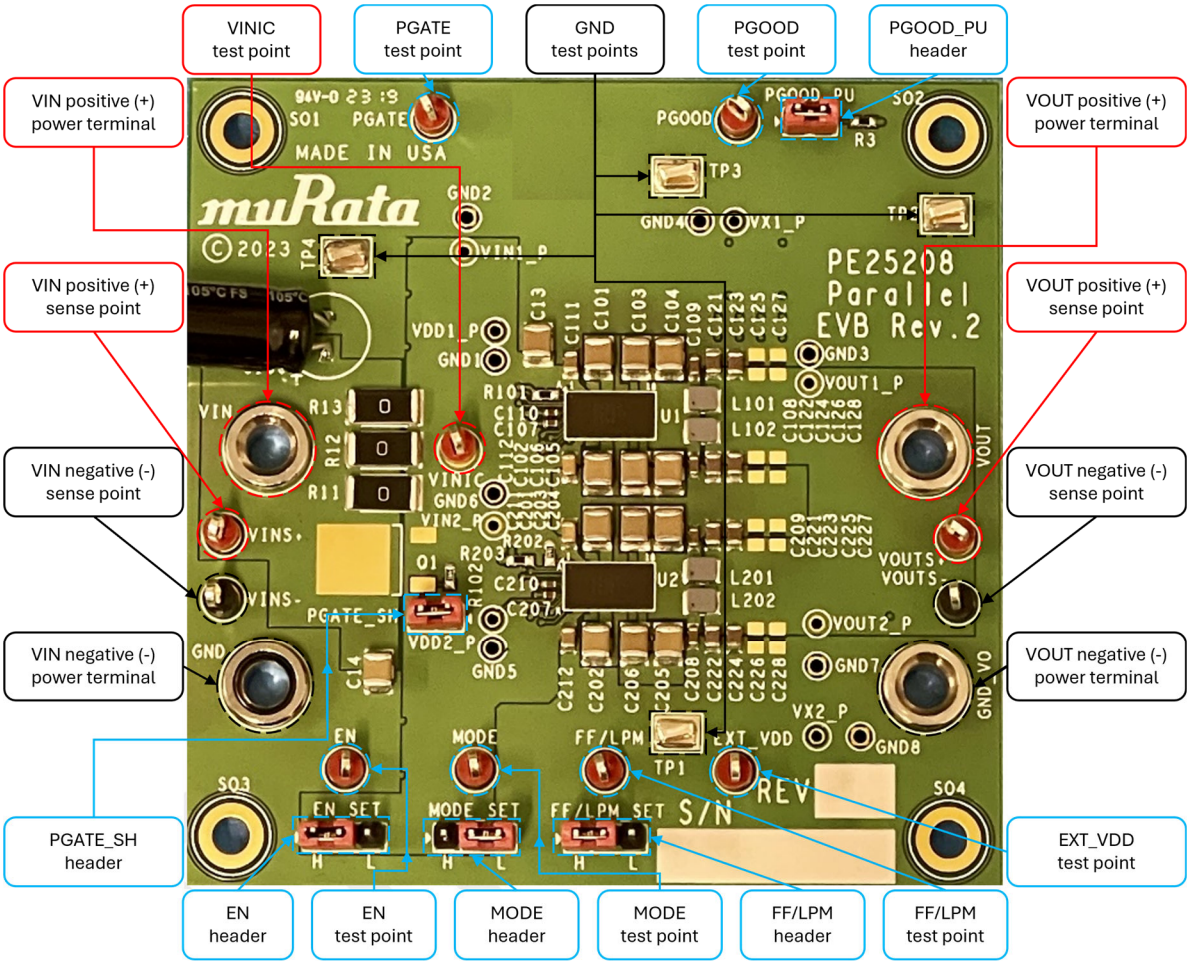

Figure 2. PE25208 Parallel EVK Hardware Interfaces

Power Input and Output Terminals

The PE25208 parallel EVK has four power terminals, as shown in Figure 2:

- The two VIN positive (+) and VIN negative (-) power input terminals, which receive input power from a connected bench DC power supply.
- The two VOUT positive (+) and VOUT negative (-) power output terminals, which deliver the output power to a connected DC load.

PCB Headers

The PE25208 parallel EVK includes two types of PCB headers:

- Configuration headers: These 3-pin headers configure the parallel PE25208 system.
- Connection headers: These 2-pin headers connect the PGATE pin of the primary PE25208 and the PGOOD pins of the two PE25208 devices to their respective auxiliary EVK connections.

Configuration Headers

The three configuration headers on the PE25208 parallel EVK include the following, as shown in Figure 2:

- EN header (EN_SET)
- MODE header (MODE_SET)
- FF/LPM header (FF/LPM_SET)

Before you apply power to the parallel EVK, verify that the three configuration headers are fitted with jumpers for your preferred configuration, because the set configurations only load at startup. To change the MODE header (MODE_SET) or the FF/LPM header (FF/LPM_SET) configuration during operation, you must first disable and then re-enable the PE25208 parallel system. If needed, you can change the EN header (EN_SET) configuration at any time during operation.

Table 3 lists the configuration header functions, the associated jumper configurations, and the recommended jumper configuration for a quick evaluation.

Table 3. Configuration Header Functions, Jumper Configurations, and Quick Evaluation Recommendations

Header	Function	Jumper		Quick Evaluation Recommendation
		High	Low	
EN_SET	Enables or disables the parallel PE25208 system through the EN input pin of both PE25208 devices: Logic high: Enabled Logic low: Disabled	Enabled: EN pins are tied to V_{IN}.	Disabled: EN pins are tied to GND.	HIGH
MODE_SET	Selects the output voltage division ratio of the parallel PE25208 system between DIV2 or DIV3 through the MODE pins of both PE25208 devices: Logic high: DIV2 Logic low: DIV3	DIV2 mode: MODE pins are tied to VDD.	DIV3 mode: MODE pins are tied to GND.	HIGH or LOW
FF/LPM_SET	Selects the clock mode of the parallel PE25208 system between fixed-frequency (FF) and low power mode (LPM) through the FF/LPM pins of both PE25208 devices: Logic high: FF Logic low: LPM	Fixed frequency (FF): FF/LPM pins are tied to VDD.	Low power mode (LPM): FF\LPM pins are tied to GND.	HIGH

Figure 3 shows the two valid jumper configurations of the configuration (3-pin) headers for operation.

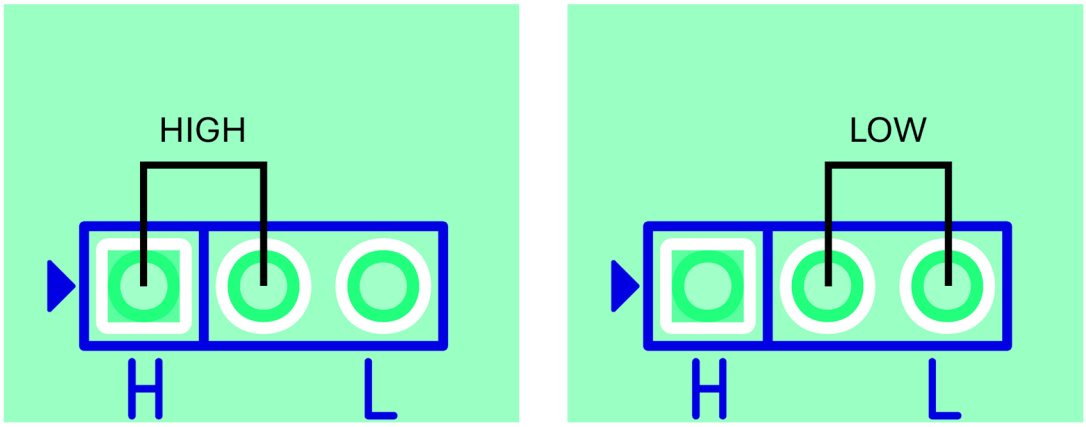

Figure 3. Valid Jumper Configurations for Operation

Connection Headers

The PE25208 parallel EVK has two connection headers, as shown in Figure 2:

- PGATE_SH header (PGATE_SH)
- PGOOD_PU header (PGOOD_PU)

Table 4 lists the connection header functions.

Table 4. Connection Header Functions

Header	Function
PGATE_SH	Connects the PGATE pin of the primary PE25208 device (U1) to the gate terminal of the external P-channel disconnect FET switch (Q1) and the anode terminal of the Zener diode (D1).
PGOOD_PU	Connects the PGOOD pin of both PE25208 devices to the 10 kΩ VDD pull-up resistor (R3).

To maintain the typical connections of the parallel EVK associated with the PGATE pin of the primary PE25208 (U1) and the PGOOD pins of both PE25208 devices, always fit the connection headers with jumpers as shown in the (✓) image in Figure 4, whether in operation or not. Do not use the (✗) image configuration in Figure 4.

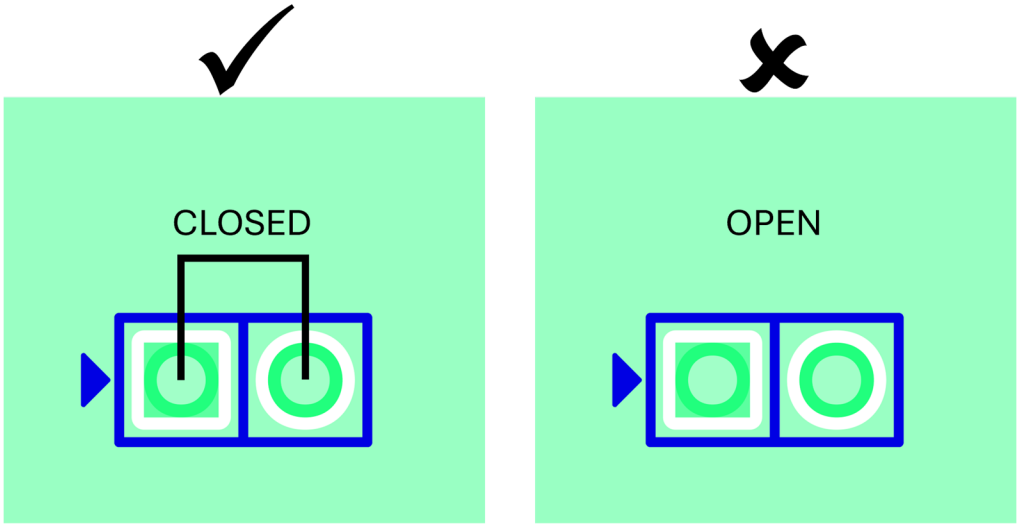

Figure 4. Mandatory (✓) and Invalid (✗) Jumper Configuration of Connection (2-pin) Headers

Test and Sense Points

The PE25208 parallel EVK includes various test points to measure the voltage values of critical signals, probe critical signals to observe their waveforms, and monitor supply external voltages to the parallel PE25208 system.

- To take accurate input voltage measurements, use the VIN positive (+) sense point (VINS+) and VIN negative (-) sense point (VINS-), as shown in Figure 2.
- To take accurate output voltage measurements, use the VOUT positive (+) sense point (VOUTS+) and VOUT negative (-) sense point (VOUTS-), as shown in Figure 2.

Table 5 lists all test points on the PE25208 parallel EVK, as shown in Figure 2.

Table 5. Test Point Descriptions

Test Point (TP)	Description
VINS+	Positive TP to measure the input voltage of the PE25208 parallel EVK.
VINS-	Negative TP to measure the input voltage of the PE25208 parallel EVK.
VOUTS+	Positive TP to measure the output voltage of the PE25208 parallel EVK.
VOUTS-	Negative TP to measure the output voltage of the PE25208 parallel EVK.
VINIC	Positive TP to measure the input voltage of the two parallel PE25208 devices.
EN	Status of the enable signal (EN) from the EN pins of the two parallel PE25208 devices.
MODE	Status of the output voltage division ratio's mode signal (MODE) from the MODE pins of the two parallel PE25208 devices.
FF/LPM	Status of the FF/LPM signal from the FF/LPM pins of the two parallel PE25208 devices.
PGOOD	Status of the power good (PGOOD) signal from the PGOOD pins of the two parallel PE25208 devices.
PGATE	Positive TP to measure the gate drive voltage of the external P-channel input disconnect FET switch from the PGATE pin of the primary PE25208 device.
EXT_VDD	Positive TP to apply and measure an external VDD supply voltage between 4.75V and 5.5V to the two parallel PE25208 devices through their EXT VDD pins.
TP1, TP2, TP3, TP4 (GND)	0V ground reference TPs.

Parallel EVK Connection

Connect the DC and power sense leads to the PE25208 parallel EVK as shown in Figure 5.

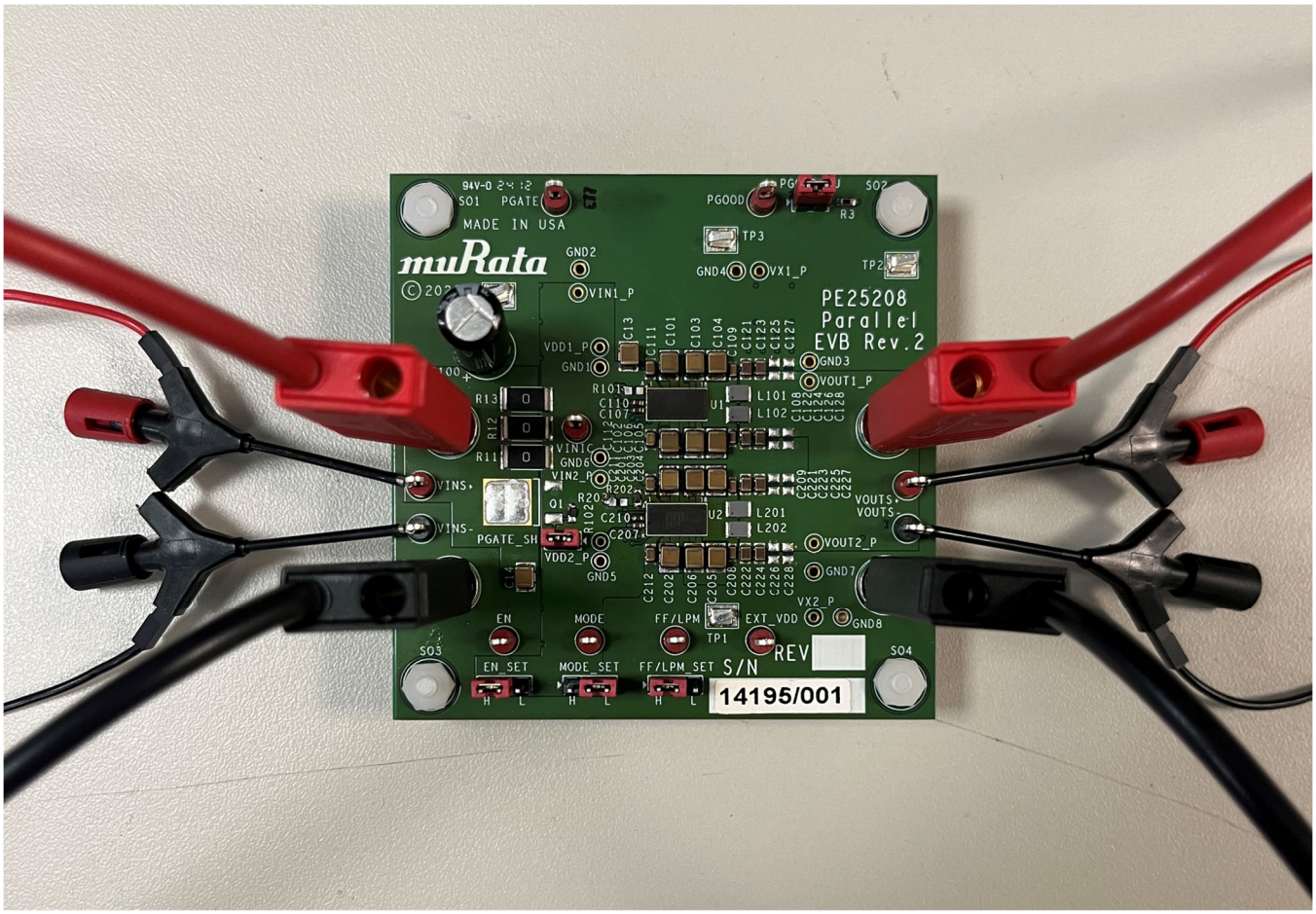

Figure 5. PE25208 Parallel EVK Connection to the Power and Sense Leads

Voltage-only Measurement Connections

To take only voltage measurements, connect the parallel EVK to the equipment as shown in Figure 6.

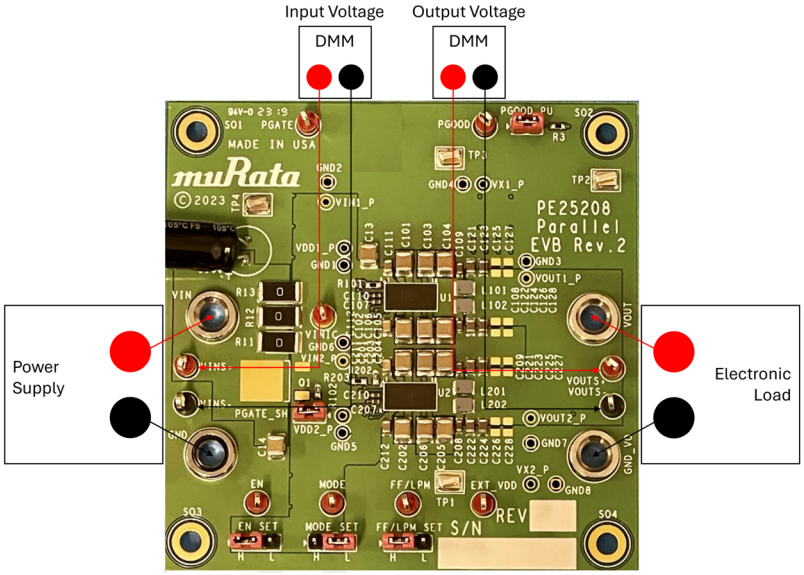

Figure 6. PE25208 Parallel EVK Connections to Equipment for Voltage-only Measurements

Voltage and Current Measurement Connections

To take both voltage and current measurements, connect the parallel EVK to the equipment as shown in Figure 7.

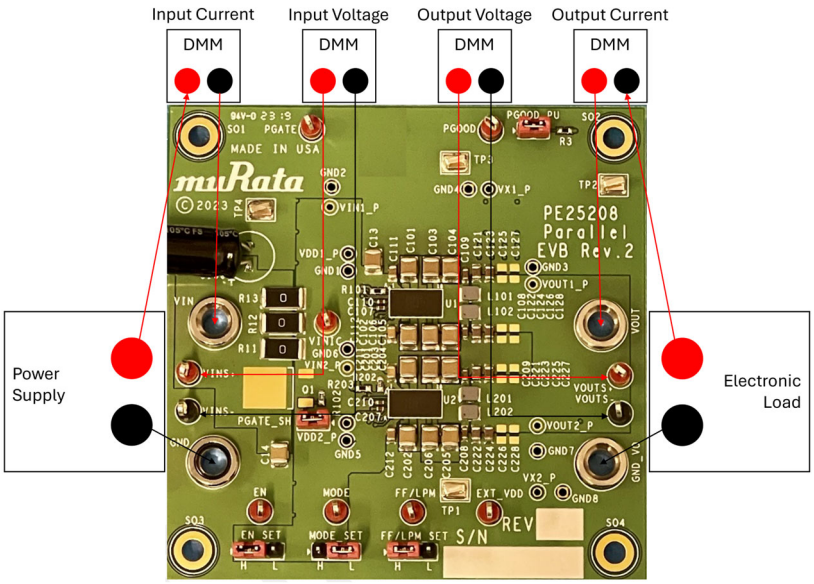

Figure 7. PE25208 Parallel EVK Connections to Equipment for Voltage and Current Measurements

Start-Up Procedure (Hardware Operating Guidelines)

This section provides the general guidelines and procedures to start up and operate the PE25208 parallel EVK. To achieve optimal performance, follow these steps to configure and operate the parallel EVK.

1. Before powering up the parallel EVK, install the jumpers on the PGATE_SH and PGOOD_PU headers as shown in Figure 8, then configure the EN_SET, MODE_SET, and FF/LPM_SET headers by fitting jumpers in the recommended positions for quick evaluation as listed in Table 3. For example, Figure 8 shows the EN_SET, MODE_SET, and FF/LPM headers set in the enable, divide-by-3 (DIV3) mode and fixed-frequency (FF) mode configuration, respectively.
2. Optional: If you prefer to use the PGATE input disconnect switch, fit the given external P-channel FET as Q1 and remove the three 0Ω jumper resistors, R11, R12, and R13.
3. Optional: If you prefer, supply an external VDD supply voltage between 4.75V and 5.5V to the EXT_VDD test point for light-load efficiency improvement and power consumption reduction on both parallel PE25208 devices instead of using their internally generated VDD voltage.
4. Connect the DC power and sense leads to the parallel EVK as shown in Figure 5, and with the power equipment turned off, connect the parallel EVK to the power and measuring equipment as shown in Figure 7. Minimize the length of the connections.
5. Apply an input voltage to the parallel EVK by setting the connected DC bench power supply to an 18V–60V voltage output and 5.5A current limit for DIV3 mode or a 18V–45V voltage output at 5.5A current limit for DIV2 mode.
6. Apply a load current to the parallel EVK by setting the connected electronic load to a 0A–15A current input for DIV3 mode or a 0A–10A current input for DIV2 mode.

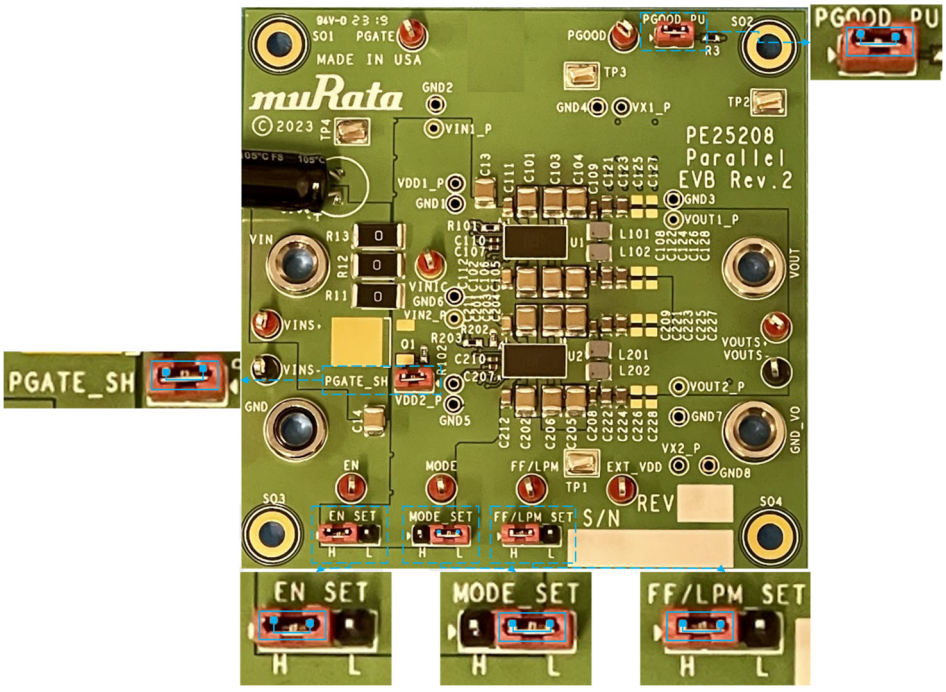

Figure 8. Jumper Installation of the PE25208 Parallel EVK PCB Headers

Performance Data

Figure 9 and Figure 10 show the typical performance of the PE25208 parallel EVK.

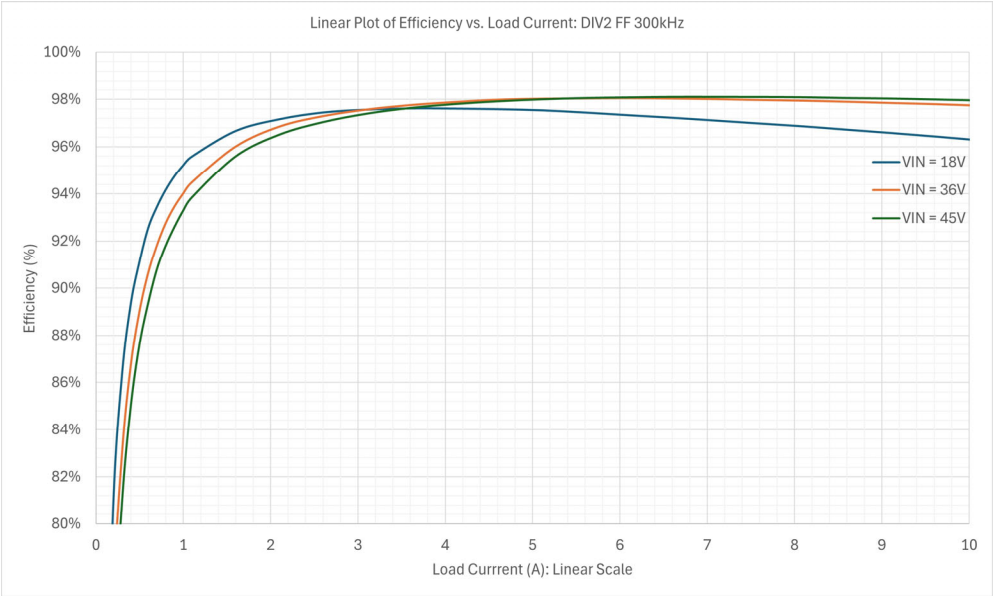

Figure 9. Linear Efficiency (%) vs. Load Current (A) Plot: VIN = (18V, 36V, 45V), DIV2, FF, 300 kHz

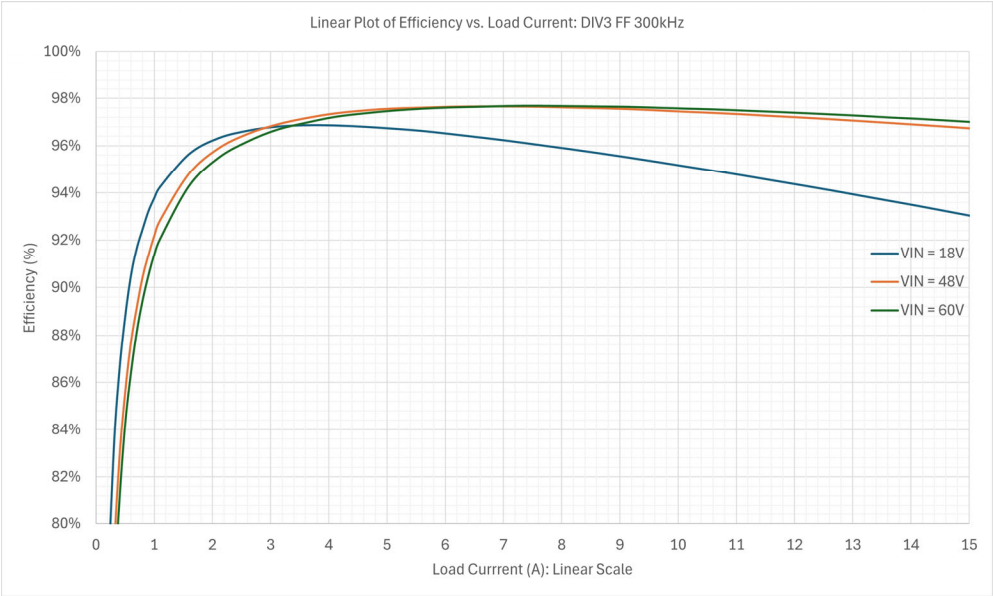

Figure 10. Linear Efficiency (%) vs. Load Current (A) Plot: VIN = (18V, 48V, 60V), DIV3, FF, 300 kHz

PE25208 Parallel EVK Schematic

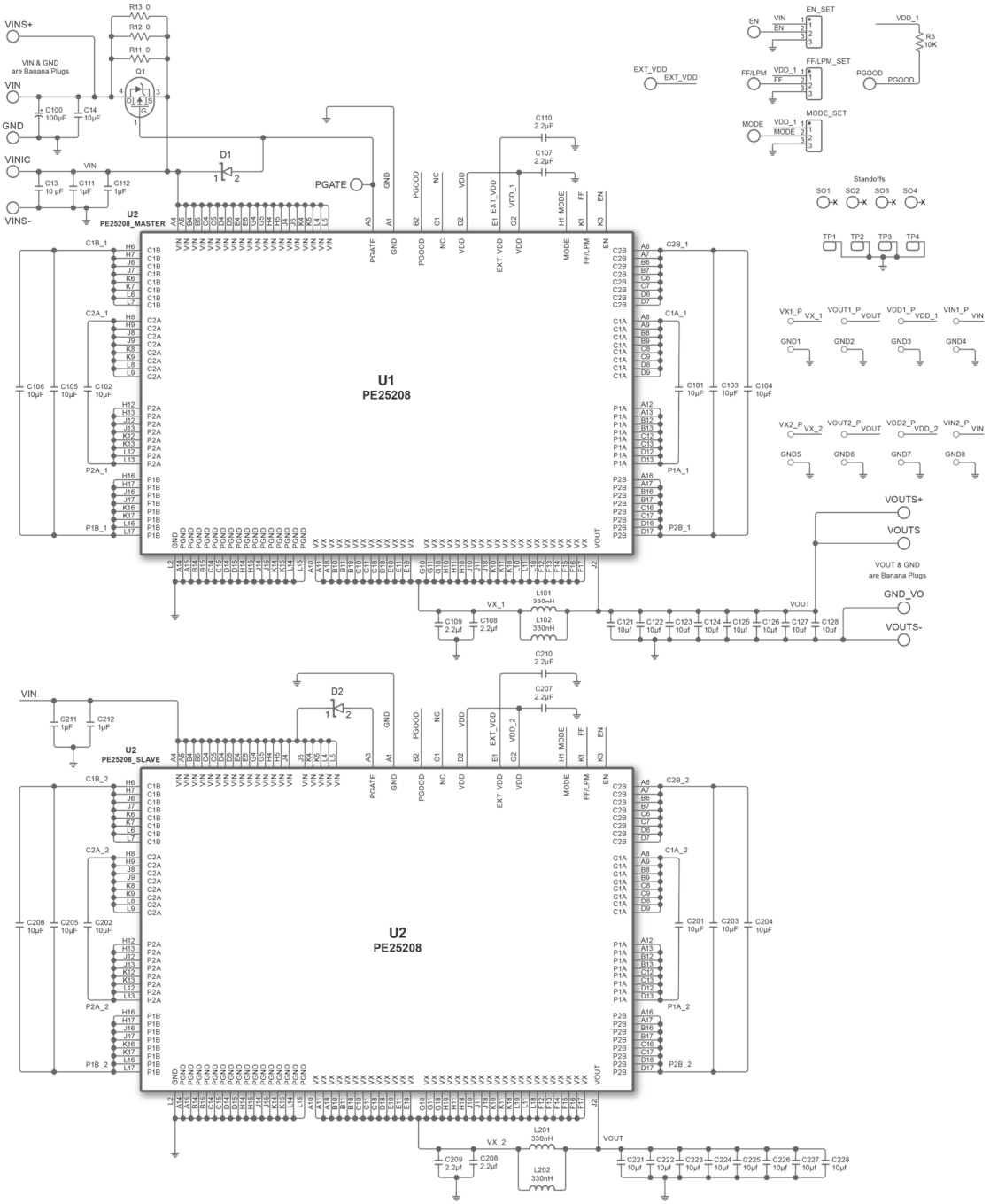

Figure 11. PE25208 Parallel EVK Schematic

PE25208 Parallel EVK Parts List

Table 6. PE25208 Parallel EVK Parts List

Reference	Qty	Value	Description	Part Number
Components required for parallel operation				
C13, C14, C101, C102, C103, C104, C105, C106, C201, C202, C203, C204, C205, C206	14	10 µF	CAP CER 10µF 100V X7S 1210	GRM32EC72A106KE05
C107, C110, C207, C210	4	2.2 µF	CAP CER 2.2µF 25V X5R 0402	GRM155R61E225ME15D
C108, C109, C208, C209	4	2.2 µF	CAP CER 2.2µF 50V X5R 0603	GRM188R61H225ME11D
C111, C112, C211, C212	4	1 µF	CAP CER 1µF 100V X7S 0805	GRM21BC72A105KE01L
C121, C122, C123, C124, C221, C222, C223, C224 [2]	8	10 µF	CAP CER 10µF 50V X5R 0805	GRM21BR61H106KE43
L101, L102, L201, L202	4	330 nH	FIXED IND 330nH 7.8A 8mΩ SMD	HTEL25201B-R33MXR-01
D1, D2	2	DIODE	DIODE ZENER 5.6V 500MW SOD523	MM5Z5V6T1G
R3	1	10 kΩ	RES SMD 10kΩ 1% 1/10W 0603	ERJ-3EKF1002V
U1, U2	2	PE25208	48 V_{IN} Divide-by-2 and -3, 15A Charge Pump, Capacitor Divider	PE25208
Additional components for evaluation purposes				
C100	1	100 µF	CAP ALUM 100µF 20% 80V RADIAL	EEU-FS1K101LB
R11, R12, R13	3	0 Ω	RES SMD 0Ω JUMPER 3W 2512	3522ZR
Q1 [1]	1	MOSFET	MOSFET P-CH 100V 37.1A TO252	SUD50P10-43L-GE3
VOUT, VIN, GND_VO, GND	4	TERMINAL	CONN BANANA JACK SOLDER	575-4
VOUTS+, VINS+, VINIC, PGOOD, PGATE, MODE, FF/LPM, EXT_VDD, EN	9	TP	PC TEST POINT MULTIPURPOSE RED	5010
VOUTS-, VINS-	2	TP	PC TEST POINT MULTIPURPOSE BLACK	5011
TP1, TP2, TP3, TP4	4	TP SMT	PC TEST POINT COMPACT SMT	5016
MODE_SET, FF/LPM_SET, EN_SET	3	HEADER	CONN HEADER VERT 3POS 2.54MM	PREC003SAAN-RC
PGOOD_PU, PGATE_SH	2	HEADER	CONN HEADER VERT 2POS 2.54MM	PREC002SAAN-RC
C125, C126, C127, C128, C225, C226, C227, C228, VX1_P, VOUT1_P, VIN1_P, VDD1_P, VX2_P, VOUT2_P, VIN2_P, VDD_2P, GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8	24	DNI	–	–
SO1, SO2, SO3, SO4	4	M3 HOLE	–	–

Notes:

1. External P-channel FET Q1 is optional, but when implemented remove R11, R12, and R13.
2. The minimum required VOUT capacitance is 47 µF. The maximum VOUT capacitance is up to 1 mF.

PE25208 Parallel EVK PCB Layout

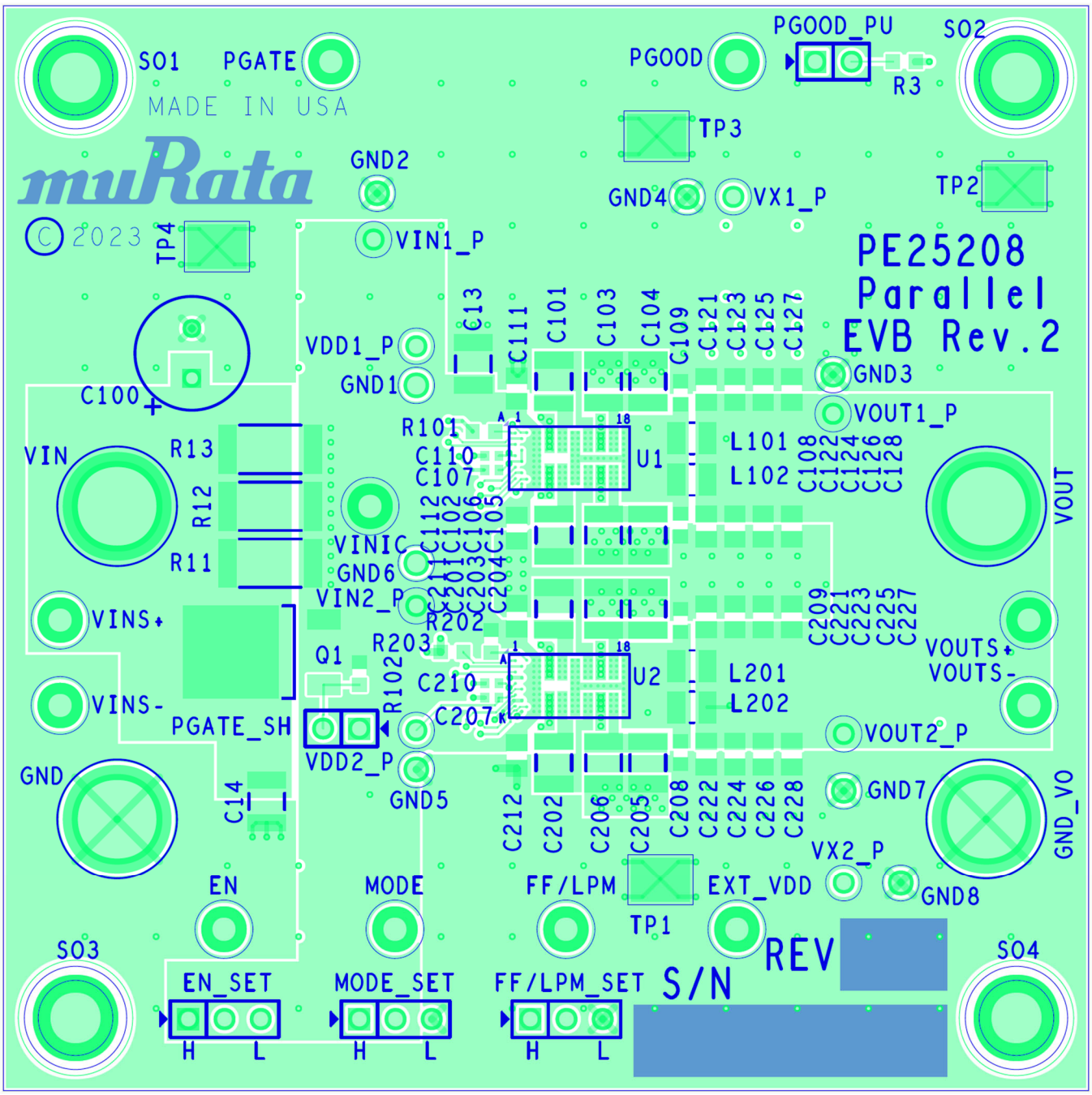

Figure 12. Top Layer (PWR and IC Signal Fanout) PCB Layout of the PE25208 Parallel EVK

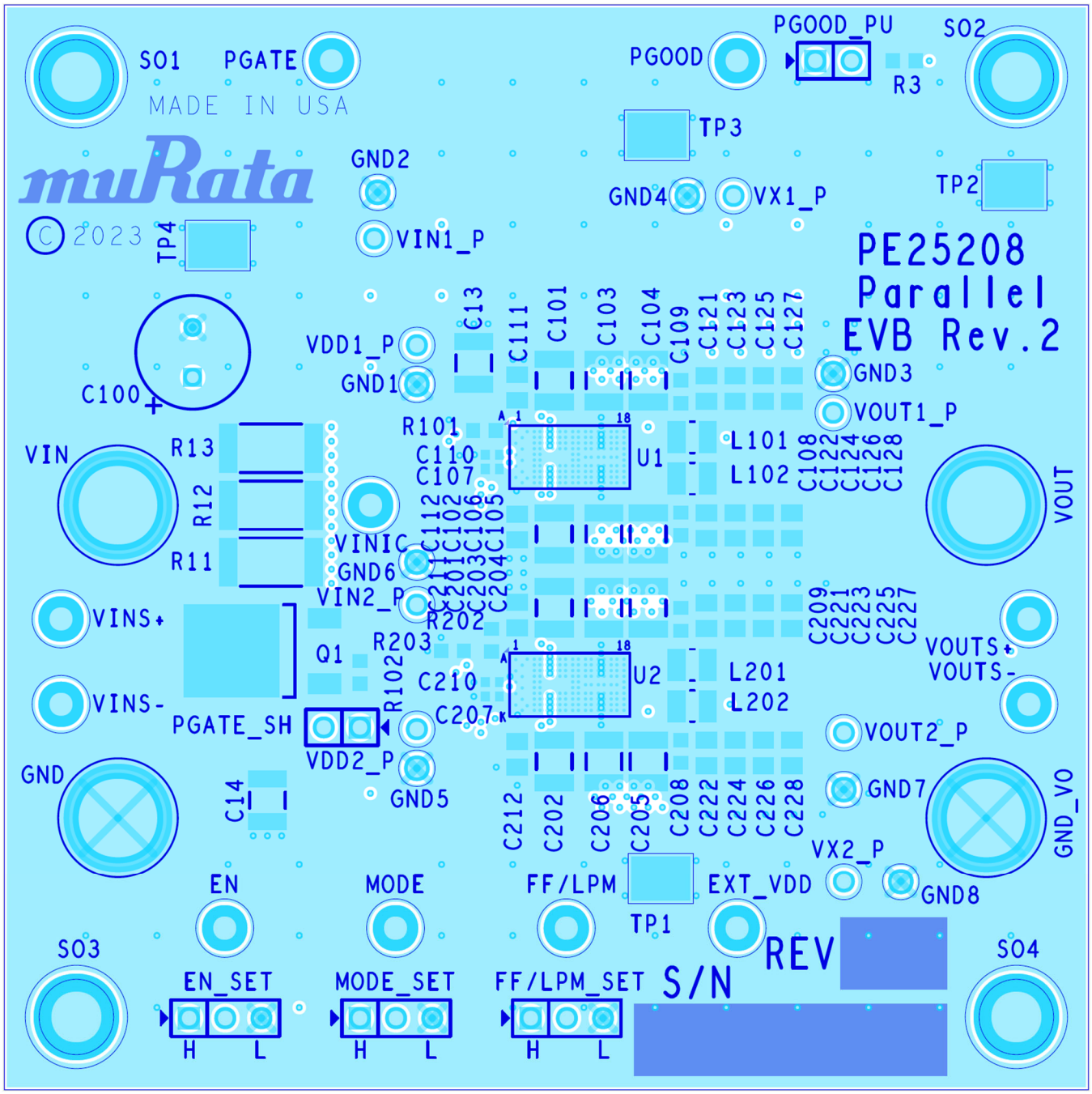

Figure 13. Inner Layer 1 (GND) PCB Layout of the PE25208 Parallel EVK

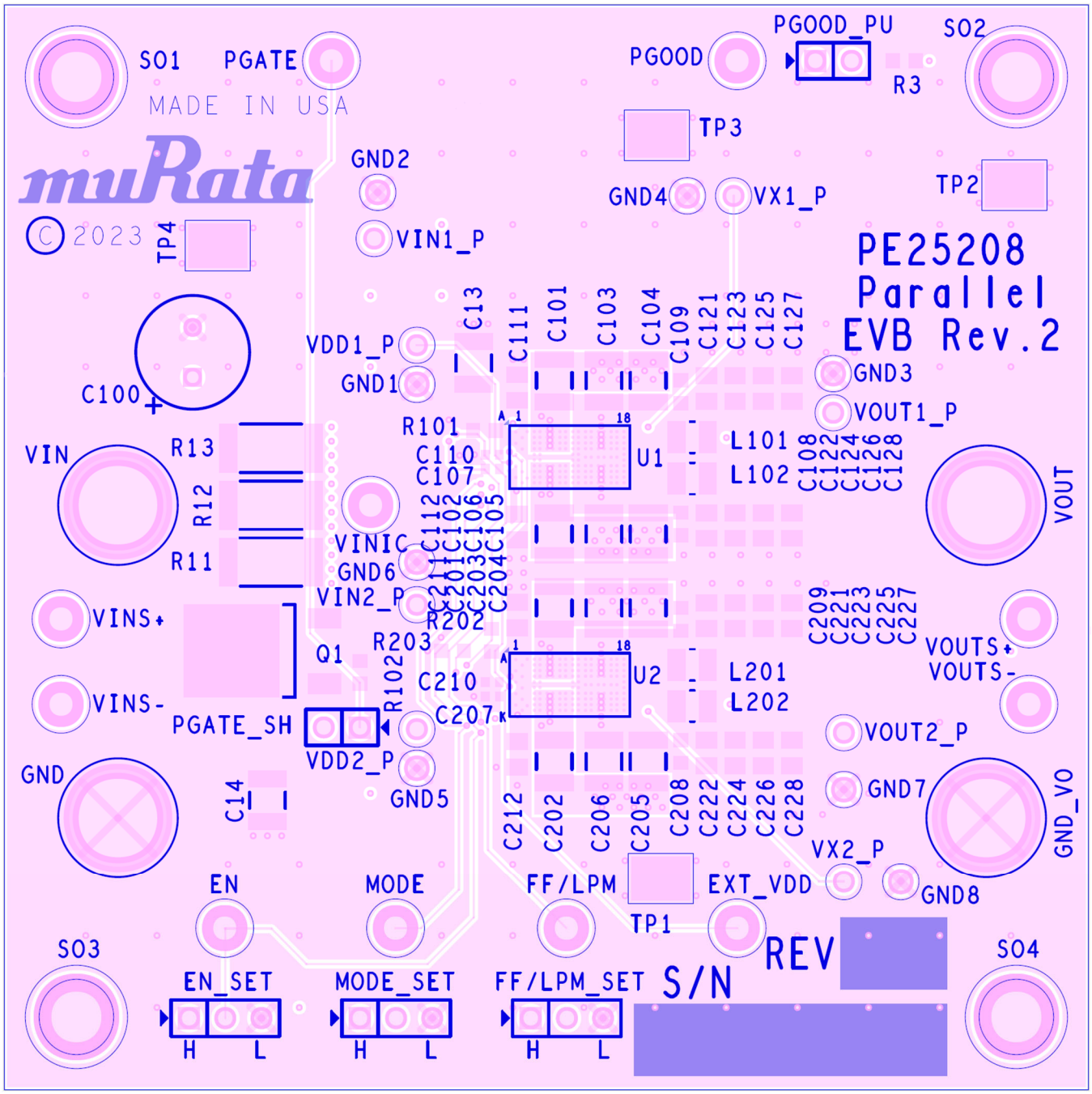

Figure 14. Inner Layer 2 (PWR and Signal) PCB Layout of the PE25208 Parallel EVK

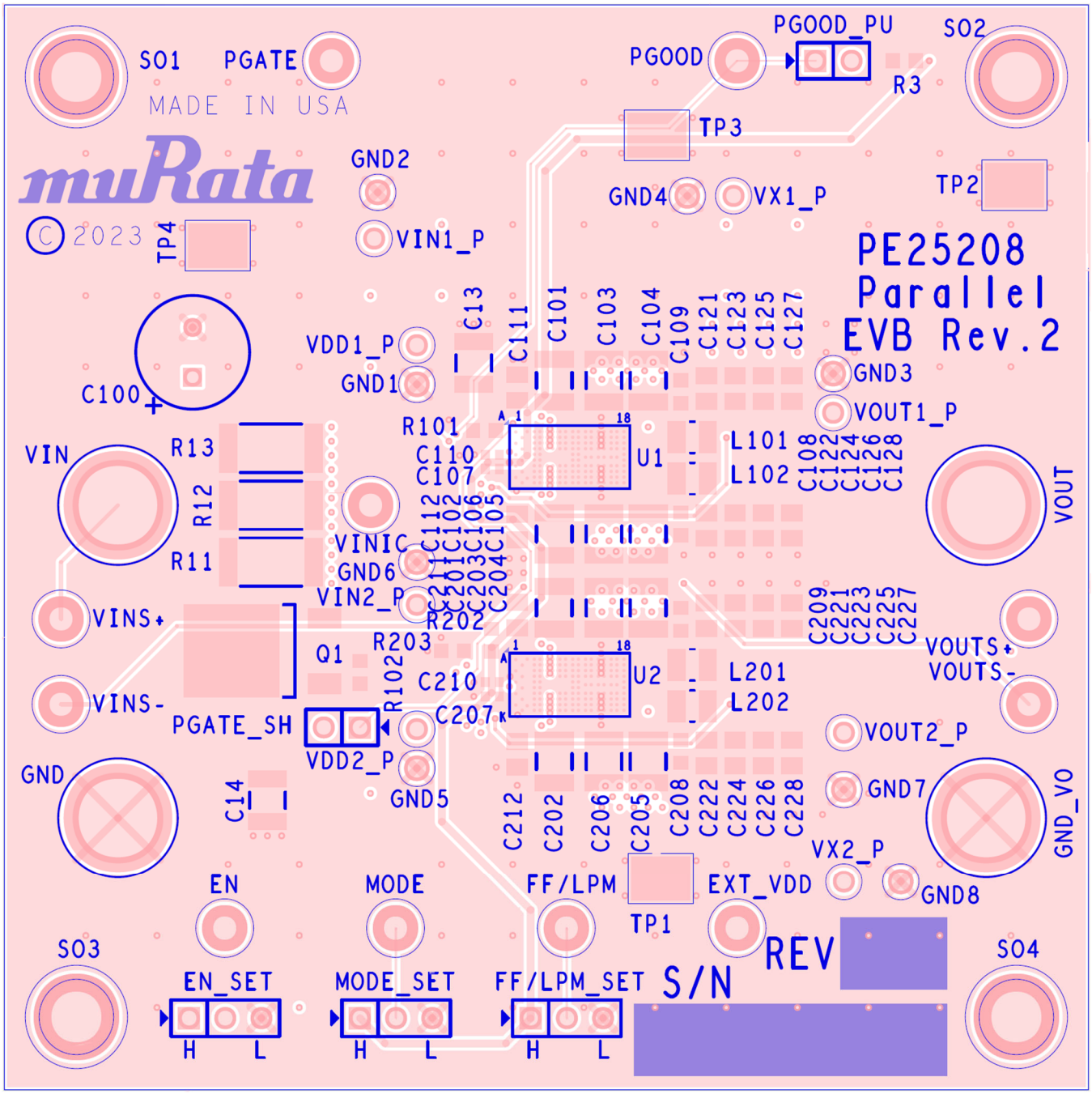

Figure 15. Bottom Layer (Signal) PCB Layout of the PE25208 Parallel EVK

Layout Considerations

Figure 16 shows the critical components required to implement the two parallel PE25208 devices. The red-highlighted connection lines are the high-power nodes in the design. Pay close attention to the parasitic resistances and parasitic inductances at these nodes. The area of these connections must be made sufficient.

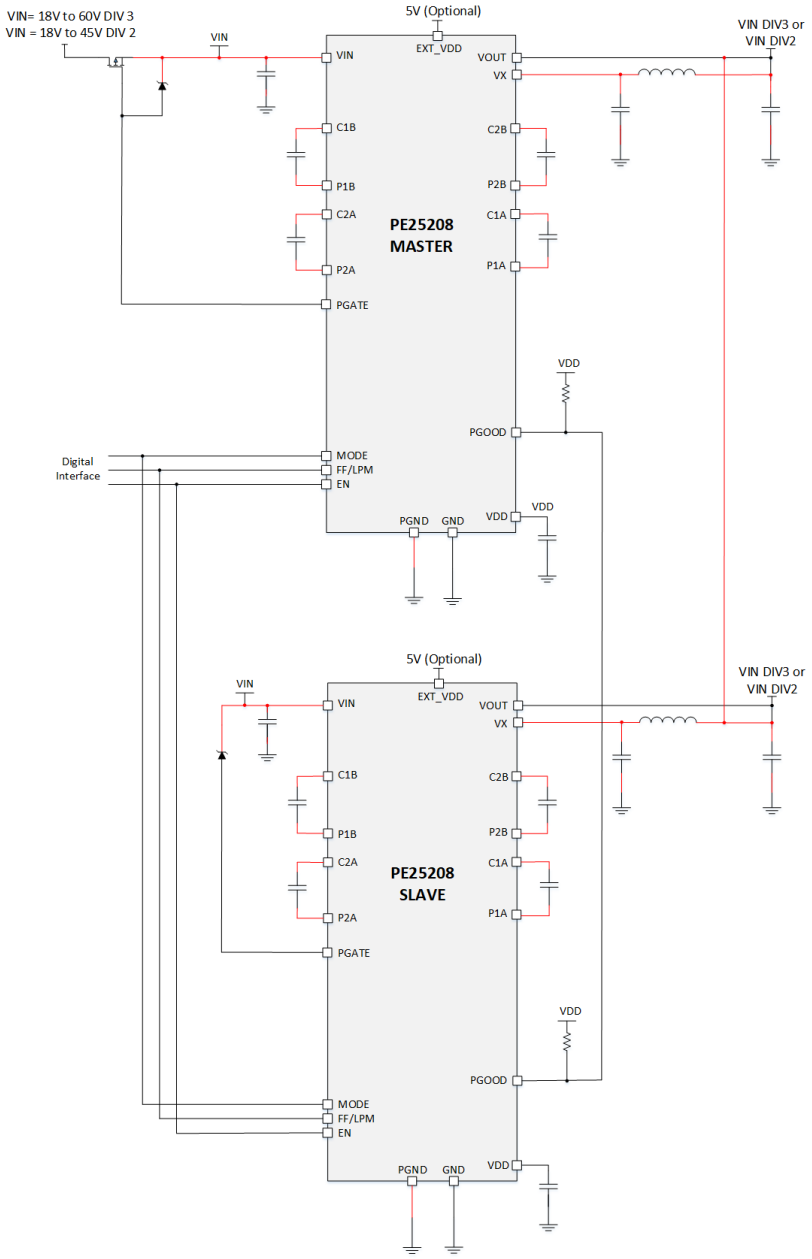

Figure 16. Application Circuit of Two PE25208 Devices in Parallel Operation

Pinout Information and Component Placement

In the PE25208 parallel EVK, both PE25208 devices are placed according to the Figure 17 pin map, where the input voltage (VIN) is at its left side and the output voltage that requires filtering (VX) is at the right side.

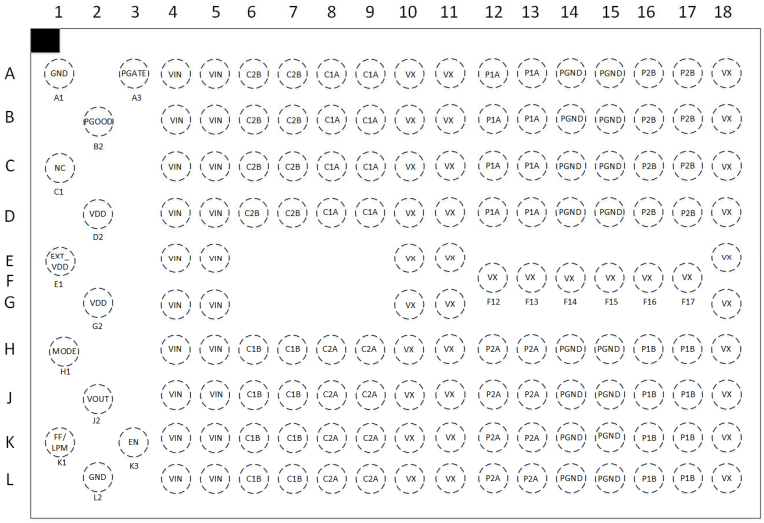

Figure 17. PE25208 Device Pinout (Top View: Bumps Down)

In design, place critical components required to implement the two parallel PE25208 devices as close as possible to both devices as shown in Figure 18.

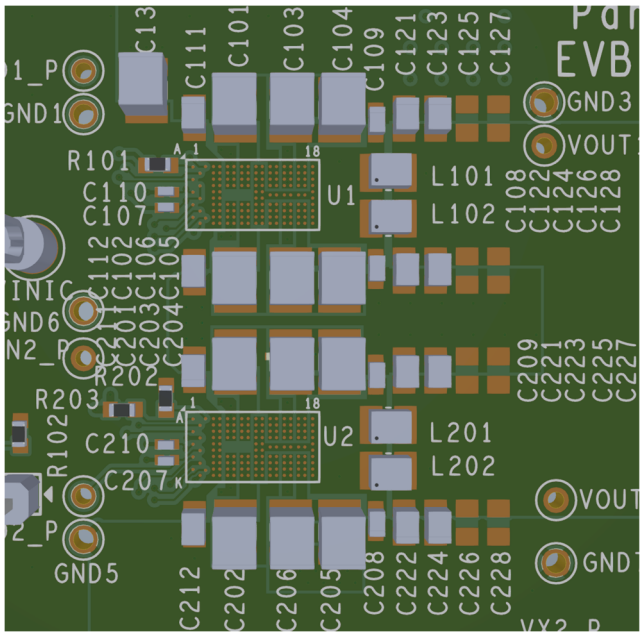

Figure 18. 3D PCB Layout and Critical Component Placement for the Two Parallel PE25208 Devices

Technical Resources

Additional technical resources are available for download in the Products section at www.psemi.com. These include the product specification datasheet, S-parameters, zip file, evaluation kit schematic, bill of materials, material declaration form, and PC-compatible software file.

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