ADVANCE INFORMATION

PE3337DIE

3.0 GHz Integer-N PLL

Features

- 3.0 GHz operation
- ÷10/11 dual modulus prescaler
- Phase detector output
- Serial interface or hardwired programmable
- Ultra-low phase noise
- Die Form

Product Description

Peregrine's PE3337 is a high-performance integer-N PLL capable of frequency synthesis up to 3.0 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLL's. The device is offered in electrically screened die form for MCM/Hybrid applications.

The PE3337 features a ÷10/11 dual modulus prescaler, counters, and a phase comparator as shown in Figure 1. Counter values are programmable through a serial interface, and can also be directly hard wired.

Fabricated in Peregrine's patented UTSi® (Ultra Thin Silicon) CMOS technology, the PE3337 offers excellent RF performance and intrinsic radiation tolerance.

Figure 1. Block Diagram

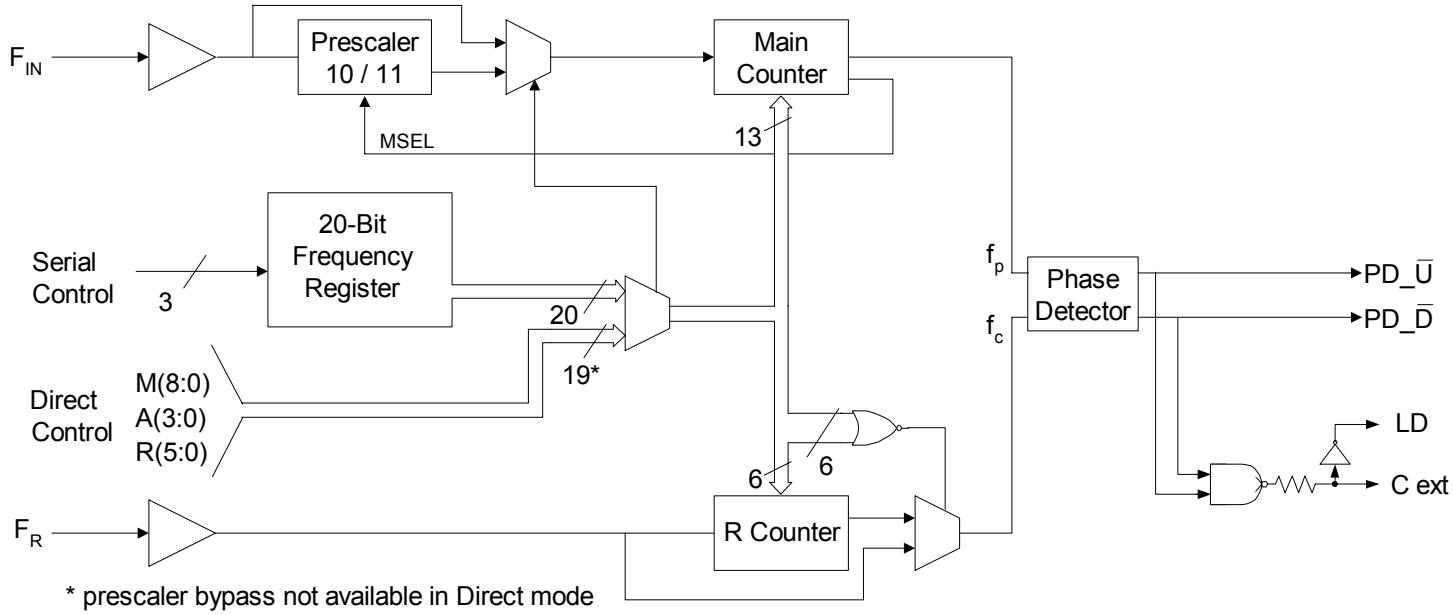


Figure 2. Pad Configuration

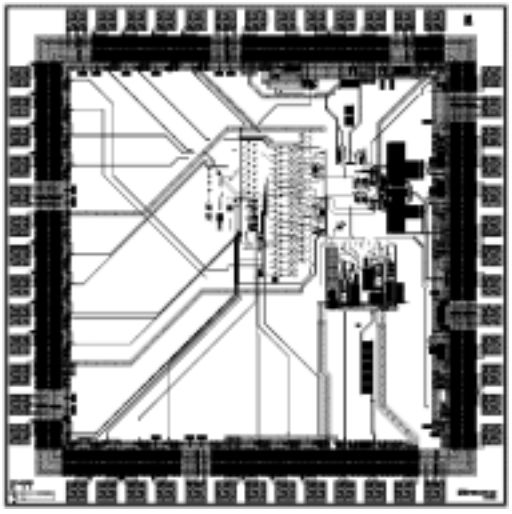


Table 1. Pad Descriptions

Pad #	X	Y	Name	Interface Mode	Type	Description
1	0	1188	VDD_R	Both	(Note 1)	Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended.
2	-150	1188	VDD_E	Both	(Note 1)	Same as Pad 1
3	-300	1188	R0	Direct	Input	R Counter bit0
4	-450	1188	R1	Direct	Input	R Counter bit1
5	-600	1188	R2	Direct	Input	R Counter bit2
6	-750	1188	R3	Direct	Input	R Counter bit3
7	-900	1188	GND_E	Both		GND
8	-1188	900	R4	Direct	Input	R Counter bit4
9	-1188	750	R5	Direct	Input	R Counter bit5 (MSB)
10	-1188	600	M0	Direct	Input	M Counter bit0
11	-1188	450	M1	Direct	Input	M Counter bit1
12	-1188	300	VDD_E	Both	(Note 1)	Same as Pad 1
13	-1188	150	VDD_C	Both	(Note 1)	Same as Pad 1
14	-1188	0	M_2	Direct	Input	M Counter bit2
15	-1188	-150	M_3	Direct	Input	M Counter bit3
16	-1188	-300	S_WR	Serial	Input	Frequency register load enable input. Buffered data is transferred to the frequency register on S_WR rising edge.
			M_4	Direct	Input	M Counter bit4
17	-1188	-450	DATA	Serial	Input	Binary serial data input. Data is entered LSB first, and is clocked serially into the 20-bit frequency control register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of CLOCK.

Pad #	X	Y	Name	Interface Mode	Type	Description
			M_5	Direct	Input	M Counter bit5
18	-1188	-600	GND_C	Both		GND
19	-1188	-750	GND_E	Both		GND
20	-1188	-900	CLOCK	Serial	Input	Clock input. Data is clocked serially into either the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of CLOCK.
			M6	Direct	Input	M Counter bit6
21	-900	-1188	M7	Direct	Input	M Counter bit7
22	-750	-1188	M8	Direct	Input	M Counter bit8 (MSB)
23	-600	-1188	A0	Direct	Input	A Counter bit0
24	-450	-1188	BMODEX	Both	Input	Selects direct interface mode (D_{MODE}=1) or serial interface mode (D_{MODE}=0)
25	-300	-1188	VDD_E	Both	(Note 1)	Same as Pad 1
26	-150	-1188	VDD_P	Both	(Note 1)	Same as Pad 1
27	0	-1188	E_WR	Serial	Input	Enhancement register write enable. While E_WR is "high", DATA can be serially clocked into the enhancement register on the rising edge of CLOCK.
			A1	Direct	Input	A Counter bit1.
28	150	-1188	A2	Direct	Input	A Counter bit2
29	300	-1188	A3	Direct	Input	A Counter bit3 (MSB)
30	450	-1188	FIN	Both	Input	RF prescaler input from the VCO. 3.0 GHz max frequency
31	600	-1188	FINX	Both	Input	Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor directly to the ground plane.
32	750	-1188	GND_P	Both		GND
33	900	-1188	GND_E	Both		GND
34	1188	-900	GND_0	Both		GND
35	1188	-750	CPSEL	Both	Input	Charge pump select. "High" enables the charge pump and disables pins PD_U and PD_D by forcing them "low". A "low" Tri-states the CP and enables PD_U and PD_D.
36	1188	-600	VDD_O	Both	(Note 1)	Same as Pad 1
37	1188	-450	DOUT	Serial	Output	Data Out. The Main Counter output, R Counter output, or dual modulus prescaler select (MSEL) can be routed to D_{OUT} through enhancement register programming.
38	1188	-300	VDD_E	Both	(Note 1)	Same as Pad 1
39	1188	-150	CP	Both	Output	Charge pump output. Selected when CPSEL = "1". Tristate when CPSEL = "Low".
40	1188	0	VDD_O	Both	(Note 1)	Same as Pad 1
41	1188	150	GND_O	Both		GND
42	1188	300	PD_DX	Both	Output	PD_D pulses down when f_p leads f_c.
43	1188	450	PD_UX	Both		PD_U pulses down when f_c leads f_p.

Pad #	X	Y	Name	Interface Mode	Type	Description
44	1188	600	VDD_O	Both	(Note 1)	Same as Pad 1
45	1188	750	VDD_E	Both	(Note 1)	Same as Pad 1
46	1188	900	CEXT	Both	Output	Logical "NAND" of PD_U and PD_D, passed through an on-chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
47	900	1188	GND_O	Both		GND
48	750	1188	GND_E	Both		GND
49	600	1188	GND_R	Both		GND
50	450	1188	FR	Both	Input	Reference frequency input
51	300	1188	ENHX	Both	Output, OD	Enhancement mode. When asserted low ("0"), enhancement register bits are functional.
52	150	1188	LD	Serial	Output	Lock detect output, the open-drain logical inversion of C_{EXT}. When the loop is locked, LD is high impedance; otherwise LD is a logic low ("0").

Note 1: V_{DD} pads 1, 11, 12, 23, 31, 33, 35, and 38 are connected by diodes and must be supplied with the same positive voltage level.

Note 2: All digital input pins have 70 kΩ pull-down resistors to ground.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD} + 0.3	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
T_{stg}	Storage temperature range	-65	150	°C

Table 3. Operating Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.15	V
T_A	Operating ambient temperature range	-40	85	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Level	Units
V_{ESD}	ESD voltage (Human Body Model) – Note 1	1000	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 5. DC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified. All parameters at T_A = 85° C guaranteed through wafer probe. Temperature performance verified on sample basis during lot evaluation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current; Prescaler disabled Prescaler enabled	V_{DD} = 2.85 to 3.15 V		 10 24	 31	 mA mA
Digital Inputs: All except F_R, F_{IN} (all digital inputs have 70k ohm pull-up resistors)						
V_{IH}	High level input voltage	V_{DD} = 2.85 to 3.15 V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85 to 3.15 V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.15 V			+70	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.15 V	-1			µA
Reference Divider input: F_R						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.15 V			+100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.15 V	-100			µA
Counter and phase detector outputs: f_c, f_p.						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = -3 mA	V_{DD} - 0.4			V
Lock detect outputs: C_{EXT}, LD						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{out} = 100 µ			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{out} = -100 µ	V_{DD} - 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 6 mA			0.4	V

Table 6. AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified. All parameters at T_A = 85° C guaranteed through wafer probe. Temperature performance verified on sample basis during lot evaluation.

Symbol	Parameter	Conditions	Min	Max	Units
Control Interface and Latches (see Figures 1and 3)					
f_{Clk}	CLOCK Serial data clock frequency	(Note 1)		10	MHz
t_{ClkH}	CLOCK Serial clock HIGH time		30		ns
t_{ClkL}	CLOCK Serial clock LOW time		30		ns
t_{DSU}	DATA set-up time after CLOCK rising edge		10		ns
t_{DHLD}	DATA hold time after CLOCK rising edge		10		ns
t_{PW}	S_WR pulse width		30		ns
t_{CWR}	CLOCK rising edge to S_WR rising edge.		30		ns
t_{CE}	CLOCK falling edge to E_WR transition		30		ns
t_{WRC}	S_WR falling edge to CLOCK rising edge.		30		ns
t_{EC}	E_WR transition to CLOCK rising edge		30		ns
t_{MDO}	MSEL data out delay after F_{IN} rising edge	C_L = 12 pf		8	ns

Note 1: Fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify Fclk specification.

Table 7. AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified. All parameters verified on sample basis during lot evaluation.

Symbol	Parameter	Conditions	Min	Max	Units
Main Divider (Including Prescaler)					
F_{IN}	Operating frequency		500	3000	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Main Divider (Prescaler Bypassed)					
F_{IN}	Operating frequency		50	300	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Reference Divider					
F_R	Operating frequency	(Note 3)		100	MHz
P_{Fr}	Reference input power	Single-ended input, (Note 1)	-2		dBm
Phase Detector					
f_c	Comparison frequency	(Note 3)		20	MHz

Note 1: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of $0.5V_{p-p}$.

Note 2: Parameter is guaranteed through characterization only and is not tested.

Functional Description

The PE3337 consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters "R" and "M" divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter ("A") is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via a serial bus or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

Main Counter Chain

Normal Operating Mode

Setting the PB control bit "low" enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (F_{IN}) by an integer derived from the values in the "M" and "A" counters.

In this mode, the output from the main counter chain (f_p) is related to the VCO frequency (F_{IN}) by the following equation:

$$f_p = F_{IN} / [10 \times (M + 1) + A] \quad (1)$$
where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{IN} = [10 \times (M + 1) + A] \times (F_R / (R+1)) \quad (2)$$
where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that F_{IN} must be greater than or equal to 90 x (F_R / (R+1)) to obtain contiguous channels. The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode

Setting the frequency control register bit PB "high" allows F_{IN} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. This mode is only available when using the serial port to set the frequency control bits. The following equation relates F_{IN} to the reference frequency F_R:

$$F_{IN} = (M + 1) \times (F_R / (R+1)) \quad (3)$$
where $1 \leq M \leq 511$

Reference Counter

The reference counter chain divides the reference frequency F_R down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \quad (4)$$
where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency (F_R) directly to the phase detector.

Register Programming

Serial Interface Mode

Serial Interface Mode is selected by setting the D_{MODE} input "low".

While the E_WR input is "low", serial data (DATA input), B_0 to B_{19}, is clocked into a buffer register on the rising edge of CLOCK, LSB (B_0) first. The contents from this buffer register are transferred into the frequency control register on the rising edge of S_WR according to the timing diagram shown in Figure 3. This data controls the counters as shown in Table 7.

While the E_WR input is "high", serial data (DATA input), B_0 to B_7, is clocked into a buffer register on the rising edge of CLOCK, LSB (B_0) first. The contents from this buffer register are transferred into the enhancement register on the falling edge of E_WR according to the timing diagram shown in Figure 3. After the falling edge of E_WR, the data provides control bits as shown in Table 8. These bits are active when the $\overline{Enh}$ input is "low".

Direct Interface Mode

Direct Interface Mode is selected by setting the D_{MODE} input "high". In this mode, the counter values are set directly at external pins as shown in Table 7 and Figure 2. All frequency control register bits are addressable except PB (it is not possible to bypass the ÷10/11 dual modulus prescaler in Direct Mode).

Table 7. Frequency Register Programming

Interface Mode	$\overline{Enh}$	D_{MODE}	R_5	R_4	M_8	M_7	PB	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Serial*	1	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}
Direct	1	1	R_5	R_4	M_8	M_7	0	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0

* Data is clocked serially on CLOCK rising edge while E_WR is "low" and transferred to frequency register on S_WR rising edge.

LSB (first in) — MSB (last in)

Table 8. Enhancement Register Programming

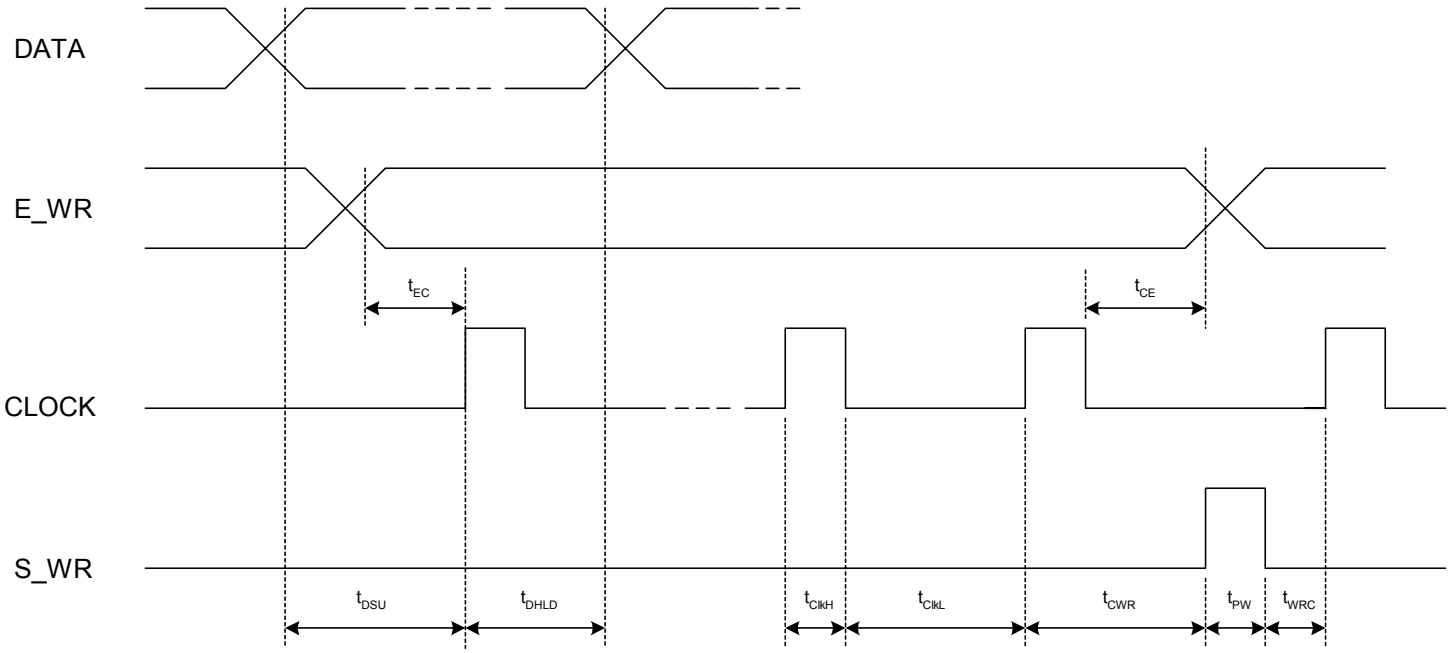
Interface Mode	$\overline{Enh}$	D_{MODE}	Reserved*	Reserved*	fp output	Power down	Counter load	MSEL output	fc output	Reserved*
Serial**	0	X	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

* Program to 0

* Data is clocked serially on CLOCK rising edge while E_WR is "low" and transferred to frequency register on S_WR rising edge.

LSB (first in) — MSB (last in)

Figure 3. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below. All bits are active high. Operation is undefined if more than one output is sent to D_{OUT}.

Table 9. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved**	
Bit 1	Reserved**	
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the R counter output onto the D_{OUT} output
Bit 7	Reserved**	

** Program to 0

Phase Detector Outputs

The phase detector is triggered by rising edges from the main counter (f_p) and the reference counter (f_c). It has two outputs, PD_$\overline{U}$, and PD_$\overline{D}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_$\overline{D}$ pulses "low". If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_$\overline{U}$ pulses "low". The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c. The phase detector gain is 430 mV / radian.

PD_$\overline{U}$ and PD_$\overline{D}$ are designed to drive an active loop filter which controls the VCO tune voltage. PD_$\overline{U}$ pulses result in an increase in VCO frequency and PD_$\overline{D}$ results in a decrease in VCO frequency.

Software tools for designing the active loop filter can be found at Peregrine's web site (www.peregrine-semi.com).

Lock Detect Output

A lock detect signal is provided at pin LD, via the pin C_{EXT} (see Figure 1). C_{EXT} is the logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$ waveforms, driven through a series 2k ohm resistor. Connecting C_{EXT} to an external shunt capacitor provides integration of this signal.

The C_{EXT} signal is then sent to the LD pin through an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_$\overline{U}$ and PD_$\overline{D}$.

Wafer and Die Packaging Options

Peregrine Semiconductor has two methods for shipment of die to our customers. The shipping option used is based on the customer's requirements and the number of die being shipped.

Peregrine offers product dice in two packaging options: Standard Die Carrier Packages and Wafer Packages. Where no shipping method is specified, Peregrine will sip in Standard Die Carrier Package (waffle pack).

Standard Die Carrier Package

- Chips which have been electrically probed, inked, visually inspected, diced, may be packaged in 4"x4" Waffle Packs.
- Standard die carrier packages protect the product from mechanical damage during shipment and prevent individual die from contacting one another
- The containers also provide protection from static discharge, moisture and other contamination by sealing in the proper static and moisture protective bags.
- Die are held in cavities with defined matrix. Ideal for small volumes.
- Die orientation is indicated on label.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection – dice in carriers, geometry side up.
- Carrier holds 100 dice.

Figure 12. Waffle Pack

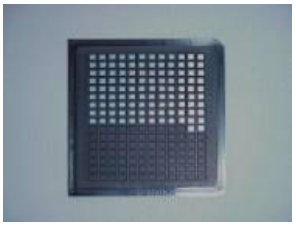
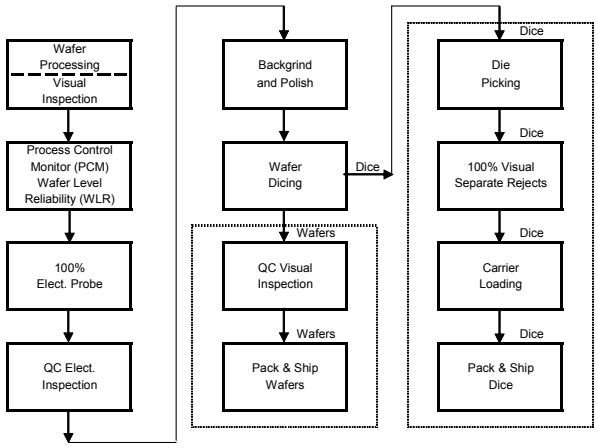


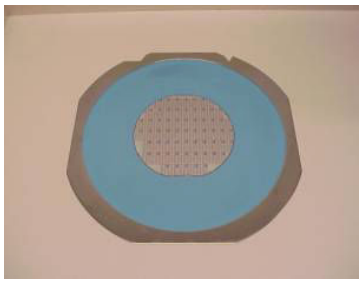
Figure 13. Dice and Wafer Processing Flow



Wafer Package

Wafers which have been electrically probed, inked, visually inspected and diced.

Figure 14. Wafer Mount



Wafer Mount/Dicing

In preparation for dicing, wafers are mounted to film frames or rings with mounting tape. There are two types of tape that can be utilized: PVC backed or U.V. release tape. Figure 14 shows a wafer mounted on film frame using PVC backed mounting tape.

- 100% electrically probed – rejects inked.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied, thinned and diced.

Wafer and Die Package, Storage and Preservation

Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.

- Product should be stored in original unopened packaging or, once opened, in a Nitrogen purged cabinet at room temperature (45% +/- 15% RH controlled environment).

- Sawn wafers mounted on dicing tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used for mounting the product. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container. To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.

- In all cases, the customer must determine the applicability of extended storage durations and conditions with respect to their assembly process and end product criteria.

Die Handling

All die products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263. ESD wrist strap and cord must be worn at a static safe workstation to eliminate failures due to ESD. Product must be handled only in a class 10,000 or better designated clean room environment.

Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used. Automated Wafer and Die Handling systems are readily available and provide the highest degree of protection and consistency to the handling operation.

Recommended Dice Assembly Procedure

Cleaning

Dice supplied in die or wafer form do not require cleaning prior to assembly.

Die Attach

The Peregrine Semiconductor die substrate is sapphire and the recommended die attach operation uses epoxy die attach adhesive. The eutectic die attach method does not work with sapphire substrates.

Bonding

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about three times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. Aluminum 1-mil wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated. Note the bonding pad material is aluminum.

Shipping Method

Standard die carrier packages and wafer packages are vacuum-sealed with dessicant inside an ESD shielding moisture barrier bag. Sealed product is then placed inside corrugated cardboard box surrounded by bubble wrap or foam for maximum protection during shipment.

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
PE3337-99	D3337	PE3337-DIE-100W	Waffle Pack	Waffle Pack

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel 81-3-3502-5211
Fax 81-3-3502-5213

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).