ADVANCE INFORMATION

PE4460

High Isolation, Non-Blocking 4x6 RF Matrix Switch

Features

- Four inputs at 824 – 924 MHz
- High isolation: 45 dB @ 2 GHz
- High 1 dB compression point of +31 dBm
- High Input IP3 of +50 dBm
- Single 3-volt nominal power supply
- Less than 10 μA current drain
- Simple SPI control bus
- Small 7x7 mm MLPQ package

Product Description

The PE4460 is a high-performance monolithic CMOS switch matrix with integrated power splitters for non-blocking operation. Any of the four RF inputs can be connected to one or more of the six RF outputs simultaneously. With its excellent isolation, small package, and simple interface, the PE4460 is ideal for receiver switching in Cellular/GSM base stations.

The PE4460 is manufactured in Peregrine's patented Ultra-Thin Silicon (UTSi©) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

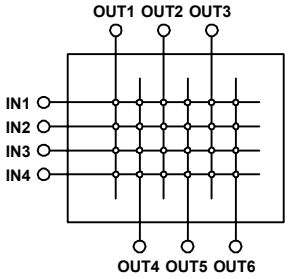


Figure 2. Package Type

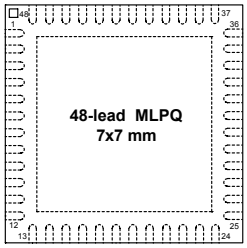


Table 1. Electrical Specifications @ +25 °C (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.7	3.0	3.3	V
Supply Current			1	10	μA
Insertion Loss	824 – 924 MHz		12		dB
Insertion Loss Flatness	824 – 924 MHz		±0.4		dB
Insertion Loss Variation	Any input to any output		±0.4		dB
Isolation	Output to output port with uncommon input port		45		dB
Splitter Isolation	Output to output port with common input port		25		dB

Table 2. Electrical Specifications @ +25 °C -- Continued (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Input 1 dB Compression Pt.			31		dBm
Input IP3			50		dBm
Return Loss	Any input or ON output		13		dB
Switching Time	50% CTL to 90/10% RF		180		ns
Video Feedthrough			15		mV_{pp}
SPI Clock			5	10	MHz

Figure 3. Detailed Functional Schematic Diagram

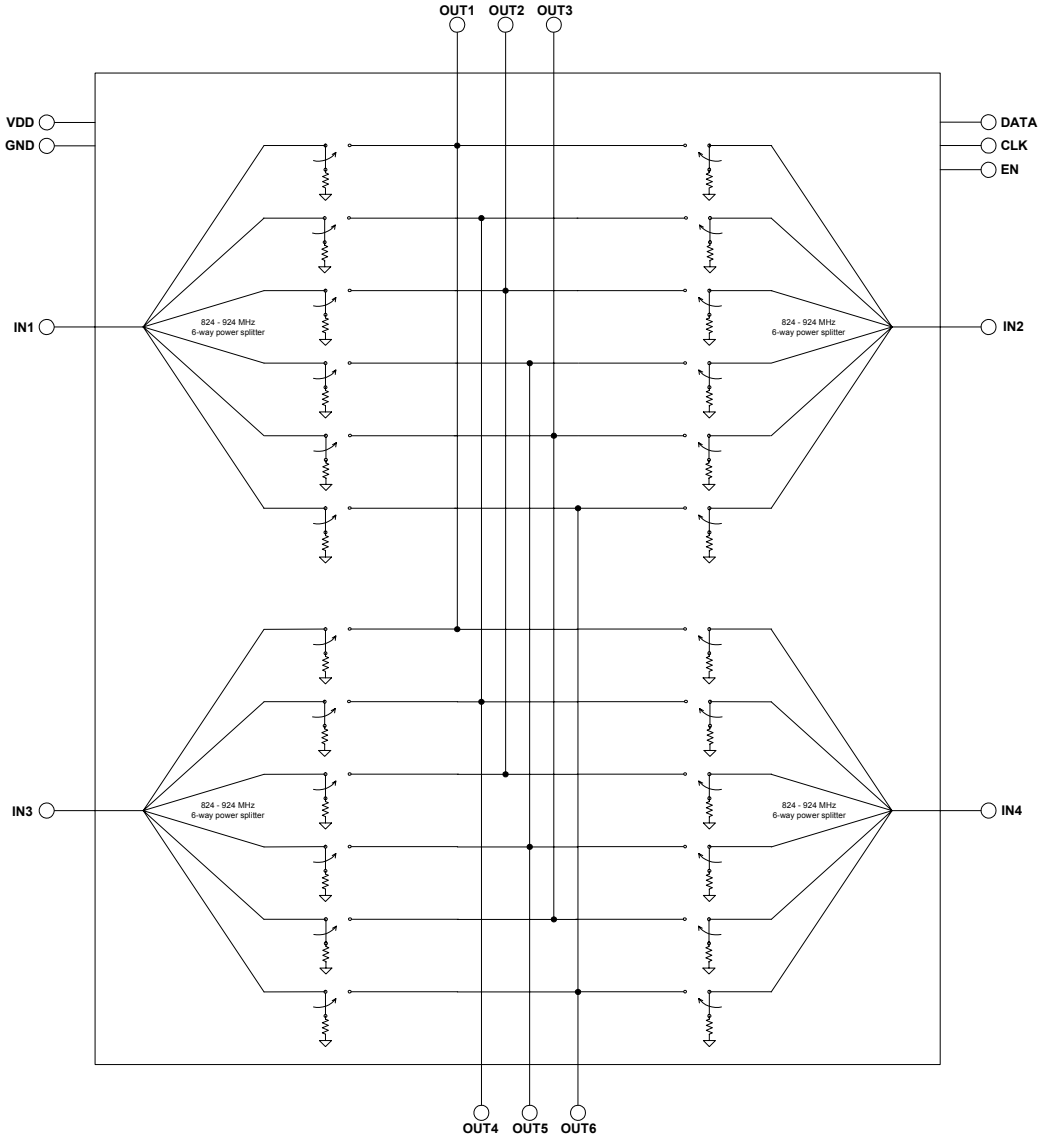


Figure 4. Pin Configuration

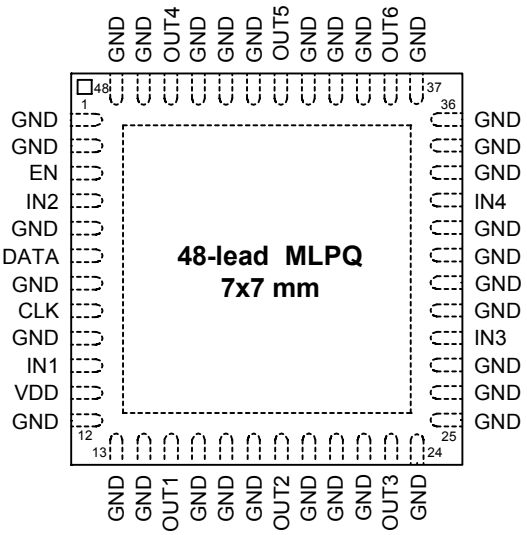


Table 3. Pin Descriptions

Pin No.	Pin Name	Description
3	EN (ENABLE)	Serial register is loaded into parallel register on rising edge of ENABLE control input. RF switches are now reconfigured.
4	IN2	RF input number 2.
6	DATA	DATA is loaded MSB into the 32-bit serial shift register on the falling edge of CLK (CLOCK).
8	CLK (CLOCK)	Falling edge of CLK loads one bit of DATA into the 32-bit serial shift register. Nominal CLK frequency is 5 MHz.
10	IN1	RF input number 1.
11	VDD	Supply voltage input for the matrix switch. This supply pin must be AC shunted to GND as close as possible to the pin.
15	OUT1	RF output number 1.
19	OUT2	RF output number 2.
23	OUT3	RF output number 3.
28	IN3	RF input number 3.
33	IN4	RF input number 4.
38	OUT6	RF output number 6.
42	OUT5	RF output number 5.
46	OUT4	RF output number 4.
All other pins and ground paddle must be grounded. (PINS 1, 2, 5, 7, 9, 12-14, 16-18, 20-22, 24-27, 29-32, 34-37, 39-41, 43-45, 47, 48 are GND pins)		

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
VDD	Supply voltage	-0.3	4.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
Vi	Maximum input voltage	-0.3	VDD+0.3	V
VESD	ESD voltage (Human Body Model)		250	V

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in table.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Device Functional Considerations

The PE4460 offers very high isolation only when care is taken in the PCB layout. Ground fill should isolate all of the RF traces from one another, and the exposed paddle should be soldered to the ground plane.

All of the RF pins must be DC blocked for proper operation.

SPI Programming

The serial programming interface consists of three CMOS compatible signals; input programming data (DATA), the serial bus clock (CLK) and a Latch Enable (EN) control line. A 32-bit data word is serially clocked LSB (B0) first into a control register on the leading edge of the serial bus clock and then captured in the control latch by taking the EN line high (EN=1) and then subsequently low (EN=0).

Each bit (except the unused bits marked by X) controls one RF switch and can connect an input to a selected output by programming that bit high ($B_{(0\text{-}31)}$ = 1) as shown in Table 5. The serial bus timing is shown in Figure 5, *Serial Programming Interface Timing Diagram,* and Table 6, *Serial Interface AC Characteristics.*

For example if bit B3 is programmed high (B3 = 1), then RF Input 1 is connected to RF Output 4.

Table 5. Programming Data Words

DATA Bit	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
	RF Input 4 To:								RF Input 3 To:							
RF Output Port:	X	X	6	5	4	3	2	1	X	X	6	5	4	3	2	1

DATA Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	RF Input 2 To:								RF Input 1 To:							
RF Output Port:	X	X	6	5	4	3	2	1	X	X	6	5	4	3	2	1

Figure 5. Serial Programming Interface Timing Diagram

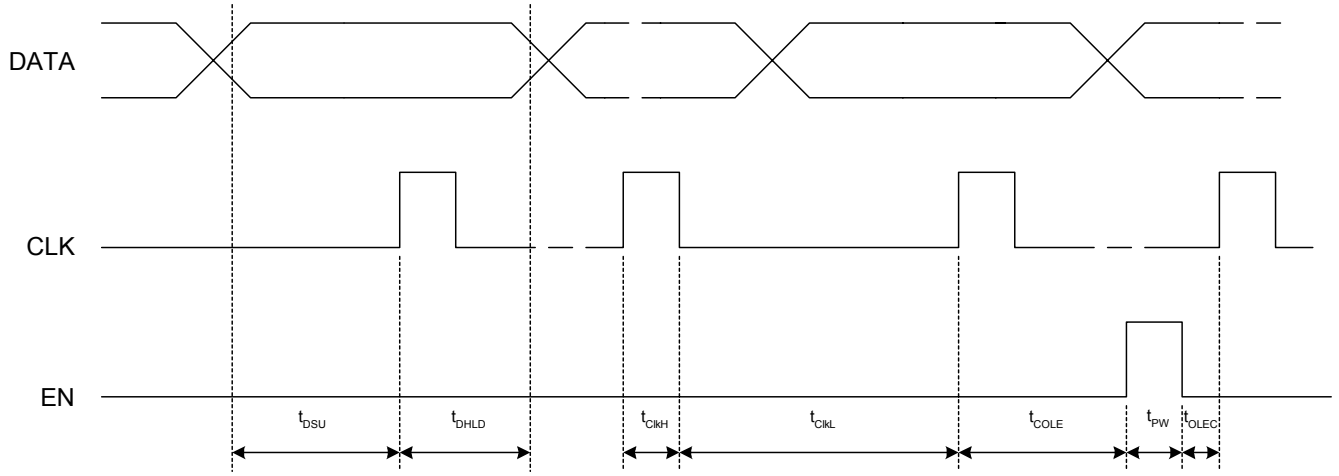


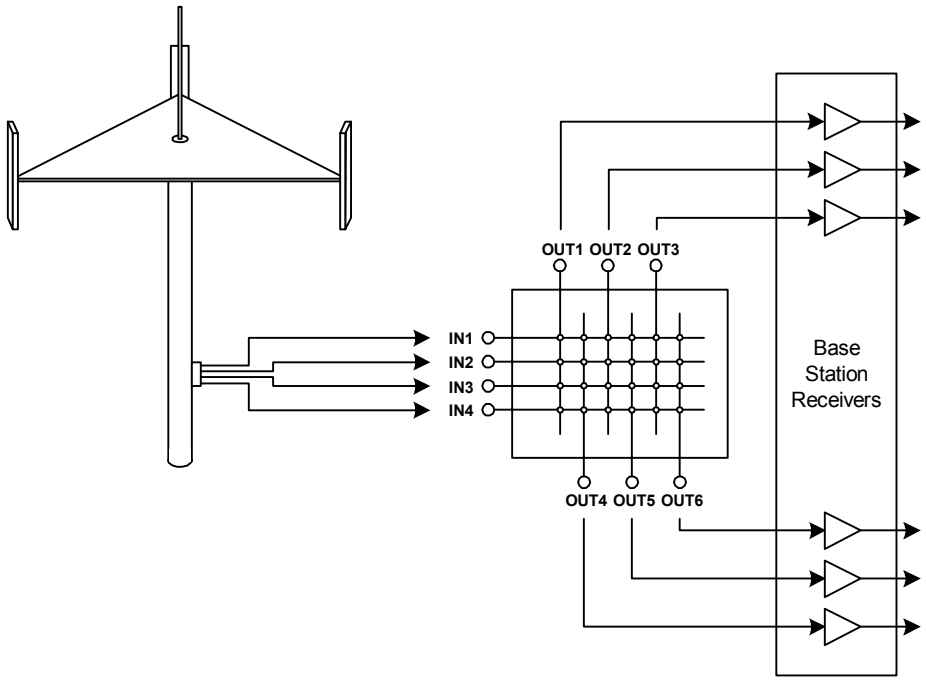
Table 6. Serial Interface AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency (Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time	60		ns
t_{ClkL}	Serial clock LOW time	60		ns
t_{DSU}	Sdata set-up time to Sclk rising edge	20		ns
t_{DHLD}	Sdata hold time after Sclk rising edge	20		ns
t_{PW}	OLE pulse width	60		ns
t_{CWR}	Sclk rising edge to S_WR rising edge	60		ns
t_{OLEC}	OLE falling edge to Sclk rising edge	60		ns

Note 1: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 5 MHz to verify fclk specification.

Figure 6. High Frequency System Application



Typical Performance Data @ +25 °C

Figure 7. Insertion Loss

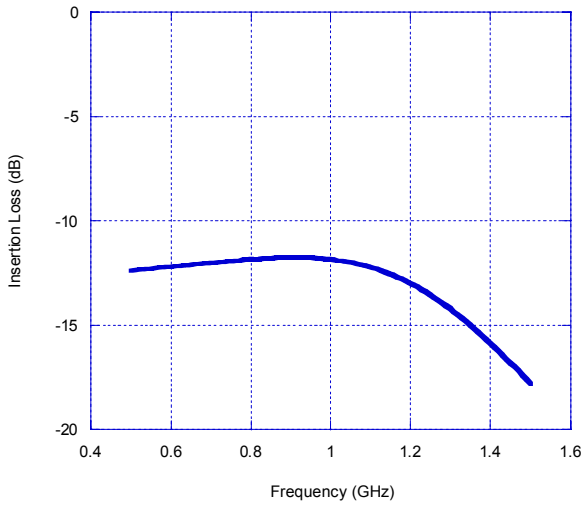


Figure 8. Input 1 dB Compression Point & IIP3

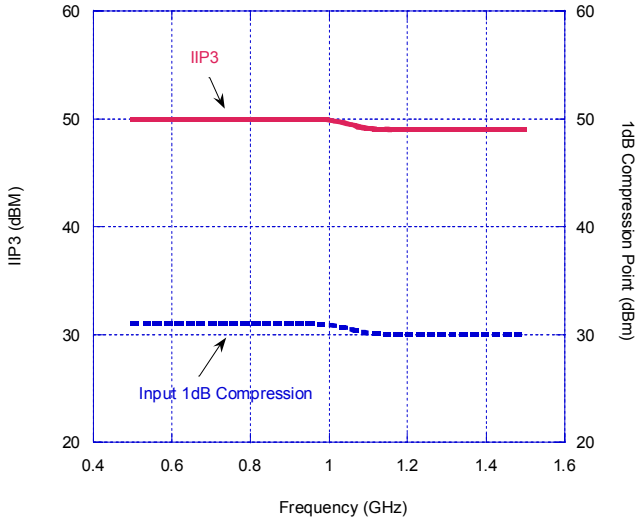


Figure 9. Output to Output Isolation – Different Inputs

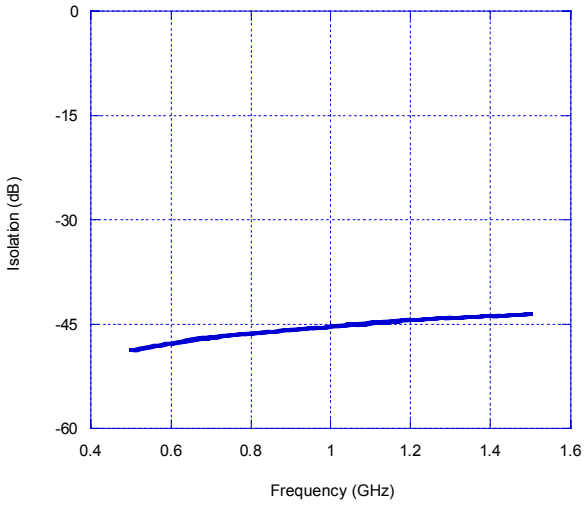
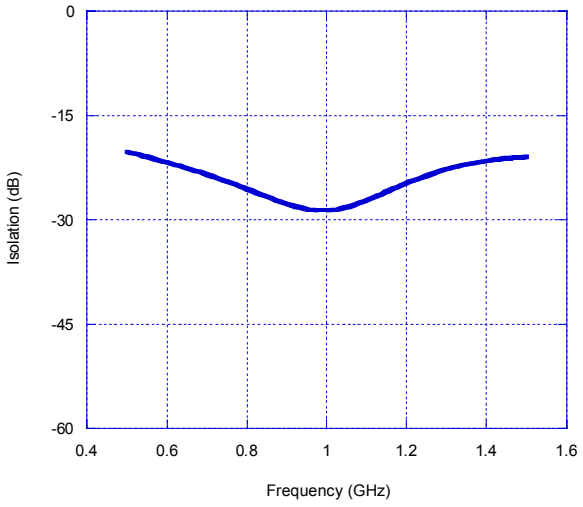


Figure 10. Output to Output Isolation – Common Input



Typical Performance Data @ +25 °C

Figure 11. Input Return Loss

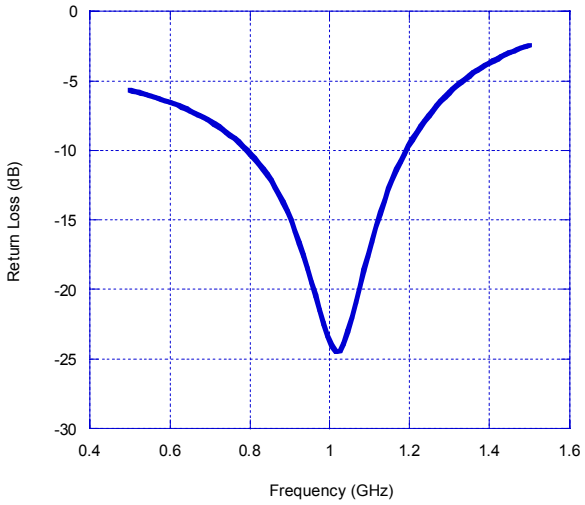


Figure 12. Output Return Loss

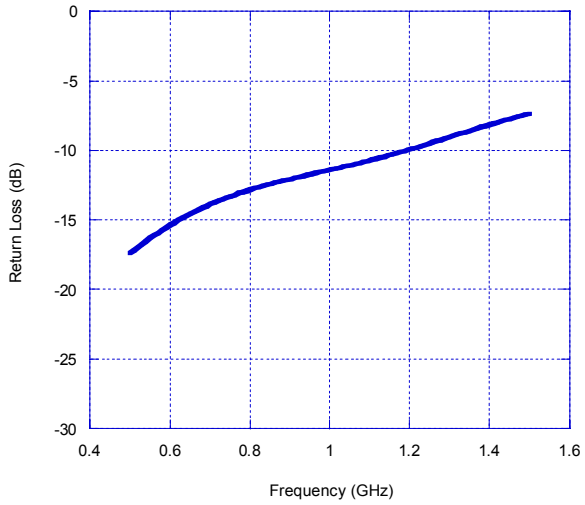
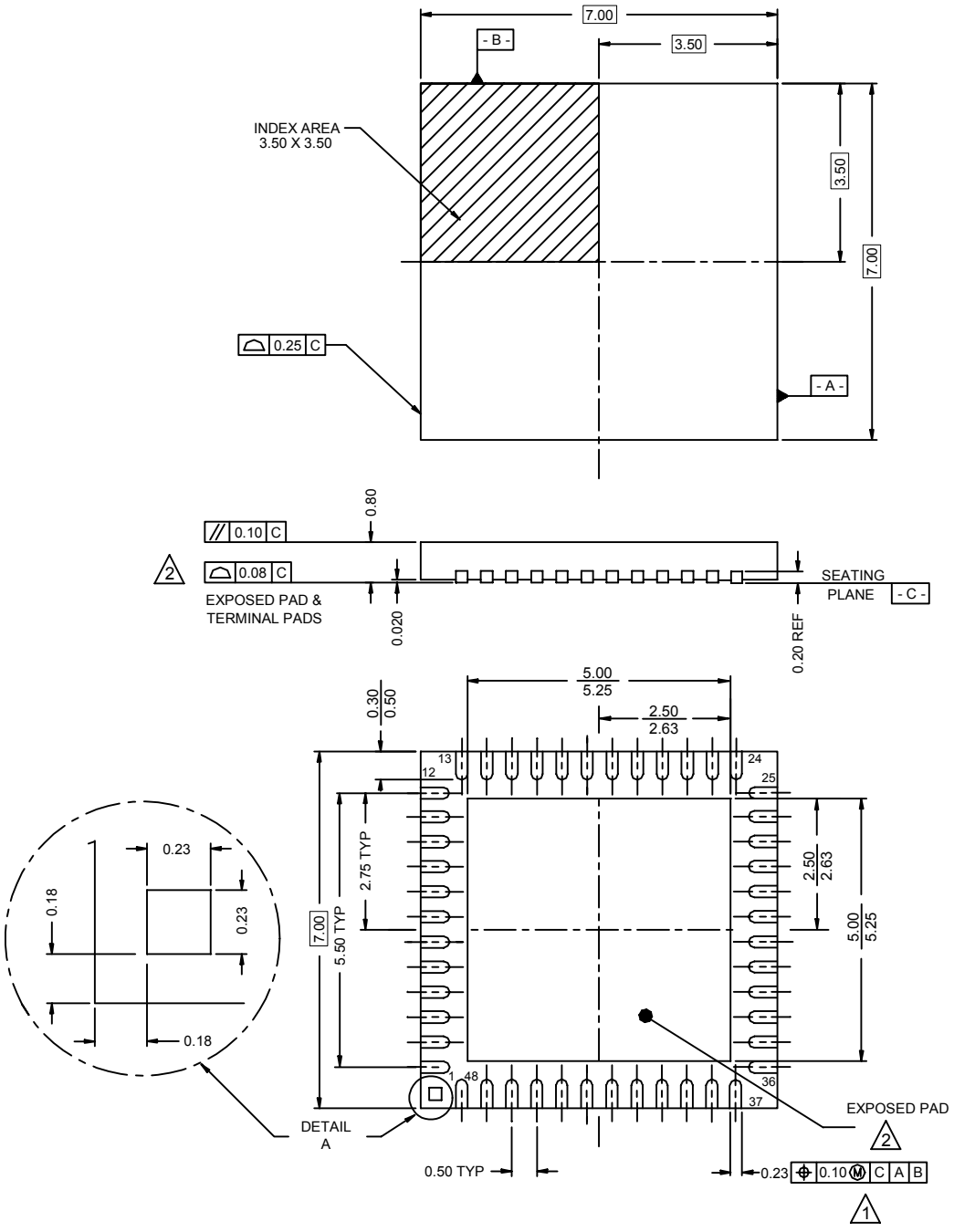


Figure 13. Package Drawing

48 Lead 7x7 mm MLPQ



1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 FROM TERMINAL TIP.

2. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4460-01	PE4460	PE4460-48MLP7X7-4000C	48-lead 7x7 mm MLPQ	4000 pcs. / T&R
4460-02	PE4460	PE4460-48MLP7X7-52A	48-lead 7x7 mm MLPQ	52 pcs. / Tube
4460-00	PE4460-EK	PE4460-48MLP7X7-EK	Evaluation Board	1 / Box

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).