PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

PE83337

Military Operating Temperature Range

3.0 GHz Integer-N PLL for Stringent Military Applications

Features

- 3.0 GHz operation
- ÷10/11 dual modulus prescaler
- Phase detector output
- Serial interface or hardwired programmable
- Ultra-low phase noise
- 44-lead CQFJ

Product Description

Peregrine's PE83337 is a high-performance integer-N PLL capable of frequency synthesis up to 3.0 GHz. The superior phase noise performance of the PE83337 makes it ideal for rugged military environments including: radio handsets, radar, avionics, missiles, etc. The PE83337 also provides an order of magnitude reduction in current consumption, when compared with other military qualified PLLs.

The PE83337 features a ÷10/11 dual modulus prescaler, counters, and a phase comparator as shown in Figure 1. Counter values are programmable through a serial interface, and can also be directly hard wired.

Fabricated in Peregrine's patented UTSi® (Ultra Thin Silicon) CMOS technology, the PE83337, while optimized for stringent military environments, offers excellent RF performance together with the economy and integration of conventional CMOS.

Figure 1. Block Diagram

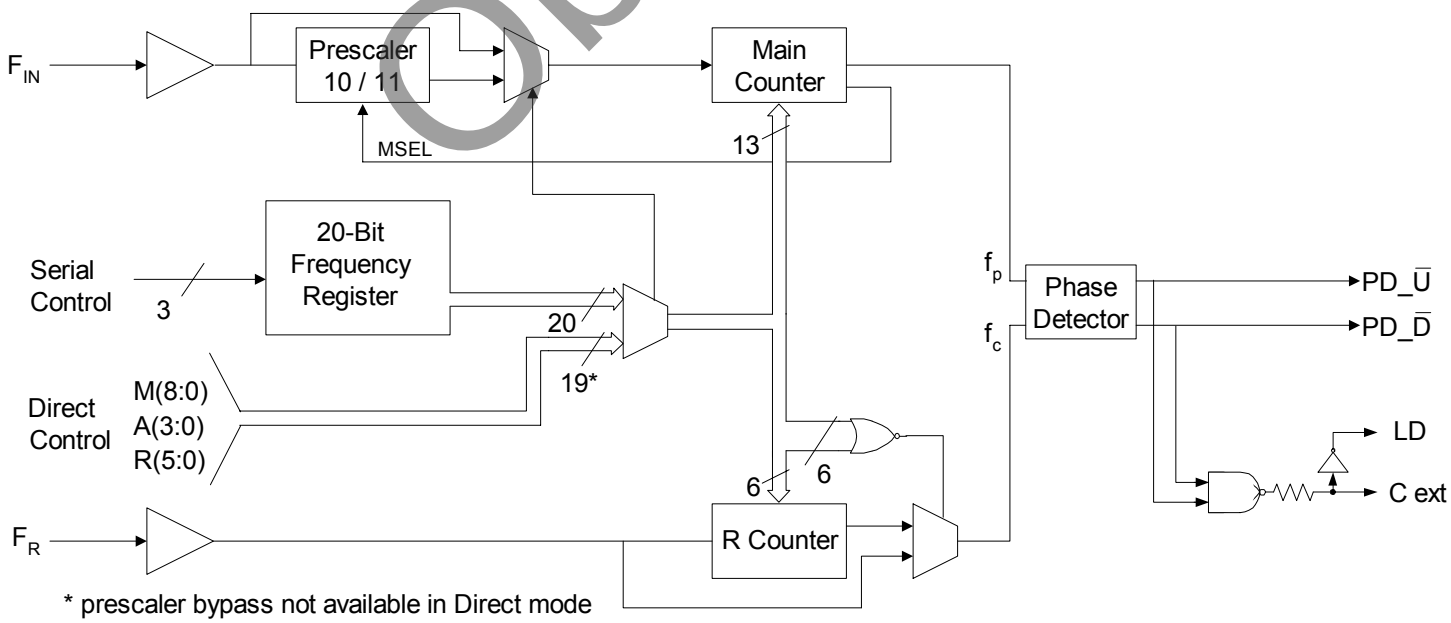


Figure 2. Pin Configuration

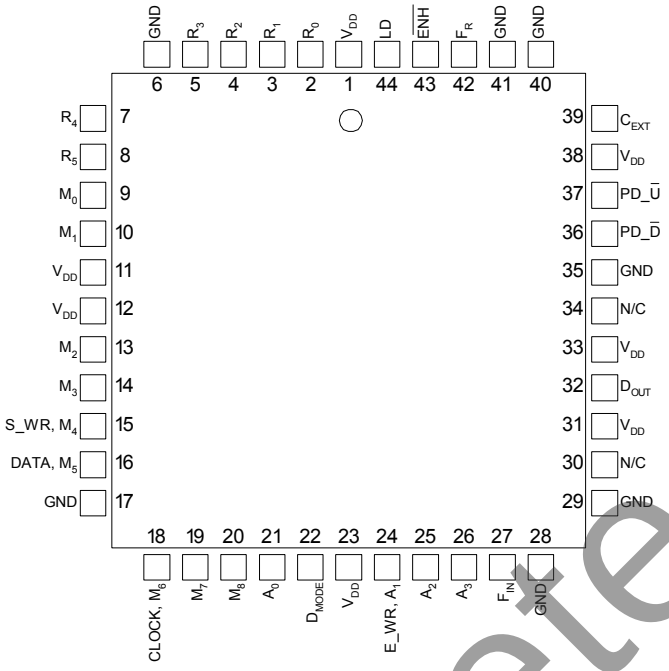


Table 1. Pin Descriptions

Pin No.	Pin Name	Interface Mode	Type	Description
1	V_{DD}	Both	(Note 1)	Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended.
2	R_0	Direct	Input	R Counter bit0
3	R_1	Direct	Input	R Counter bit1
4	R_2	Direct	Input	R Counter bit2
5	R_3	Direct	Input	R Counter bit3
6	GND	Both	(Note 1)	Ground
7	R_4	Direct	Input	R Counter bit4
8	R_5	Direct	Input	R Counter bit5 (MSB)
9	M_0	Direct	Input	M Counter bit0
10	M_1	Direct	Input	M Counter bit1
11	V_{DD}	Both	(Note 1)	Same as pin 1
12	V_{DD}	Both	(Note 1)	Same as pin 1
13	M_2	Direct	Input	M Counter bit2
14	M_3	Direct	Input	M Counter bit3
15	S_WR	Serial	Input	Frequency register load enable input. Buffered data is transferred to the frequency register on S_WR rising edge.
	M_4	Direct	Input	M Counter bit4
16	DATA	Serial	Input	Binary serial data input. Data is entered LSB first, and is clocked serially into the 20-bit frequency control register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of CLOCK.

Pin No.	Pin Name	Interface Mode	Type	Description
	M_5	Direct	Input	M Counter bit5
17	GND	Both		Ground
18	CLOCK	Serial	Input	Clock input. Data is clocked serially into either the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of CLOCK.
	M_6	Direct	Input	M Counter bit6
19	M_7	Direct	Input	M Counter bit7
20	M_8	Direct	Input	M Counter bit8 (MSB)
21	A_0	Direct	Input	A Counter bit0
22	D_{MODE}	Both	Input	Selects direct interface mode (D_{MODE}=1) or serial interface mode (D_{MODE}=0)
23	V_{DD}	Both	(Note 1)	Same as pin 1
24	E_WR	Serial	Input	Enhancement register write enable. While E_WR is "high", DATA can be serially clocked into the enhancement register on the rising edge of CLOCK.
	A_1	Direct	Input	A Counter bit1.
25	A_2	Direct	Input	A Counter bit2
26	A_3	Direct	Input	A Counter bit3 (MSB)
27	F_{IN}	Both	Input	RF prescaler input from the VCO. 3.0 GHz maximum frequency.
28	GND	Both		Ground.
29	GND	Both		Ground.
30	N/C			No connect.
31	V_{DD}	Both	(Note 1)	Same as pin 1
32	D_{OUT}	Serial	Output	Data Out. The Main Counter output, R Counter output, or dual modulus prescaler select (MSEL) can be routed to D_{OUT} through enhancement register programming.
33	V_{DD}	Both	(Note 1)	Same as pin 1
34	N/C			No connect.
35	GND	Both		Ground.
36	PD_D	Both	Output	PD_D pulses down when f_p leads f_c.
37	PD_U	Both		PD_U pulses down when f_c leads f_p.
38	V_{DD}	Both	(Note 1)	Same as pin 1
39	C_{EXT}	Both	Output	Logical "NAND" of PD_U and PD_D, passed through an on-chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
40	GND	Both		Ground
41	GND	Both		Ground
42	F_R	Both	Input	Reference frequency input
43	ENH	Both	Output, OD	Enhancement mode. When asserted low ("0"), enhancement register bits are functional.
44	LD	Serial	Output	Lock detect output, the open-drain logical inversion of C_{EXT}. When the loop is locked, LD is high impedance; otherwise LD is a logic low ("0").

Note 1: V_{DD} pins 1, 11, 12, 23, 31, 33, 35, and 38 are connected by diodes and must be supplied with the same positive voltage level.

Note 2: All digital input pins have 70 kΩ pull-down resistors to ground.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD} + 0.3	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
T_{stg}	Storage temperature range	-65	150	°C

Table 3. Operating Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.15	V
T_A	Operating ambient temperature range	-55	125	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Level	Units
V_{ESD}	ESD voltage (Human Body Model) – Note 1	1000	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this *UTSi* ® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, *UTSi* ® CMOS devices are immune to latch-up.

Table 5. DC Characteristics

V_{DD} = 3.0 V, -55° C ≤ T_A ≤ 125° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current; Prescaler disabled Prescaler enabled	V_{DD} = 2.85 to 3.15 V		 10 24	 31	 mA mA
Digital Inputs: All except F_R, F_{IN} (all digital inputs have 70k ohm pull-up resistors)						
V_{IH}	High level input voltage	V_{DD} = 2.85 to 3.15 V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85 to 3.15 V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.15 V			1	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.15 V	-70			µA
Reference Divider input: F_R						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.15 V			+100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.15 V	-100			µA
Counter and phase detector outputs: f_c, f_p.						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = -3 mA	V_{DD} - 0.4			V
Lock detect outputs: C_{EXT}, LD						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{out} = 100 µ			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{out} = -100 µ	V_{DD} - 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 6 mA			0.4	V

Table 6. AC Characteristics

V_{DD} = 3.0 V, -55° C ≤ T_A ≤ 125° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
Control Interface and Latches (see Figures 1and 3)					
f_{Clk}	CLOCK Serial data clock frequency	(Note 1)		10	MHz
t_{ClkH}	CLOCK Serial clock HIGH time		30		ns
t_{ClkL}	CLOCK Serial clock LOW time		30		ns
t_{DSU}	DATA set-up time after CLOCK rising edge		10		ns
t_{DHLD}	DATA hold time after CLOCK rising edge		10		ns
t_{PW}	S_WR pulse width		30		ns
t_{CWR}	CLOCK rising edge to S_WR rising edge.		30		ns
t_{CE}	CLOCK falling edge to E_WR transition		30		ns
t_{WRC}	S_WR falling edge to CLOCK rising edge.		30		ns
t_{EC}	E_WR transition to CLOCK rising edge		30		ns
t_{MDO}	MSEL data out delay after F_{IN} rising edge	C_L = 12 pf		8 (Note 5)	ns
Main Divider (Including Prescaler)					
F_{IN}	Operating frequency		500	3000	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Main Divider (Prescaler Bypassed)					
F_{IN}	Operating frequency		50	300	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Reference Divider					
F_R	Operating frequency	(Note 3)		100	MHz
P_{Fr}	Reference input power (Note 2)	Single-ended input	-2		dBm
Phase Detector					
f_c	Comparison frequency	(Note 3)		20	MHz
SSB Phase Noise : Output Referred (F_{in} = 1918MHz, f_r = 10 MHz, f_c = 1MHz, LBW = 70 kHz)					
PN_{OR}	Output Referred Phase Noise	100 Hz Offset: V_{DD} = 3.0V, T = 25ºC	-78	(Note 4)	dBc/Hz
PN_{OR}	Output Referred Phase Noise	1000 Hz Offset: V_{DD} = 3.0V, T = 25ºC	-83	(Note 4)	dBc/Hz

Note 1: Fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify Fclk specification.

Note 2: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of $0.5V_{p-p}$.

Note 3: Parameter is guaranteed through characterization only and is not tested.

Note 4: All devices are screened to phase noise limits listed in Table 7. The magnitude of the tester uncertainty precludes testing phase noise as part of qualification testing. These parameters are also exempt from PDA requirements.

Note 5: Parameter is tested using 100pF load capacitance and is guaranteed through characterization only. Typical test delay is 12nS.

Table 7. Phase Noise Test

Test name	Conditions	Max	Units
Phase Noise	100 Hz Offset	-68	dBc/Hz
	1000 Hz Offset	-78	dBc/Hz

Functional Description

The *PE83337* consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters "R" and "M" divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter ("A") is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via a serial bus or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

Main Counter Chain

Normal Operating Mode

Setting the PB control bit "low" enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (F_{IN}) by an integer derived from the values in the "M" and "A" counters.

In this mode, the output from the main counter chain (f_p) is related to the VCO frequency (F_{IN}) by the following equation:

$$f_p = F_{IN} / [10 \times (M + 1) + A] \quad (1)$$
where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{IN} = [10 \times (M + 1) + A] \times (F_R / (R+1)) \quad (2)$$
where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that F_{IN} must be greater than or equal to 90 x (F_R / (R+1)) to obtain contiguous channels. The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode

Setting the frequency control register bit PB "high" allows F_{IN} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. This mode is only available when using the serial port to set the frequency control bits. The following equation relates F_{IN} to the reference frequency F_R:

$$F_{IN} = (M + 1) \times (F_R / (R+1))) \quad (3)$$
where $1 \leq M \leq 511$

Reference Counter

The reference counter chain divides the reference frequency F_R down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \quad (4)$$
where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency (F_R) directly to the phase detector.

Register Programming

Serial Interface Mode

Serial Interface Mode is selected by setting the D_{MODE} input "low".

While the E_WR input is "low", serial data (DATA input), B_0 to B_{19}, is clocked into a buffer register on the rising edge of CLOCK, LSB (B_0) first. The contents from this buffer register are transferred into the frequency control register on the rising edge of S_WR according to the timing diagram shown in Figure 3. This data controls the counters as shown in Table 7.

While the E_WR input is "high", serial data (DATA input), B_0 to B_7, is clocked into a buffer register on the rising edge of CLOCK, LSB (B_0) first. The contents from this buffer register are transferred into the enhancement register on the falling edge of E_WR according to the timing diagram shown in Figure 3. After the falling edge of E_WR, the data provides control bits as shown in Table 8. These bits are active when the Enh input is "low".

Direct Interface Mode

Direct Interface Mode is selected by setting the D_{MODE} input "high". In this mode, the counter values are set directly at external pins as shown in Table 7 and Figure 2. All frequency control register bits are addressable except PB (it is not possible to bypass the ÷10/11 dual modulus prescaler in Direct Mode).

Table 8. Frequency Register Programming

Interface Mode	Enh	D_{MODE}	R_5	R_4	M_8	M_7	PB	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Serial*	1	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}
Direct	1	1	R_5	R_4	M_8	M_7	0	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0

* Data is clocked serially on CLOCK rising edge while E_WR is "low" and transferred to frequency register on S_WR rising edge.

LSB (first in) ↑ ↑ MSB (last in)

Table 9. Enhancement Register Programming

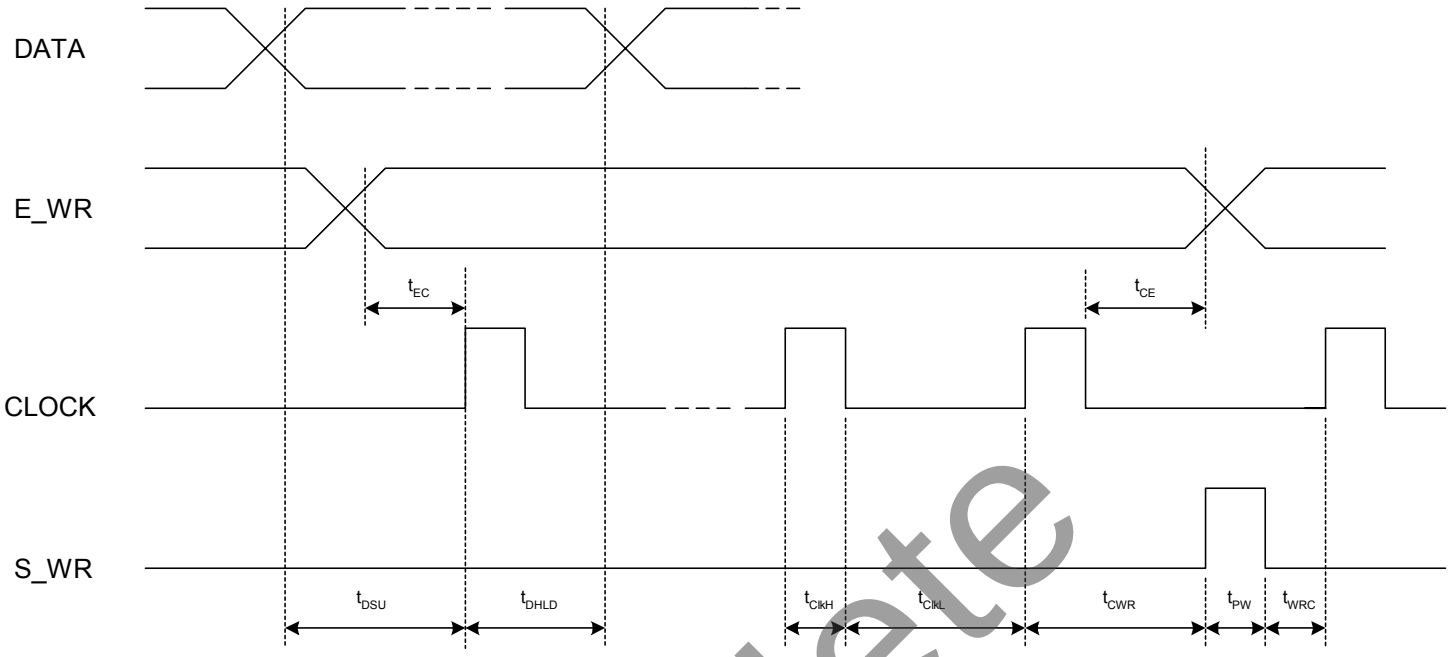
Interface Mode	Enh	D_{MODE}	Reserved*	Reserved*	fp output	Power down	Counter load	MSEL output	fc output	Reserved*
Serial**	0	X	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

* Program to 0

* Data is clocked serially on CLOCK rising edge while E_WR is "low" and transferred to frequency register on S_WR rising edge.

LSB (first in) ↑ ↑ MSB (last in)

Figure 3. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below. All bits are active high. Operation is undefined if more than one output is sent to D_{OUT}.

Table 10. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved**	
Bit 1	Reserved**	
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the R counter output onto the D_{OUT} output
Bit 7	Reserved**	

** Program to 0

Phase Detector Outputs

The phase detector is triggered by rising edges from the main counter (f_p) and the reference counter (f_c). It has two outputs, PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses "low". If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_U pulses "low". The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c. The phase detector gain is 430 mV / radian.

PD_U and PD_D are designed to drive an active loop filter which controls the VCO tune voltage. PD_U pulses result in an increase in VCO frequency and PD_D results in a decrease in VCO frequency.

Software tools for designing the active loop filter can be found at Peregrine's web site (www.peregrine-semi.com).

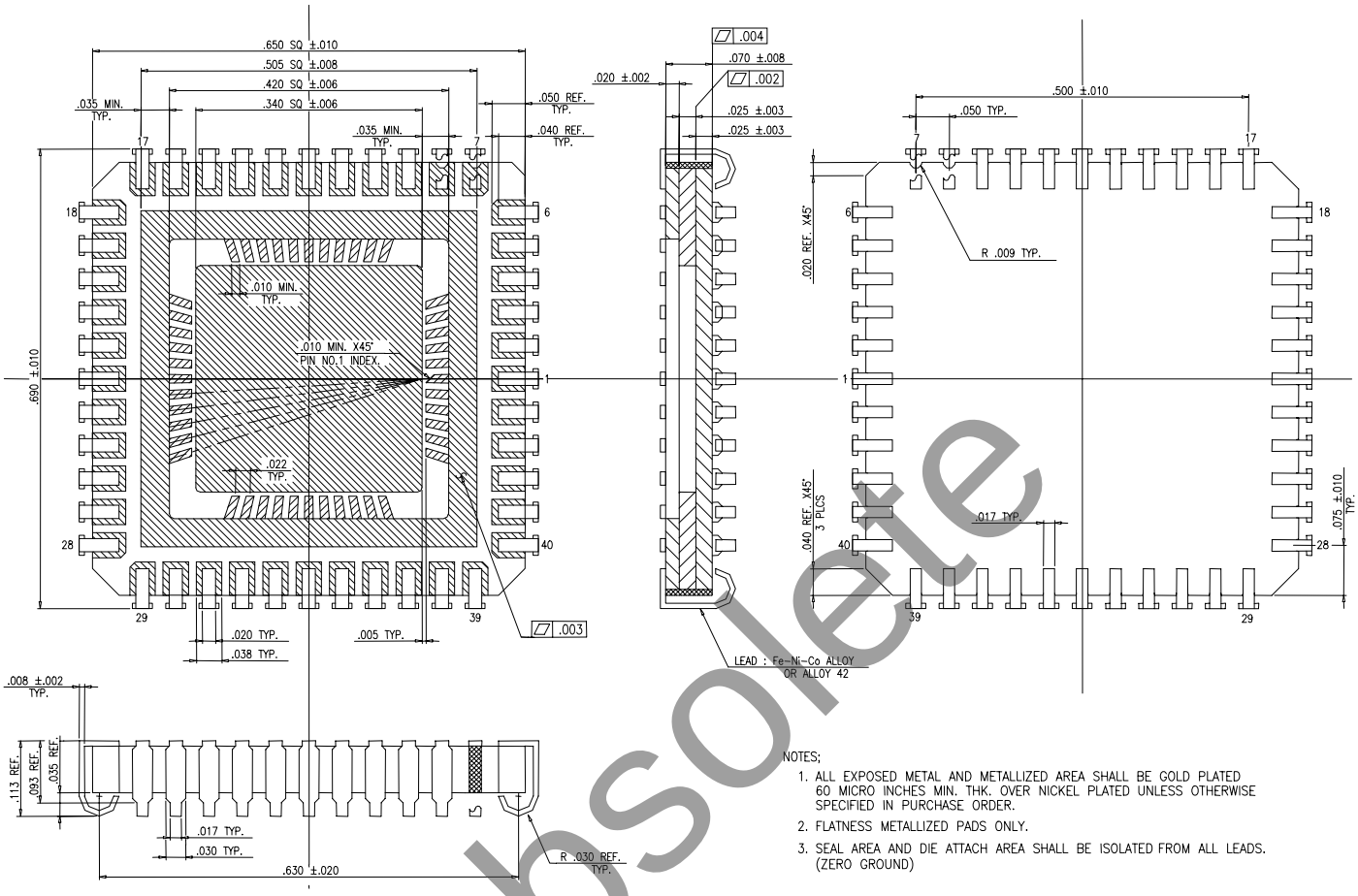
Lock Detect Output

A lock detect signal is provided at pin LD, via the pin C_{EXT} (see Figure 1). C_{EXT} is the logical "NAND" of PD_U and PD_D waveforms, driven through a series 2k ohm resistor. Connecting C_{EXT} to an external shunt capacitor provides integration of this signal.

The C_{EXT} signal is then sent to the LD pin through an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_U and PD_D.

Figure 4. Package Drawing

44-lead CQFJ



All dimensions are in mils

Table 11. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
83337-01ES	PE83337 ES	Engineering Samples	44-pin CQFJ	40 units / Tray
83337-01	PE83337	Production Units	44-pin CQFJ	40 units / Tray
83337-00	PE83337 EK	Evaluation Kit		1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents are pending.