PE83363

Military Operating Temperature Range

3.0 GHz Delta-Sigma modulated Fractional-N Synthesizer for Low Phase Noise Applications

Features

- 3.0 GHz operation
- ÷10/11 dual modulus prescaler
- Selectable phase detector or charge pump output
- Serial or Direct Mode interface
- Frequency resolution:
  - Comparison frequency / 2^{18}
- Low power — 25 - 30 mA at 3V (phase detector / charge pump)
- 50MHz Phase Comparator
- Ultra-low phase noise
- 68-lead CQFJ

Product Description

Peregrine's PE83363 is a high performance fractional-N PLL capable of frequency synthesis up to 3.0 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with the existing military PLLs.

The PE83363 features a 10/11 dual modulus prescaler, counters, a delta sigma modulator, a phase comparator and a charge pump as shown in Figure 1. Counter values are programmable through either a serial interface or directly hard-wired.

Fabricated in Peregrine's patented UTSi® (Ultra Thin Silicon) CMOS technology, the PE83363 offers excellent RF performance and versatility.

Figure 1. Block Diagram

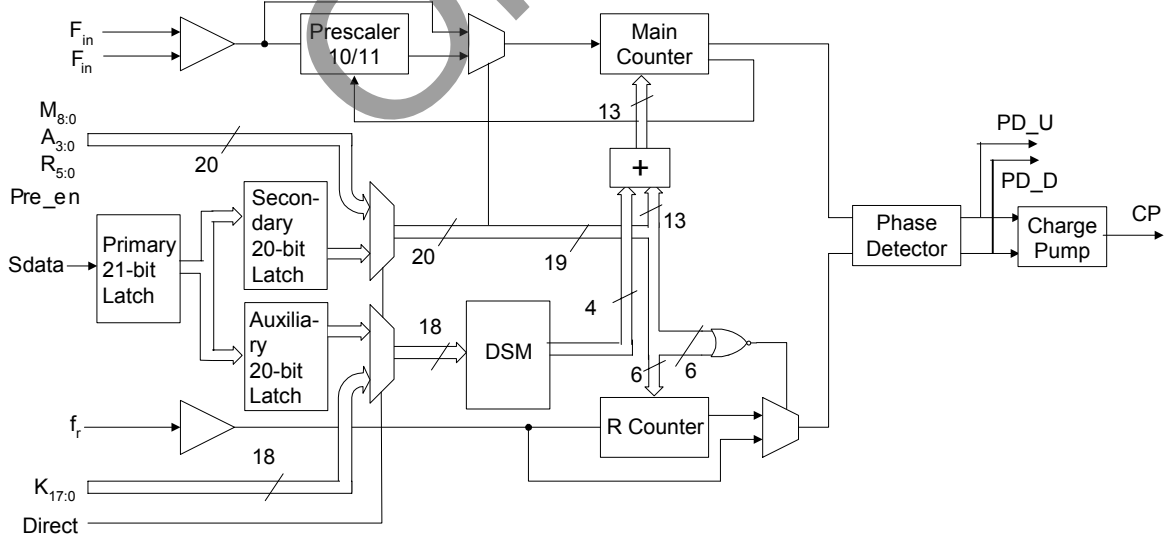


Figure 2. Pin Configuration

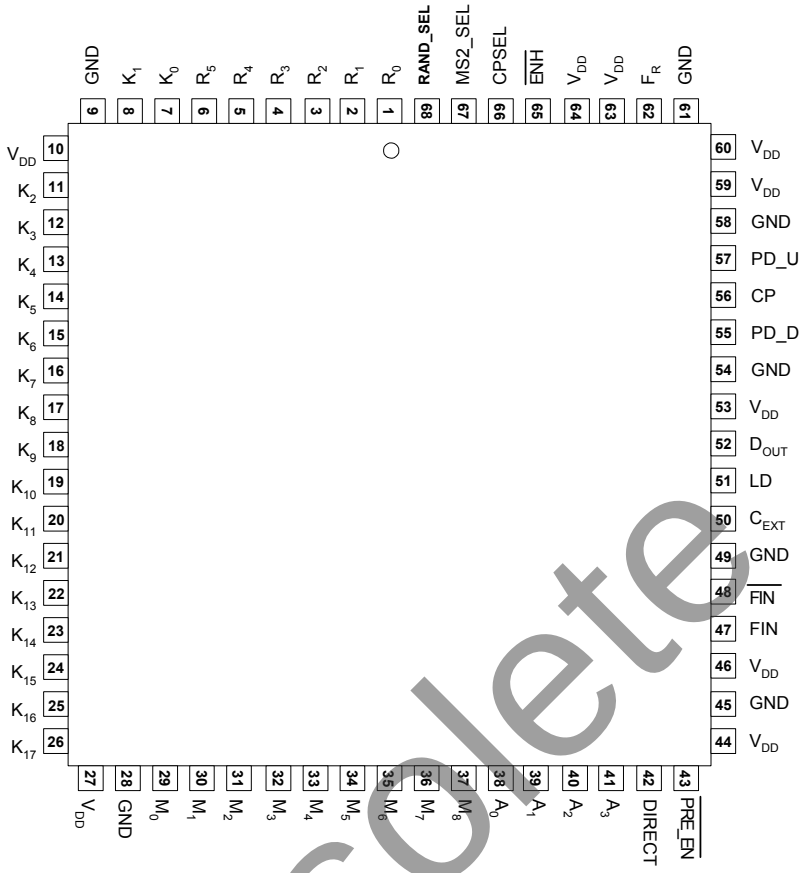


Table 1. Pin Descriptions

Pin No. (68-lead CQFJ)	Pin Name	Valid Mode	Type	Description
1	R_0	Direct	Input	R Counter bit0 (LSB).
2	R_1	Direct	Input	R Counter bit1.
3	R_2	Direct	Input	R Counter bit2.
4	R_3	Direct	Input	R Counter bit3.
5	R_4	Direct	Input	R Counter bit4.
6	R_5	Direct	Input	R Counter bit5 (MSB).
7	K_0	Direct	Input	K Counter bit0 (LSB).
8	K_1	Direct	Input	K Counter bit1.
9	GND		Power	Ground.
10	V_{DD}		Power (Note 1)	ESD & Digital core V_{DD}.
11	K_2	Direct	Input	K Counter bit2.
12	K_3	Direct	Input	K Counter bit3.
13	K_4	Direct	Input	K Counter bit4.

Pin No. (68-lead CQFJ)	Pin Name	Valid Mode	Type	Description
14	K_5	Direct	Input	K Counter bit5.
15	K_6	Direct	Input	K Counter bit6.
16	K_7	Direct	Input	K Counter bit7.
17	K_8	Direct	Input	K Counter bit8.
18	K_9	Direct	Input	K Counter bit9.
19	K_{10}	Direct	Input	K Counter bit10.
20	K_{11}	Direct	Input	K Counter bit11.
21	K_{12}	Direct	Input	K Counter bit12.
22	K_{13}	Direct	Input	K Counter bit13.
23	K_{14}	Direct	Input	K Counter bit14.
24	K_{15}	Direct	Input	K Counter bit15.
25	K_{16}	Direct	Input	K Counter bit16.
26	K_{17}	Direct	Input	K Counter bit17 (MSB).
27	V_{DD}		Power	Digital core & ESD V_{DD}.
28	GND		Power	Ground.
29	M_0	Direct	Input	M Counter bit0 (LSB).
30	M_1	Direct	Input	M Counter bit1.
31	M_2	Direct	Input	M Counter bit2
32	M_3	Direct	Input	M Counter bit3.
33	M_4	Direct	Input	M Counter bit4.
	S_WR	Serial	Input	Serial load enable input. While S_WR is “low”, Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR or Hop_WR rising edge.
34	M_5	Direct	Input	M Counter bit5.
	SDATA	Serial	Input	Binary serial data input. Input data entered MSB first.
35	M_6	Direct	Input	M Counter bit6.
	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into the 20-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of Sclk.
36	M_7	Direct	Input	M Counter bit7.
37	M_8	Direct	Input	M Counter bit8 (MSB).
38	A_0	Direct	Input	A Counter bit0 (LSB).
39	A_1	Direct	Input	A Counter bit1.
	E_WR	Serial	Input	Enhancement register write enable. While E_WR is “high”, Sdata can be serially clocked into the enhancement register on the rising edge of Sclk.
40	A_2	Direct	Input	A Counter bit2.
41	A_3	Direct	Input	A Counter bit3 (MSB).
42	DIRECT	Both	Input	Direct mode select. “High” enables direct mode. “Low” enables serial mode.
43	$\overline{\text{Pre\_en}}$	Direct	Input	Prescaler enable, active “low”. When “high”, Fin bypasses the prescaler.

Pin No. (68-lead CQFJ)	Pin Name	Valid Mode	Type	Description
44	V_{DD}		Power (Note 1)	Digital core V_{DD}.
45	GND		Power	Ground.
46	V_{DD}		Power (Note 1)	ESD & Prescaler V_{DD}.
47	F_{in}	Both	Input	Prescaler input from the VCO. 3.0 GHz max frequency.
48	$\overline{F_{in}}$	Both	Input	Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor directly to the ground plane.
49	GND		Power	Ground.
50	CEXT	Both	Output	Logical "NAND" of PD_U and PD_D terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Both	Output	Lock detect and open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0").
52	D_{OUT}	Both	Output	Data out function, enabled in enhancement mode.
53	V_{DD}		(Note 1)	Output driver/charge pump V_{DD}.
54	GND		Power	Ground.
55	PD_D	Both	Output	PD_D pulses down when f_p leads f_c. PD_U is driven to GND when CPSEL = "High".
56	CP	Both	Output	Charge pump output. Selected when CPSEL = "1". Tristate when CPSEL = "Low".
57	PD_U	Both	Output	PD_U pulses down when f_c leads f_p. PD_D is driven to GND when CPSEL = "High".
58	GND		Power	Ground.
59	V_{DD}		Power (Note 1)	Output driver/charge pump V_{DD}.
60	V_{DD}		Power (Note 1)	Phase detector & ESD V_{DD}.
61	GND		Power	Ground.
62	f_r	Both	Input	Reference frequency input.
63	V_{DD}		Power (Note 1)	Reference V_{DD}.
64	V_{DD}		Power (Note 1)	Digital core V_{DD}.
65	$\overline{ENH}$	Both	Input	Enhancement mode. When asserted low ("0"), enhancement register bits are functional.
66	CPSEL	Both	Input	Charge pump select. "High" enables the charge pump and disables pins PD_U and PD_D by forcing them "low". A "low" Tri-states the CP and enables PD_U and PD_D.
67	MS2_SEL	Both	Input	MASH 1-1 select. "High" selects MASH 1-1 mode. "Low" selects the MASH 1-1-1 mode.
68	RND_SEL	Both	Input	K register LSB toggle enable. "1" enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the phase detector comparison frequency / 2^{19}.

Note 1: All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.

Note 2: All digital input pins have 70 kΩ pull-down resistors to ground.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD} + 0.3	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
T_{stg}	Storage temperature range	-65	150	°C

Table 3. Operating Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.15	V
T_A	Operating ambient temperature range	-55	125	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Level	Units
V_{ESD}	ESD voltage human body model (Note 1)	1000	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 5. DC Characteristics

V_{DD} = 3.0 V, -55° C < T_A < 125° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current; Prescaler enabled, charge pump disabled	V_{DD} = 2.85 to 3.15 V		25		mA
I_{DD}	Operational supply current; Prescaler enabled, charge pump enabled	V_{DD} = 2.85 to 3.15 V		30		mA
I_{DD}	Operational supply current; Prescaler disabled, charge pump disabled	V_{DD} = 2.85 to 3.15 V		10		mA
I_{DD}	Operational supply current; Prescaler disabled, charge pump enabled	V_{DD} = 2.85 to 3.15 V		15		mA
All Digital inputs: K[17:0], R[5:0], M[8:0], A[3:0], Direct, Pre_en, Rand_en, M2_sel, Cpsel, Enh (contains a 70 kΩ pull-down resistor)						
V_{IH}	High level input voltage	V_{DD} = 2.85 to 3.15 V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85 to 3.15 V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.15 V			+100	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.15 V	-1			µA
Reference Divider input: f_r						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.15 V			+100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.15 V	-100			µA
Counter and phase detector outputs: PD_D, PD_U						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = +3 mA	V_{DD} - 0.4			V
Digital test outputs: Dout						
V_{OLD}	Output voltage LOW	I_{out} = -200 µA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = 200 µA	V_{DD} - 0.4			V
Charge Pump output: CP						
I_{CP} - Source	Drive current	V_{CP} = V_{DD} / 2	-2.6	2	-1.4	mA
I_{CP} -Sink	Drive current	V_{CP} = V_{DD} / 2	1.4	2	2.6	mA
I_{CPL}	Leakage current	1.0 V < V_{CP} < V_{DD} – 1.0 V	-1		1	µA
I_{CP} - Source vs. I_{CP} - Sink	Sink vs. source mismatch	V_{CP} = V_{DD} / 2 T_A = 25° C			15	%
I_{CP} vs. V_{CP}	Output current magnitude variation vs. voltage	1.0 V < V_{CP} < V_{DD} – 1.0 V T_A = 25° C			15	%
Lock detect outputs: (Cext, LD)						
V_{OLC}	Output voltage LOW, Cext	I_{out} = -0.1 mA			0.4	V
V_{OHC}	Output voltage HIGH, Cext	I_{out} = 0.1 mA	V_{DD} - 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 1 mA			0.4	V

Table 6. AC Characteristics

V_{DD} = 3.0 V, -55° C < T_A < 125° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Control Interface and Latches (see Figures 3, 4)						
f_{Clk}	Serial data clock frequency	(Note 1)			10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	Sdata set-up time to Sclk rising edge		10			ns
t_{DHLD}	Sdata hold time after Sclk rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	Sclk rising edge to S_WR rising edge		30			ns
t_{CE}	Sclk falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to Sclk rising edge		30			ns
t_{EC}	E_WR transition to Sclk rising edge		30			ns
Main Divider (Including Prescaler)						
F_{in}	Operating frequency		275		3000	MHz
P_{Fin}	Input level range	External AC coupling	-5		5	dBm
Main Divider (Prescaler Bypassed)						
F_{in}	Operating frequency		50		300	MHz
P_{Fin}	Input level range	External AC coupling	-5		5	dBm
Reference Divider						
f_r	Operating frequency	(Note 3)			100	MHz
P_{fr}	Reference input power (Note 2)	Single ended input	-2			dBm
Phase Detector						
f_c	Comparison frequency	(Note 3)			50	MHz
SSB Phase Noise (F_{in} = 1.9 GHz, f_r = 20 MHz, f_c = 10 MHz, LBW = 50 kHz, V_{DD} = 3.0 V, Temp = 25° C)						
Φ_N	Phase Noise	1 kHz Offset		-88		dBc/Hz
Φ_N	Phase Noise	10 kHz Offset		-92		dBc/Hz

Note 1: fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.

Note 2: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5 Vp-p. For optimum phase noise performance, the reference input falling edge rate should be faster than 80mV/ns.

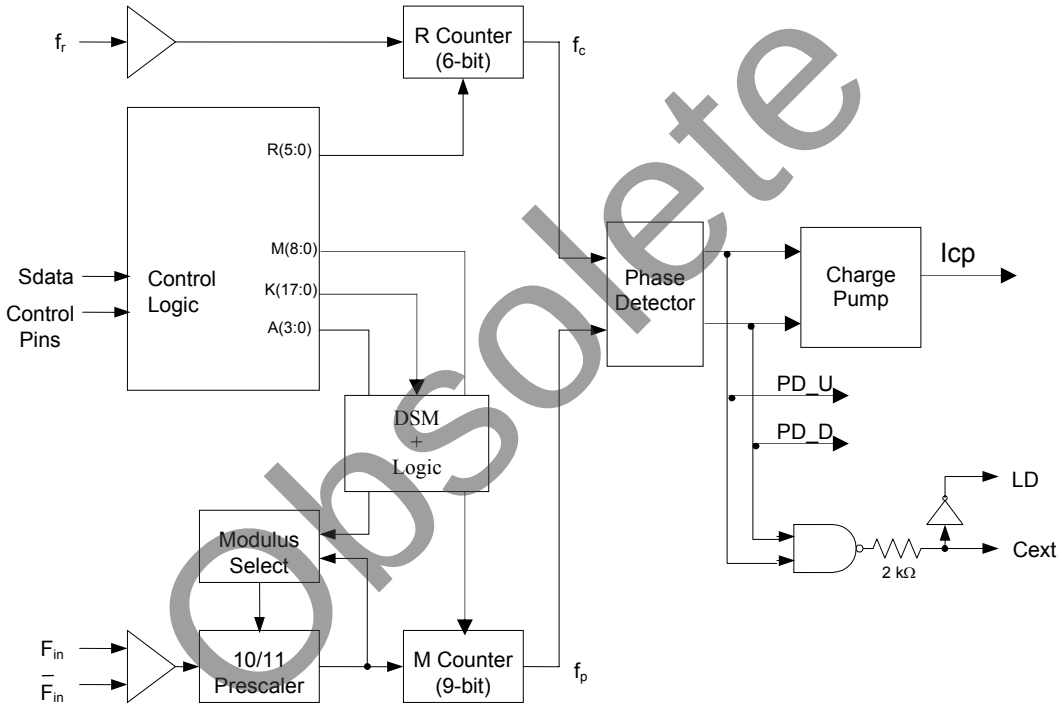
Note 3: Parameter is guaranteed through characterization only and is not tested.

Functional Description

The PE83363 consists of a prescaler, counters, an 18-bit delta-sigma modulator (DSM), a phase detector and a charge pump. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The DSM modulates the “A” counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. These signals can be configured to drive a tri-state charge pump. Data is written into the internal registers via the three wire serial bus or set directly from device pin configuration (direct mode). There are also various operational and test modes and a lock detect output.

Figure 3. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

Setting the Pre_en control bit "low" enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (F_{in}) by an integer or fractional number derived from the values in the "M", "A" counters and the DSM input word K. The accumulator size is 18 bits, so the fractional value is fixed from the ratio $K/2^{18}$. There is an additional bit in the DSM that acts as an extra bit (19^{th} bit). This bit is enabled by asserting the pin RAND_SEL to "high". Enabling this bit has the benefit of reducing the spurious levels at the cost of a small frequency offset will occur. This positive frequency offset is calculated with the following equation.

$$f_{offset} = (f_r / (R + 1)) / 2^{19} \quad (1)$$

All of the following equations do not take into account of this frequency offset. If this offset is important to a specific frequency plan, appropriate account needs to be taken.

In the normal mode, the output from the main counter chain (f_p) is related to the VCO frequency (F_{in}) by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A + K/2^{18}] \quad (2)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, F_{in} is related to the reference frequency (f_r) by the following equation:

$$F_{in} = [10 \times (M + 1) + A + K/2^{18}] \times (f_r / (R+1)) \quad (3)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that F_{in} must be greater than or equal to 90 x (f_r / (R+1)) to obtain contiguous channels. The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M counter with the minimum allowed value of "1" will result in a minimum divide ratio of "2" or "20", depending on the state of "prescaler enable".

Prescaler Bypass Mode (*)

Setting the frequency control register bit Pre_en "high" allows F_{in} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{in} to the reference frequency f_r:

$$F_{in} = (M + 1) \times (f_r / (R+1)) \quad (4)$$
$$\text{where } 1 \leq M \leq 511$$

(*) Only integer mode

In prescaler bypass mode, neither the A nor K counter is used. Therefore, only integer-N operation is possible.

Reference Counter

The reference counter chain divides the reference frequency f_r down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (5)$$
$$\text{where } 0 \leq R \leq 63$$

Note that programming R with "0" will pass the reference frequency (f_r) directly to the phase detector.

Register Programming

Serial Interface Mode

While the E_WR input is "low" and the S_WR input is "low", serial input data (Sdata input), B_0 to B_{20}, are clocked serially into the primary register on the rising edge of Sclk, MSB (B_0) first. The LSB is used as address bit. When "0", the contents from the primary register are transferred into the secondary register on the rising edge of either S_WR according to the timing diagrams shown in Figure 4. When "1", data is transferred to the auxiliary register according to the same timing diagram. The secondary register is used to program the various counters, while the auxiliary register is used to program the DSM.

Data are transferred to the counters as shown in Table 7 on page 9.

While the E_WR input is "high" and the S_WR input is "low", serial input data (Sdata input), B_0 to B_7, are clocked serially into the enhancement register on the rising edge of Sclk, MSB (B_0) first. The enhancement register is double buffered. Buffer capture of the serially entered data occurs on the falling edge of E_WR according to the timing diagram shown in Figure 4. After the falling edge of E_WR, the data control bits (shown in Table 8 on page 9) will have their function enabled by asserting the Enh input "low". **NOTE:** Bits B_2, B_4, B_5, and B_6 are only selectable one at a time.

Direct Interface Mode

Direct Interface Mode is selected by setting the DIRECT input (pin 42) "high".

Counter control bits are then set directly at the pins as shown in Tables 7 and 8.

Table 7. Seconadry Register Programming

Interface Mode	$\overline{Enh}$	R_5	R_4	M_8	M_7	$\overline{Pre\_en}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	Addr
Direct	1	R_5	R_4	M_8	M_7	Pre_en	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	0

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

MSB (first in) (last in) LSB

Table 8. Auxiliary Register Programming

Interface Mode	$\overline{Enh}$	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	Rsrv	Rsrv	Addr
Direct	1	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	X	X	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	1

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

MSB (first in) (last in) LSB

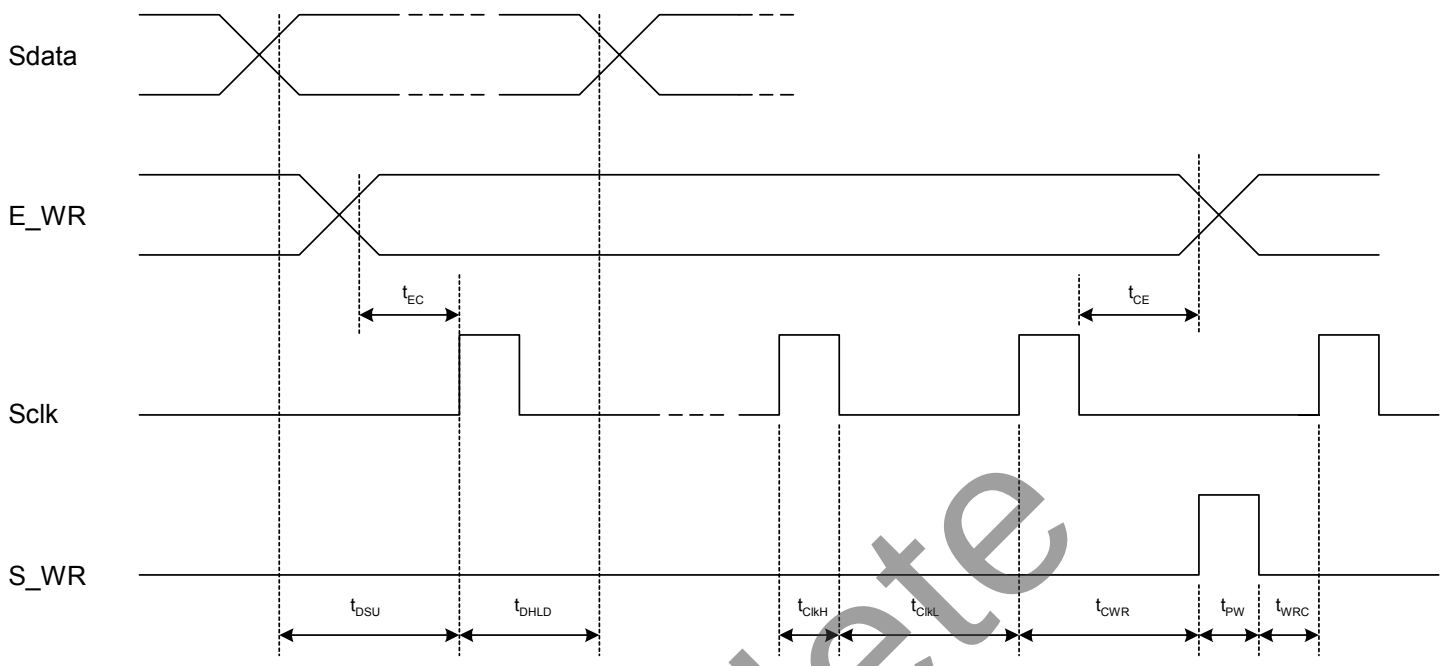
Table 9. Enhancement Register Programming

Interface Mode	$\overline{Enh}$	Reserved	Reserved	f_p output	Power Down	Counter load	MSEL output	f_c output	LD Disable
Serial*	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

*Serial data clocked serially on Sclk rising edge while E_WR "high" and captured in the double buffer on E_WR falling edge.

MSB (first in) (last in) LSB

Figure 4. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 10. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved **	Reserved.
Bit 1	Reserved **	Reserved.
Bit 2	f_p output	Drives the M counter output onto the Dout output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output.
Bit 6	f_c output	Drives the reference counter output onto the Dout output.
Bit 7	LD Disable	Disables the LD pin.

** Program to 0

Phase Detector and Charge Pump

The phase detector is rising edge triggered from the main (f_p) and reference counters (f_c). It has two outputs, PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_U pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

For the UP and DOWN mode, PD_U and PD_D drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to VDD / 2 π.

PD_U pulses cause an increase in VCO frequency and PD_D pulses cause a decrease in VCO frequency, when using a positive Kv VCO.

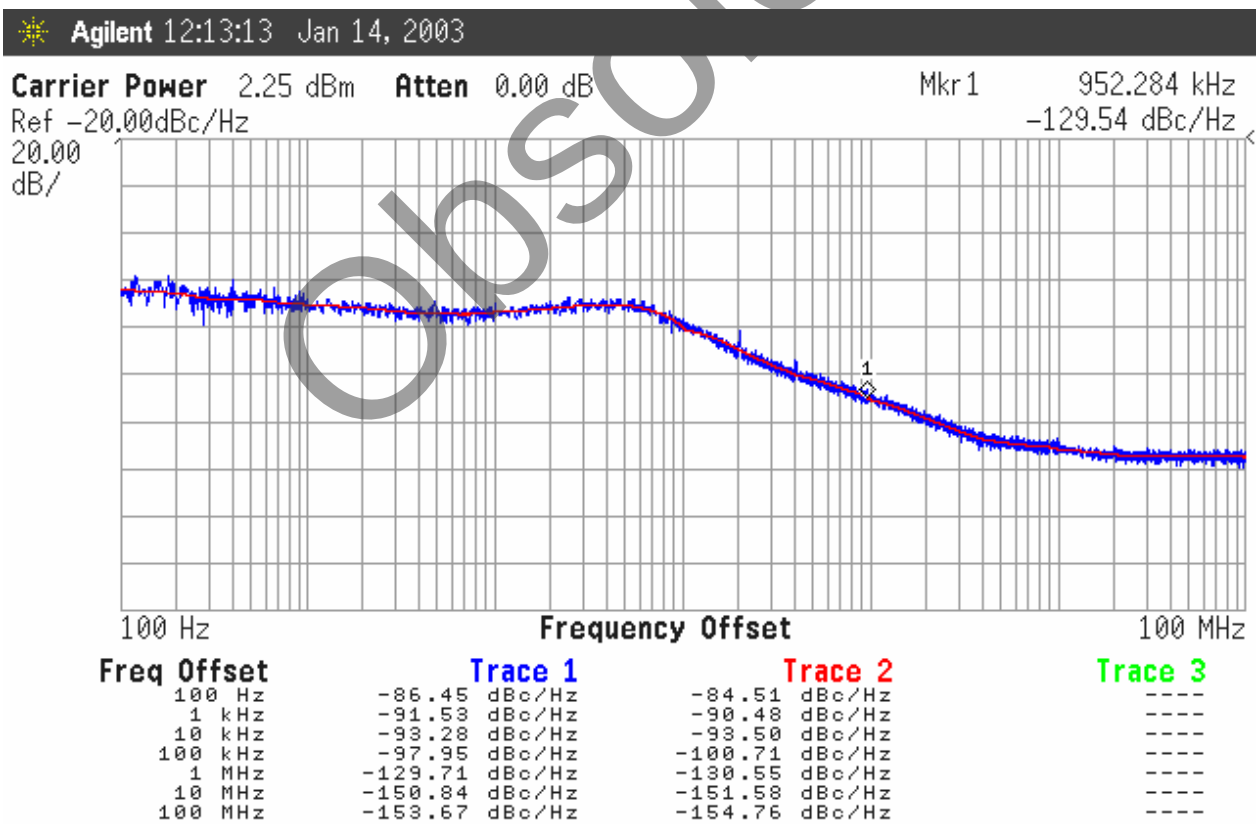
For the charge pump mode, the phase detector outputs are used internally to drive a tri-state charge pump. The PD_U, and PD_D output pins are disabled to logic Lo. The charge pump current is fixed at 2mA.

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of PD_U and PD_D waveforms, which is driven through a series 2 kohm resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. The LD output is an AND function of PD_U and PD_D.

Figure 5. Typical Phase Noise

Phase noise results for “Trace 2” is an averaging function of the measurement device.

Test Conditions: Fout = 1.92 GHz, Fcomparison = 10 MHz, V_{DD} = 3 V, Temp = 25 C.



Freq Offset	Trace 1	Trace 2	Trace 3
100 Hz	-86.45 dBc/Hz	-84.51 dBc/Hz	----
1 kHz	-91.53 dBc/Hz	-90.48 dBc/Hz	----
10 kHz	-93.28 dBc/Hz	-93.50 dBc/Hz	----
100 kHz	-97.95 dBc/Hz	-100.71 dBc/Hz	----
1 MHz	-129.71 dBc/Hz	-130.55 dBc/Hz	----
10 MHz	-150.84 dBc/Hz	-151.58 dBc/Hz	----
100 MHz	-153.67 dBc/Hz	-154.76 dBc/Hz	----

Figure 6. Typical Spurious Plot

Test Conditions: Frequency step = 200 KHz, Loop bandwidth = 50 KHz, Fout = 1.92 GHz, Fcomparison = 10 MHz, V_{DD} = 3 V, Temp = 25 C.

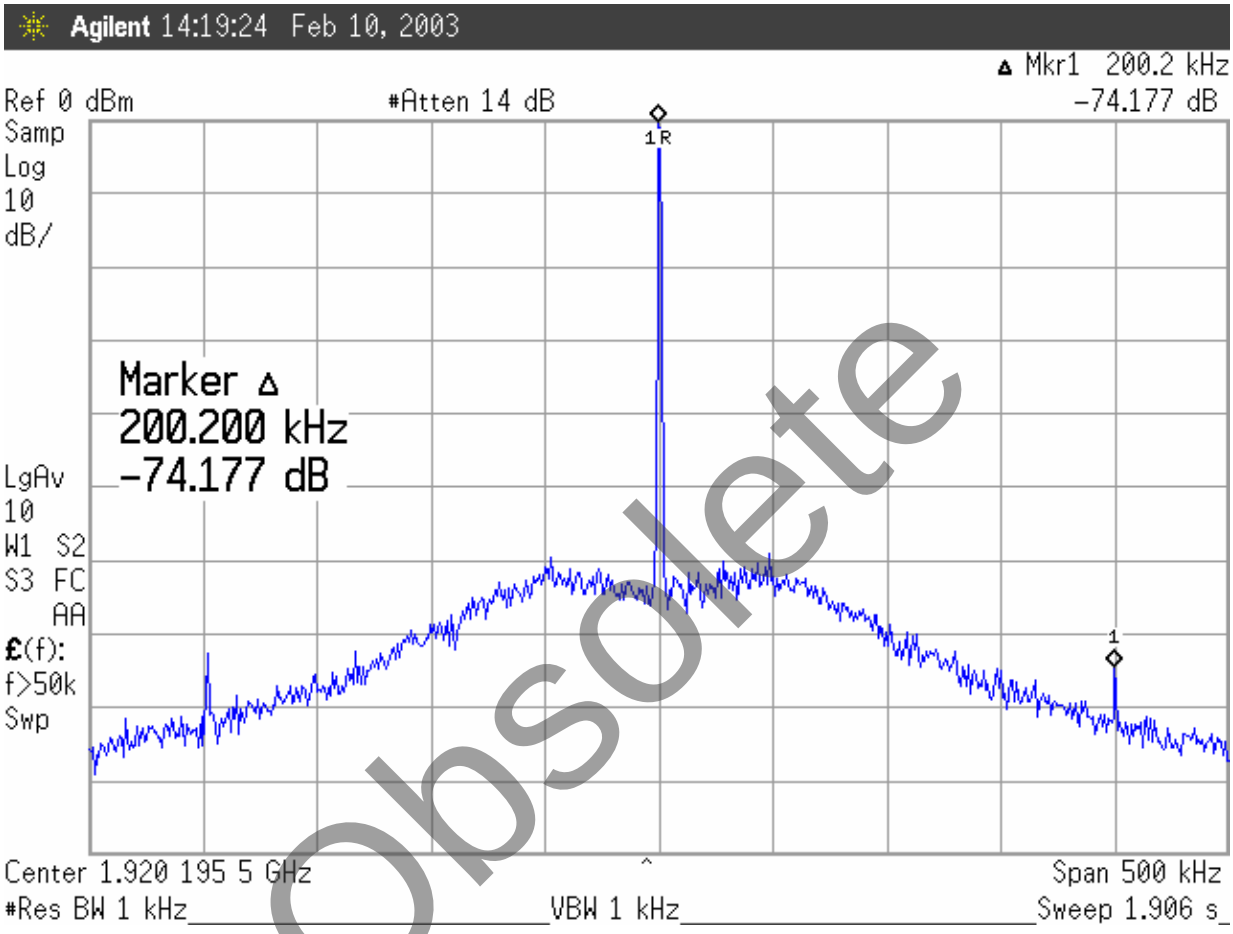


Figure 7. Package Drawing

Package dimensions: 68-lead CQFJ w/o lid

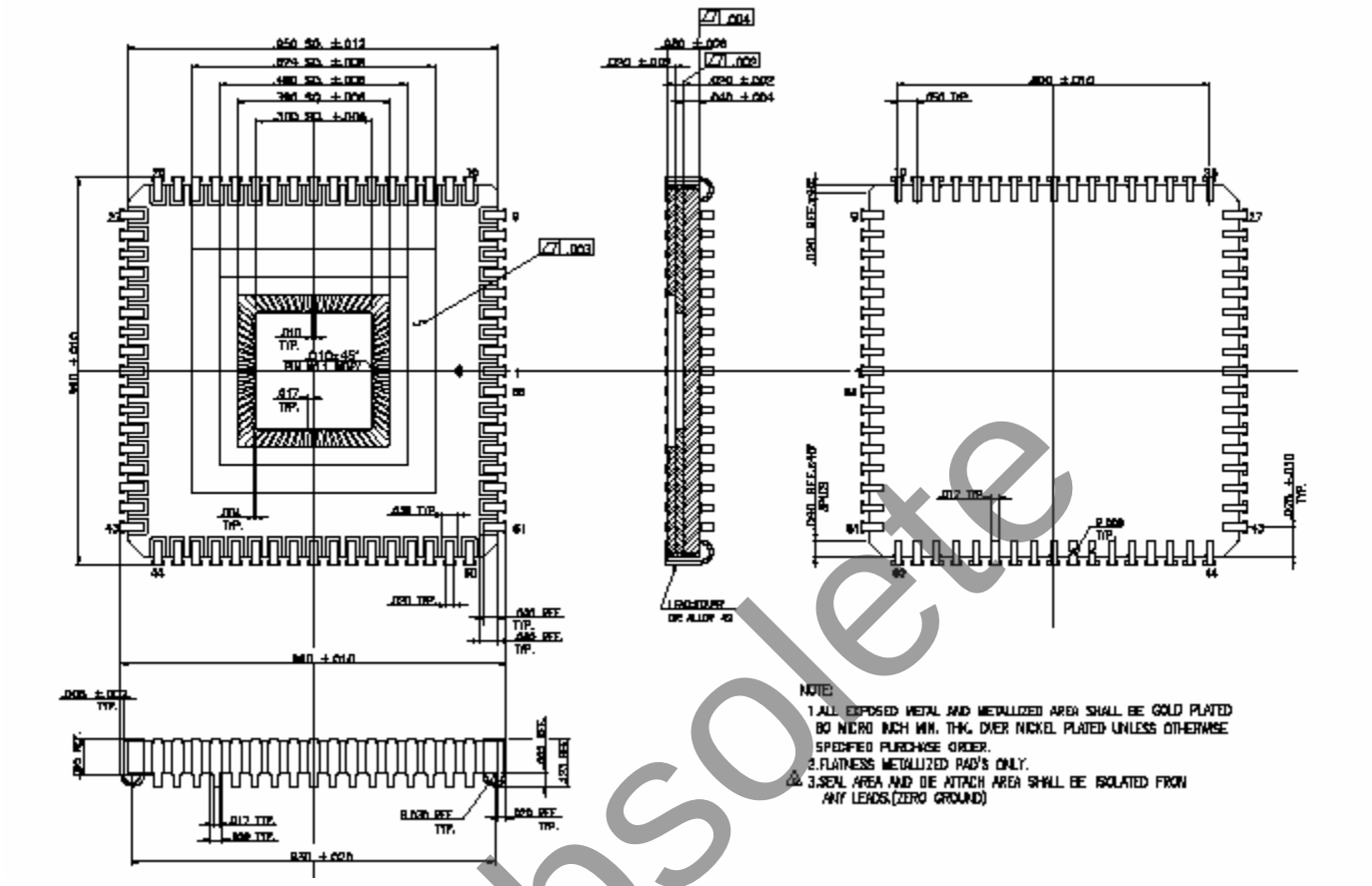


Table 11. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
83363-01	PE83363 ES	Engineering Samples	68-pin CQFJ	Tray
83363-11	PE83363	Production Units	68-pin CQFJ	21 units / Tray
83363-00	PE83363 EK	Evaluation Kit		1 / Box

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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