Product Specification

PE42551

SPDT UltraCMOS® RF Switch
9 kHz - 6000 MHz

Product Description

The PE42551 RF Switch is designed to support the requirements of the test equipment and ATE market. This broadband general purpose switch maintains excellent RF performance and linearity from 9 kHz through 6000 MHz. The PE42551 integrates on-board CMOS control logic driven by a single-pin, low voltage CMOS control input. It also has a logic select pin which enables changing the logic definition of the control pin. Additional features include a novel user defined logic table, enabled by the on-board CMOS circuitry. The PE42551 also exhibits outstanding isolation that approaches 21 dB at 6000 MHz and is offered in a small 4x4x0.85 mm QFN package.

The PE42551 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™-Technology –Enhanced
  - Eliminates Gate and Phase Lag
  - No insertion loss nor phase drift
  - Fast settling time
- High linearity 50 dBm IIP3
- Low insertion loss: 0.65 dB at 3000 MHz, 0.90 dB at 6000 MHz
- High isolation of 29 dB at 3000 MHz, 21 dB at 6000 MHz
- High power 1 dB compression point of +34 dBm
- ESD: 500 V HBM
- Single-pin 2.75V CMOS logic control
- Logic select pin to change definition of logic control
- Reflective switch design
- 20-lead 4x4x0.85 mm QFN package

Figure 1. Functional Diagram
Peregrine Specification 71-0065

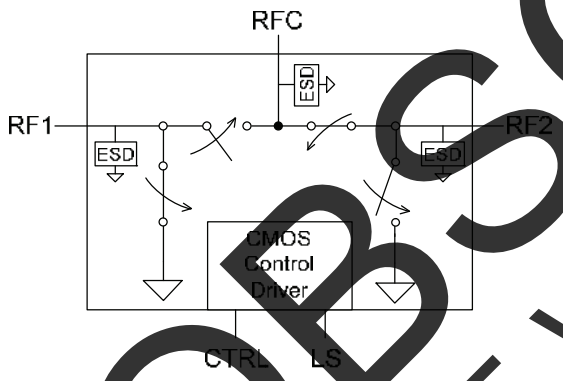


Figure 2. Package Type
20-lead 4x4x0.85 mm QFN

Table 1. Electrical Specifications @ +25°C, V_{DD} = 2.75V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency		9 kHz		6000	MHz
Insertion Loss	9 kHz 3000 MHz 6000 MHz		0.55 0.65 0.90	0.65 0.75	dB dB dB
Isolation – RF1 to RF2	3000 MHz 6000 MHz	28	29 21		dB dB
Return Loss RF1, RF2 and RFC	3000 MHz 6000 MHz	14	18 14		dB dB
Switching Time	50% CTRL to 0.1 dB final value		7		µs
Input 1 dB Compression	6000 MHz	32	34		dBm
Input IP3	6000 MHz		+50		dBm

Note: Device linearity will begin to degrade below 10 MHz.

Figure 3. Pin Configuration (Top View)

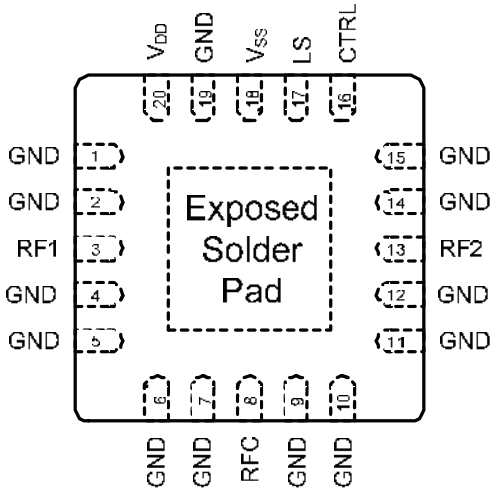


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
13	RF2	RF2 port.[1]
1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 19	GND	Ground Connection. Traces should be physically short and connected to the ground plane. This pin is connected to the exposed solder pad that also must be soldered to the ground plane for best performance.
3	RF1	RF1 port.[1]
16	CTRL	CMOS level (See *Table 5*)
8	RFC	Common RF port for switch[1]
17	LS	Logic Select - Used to determine the definition for the CTRL pin (see *Table 5*)
18	V_{SS}	Negative power supply. Apply nominal -2.75V supply[2]
20	V_{DD}	Nominal 2.75V supply connection
Paddle	GND	Exposed Ground Paddle

Notes: 1. All RF pins must be held at 0 VDC or the DC must be blocked with an external series capacitor.
2. Use V_{SS} (pin 18, V_{SS} = -V_{DD}) to bypass and disable internal negative voltage generator. Connect V_{SS} (pin 18) to GND (V_{SS} = 0V) to enable internal negative voltage generator.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for CTRL and LS inputs	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		4.0	V
V_{LS}	Voltage on LS input		4.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input Power 50Ω: 9 kHz ≤ 4 MHz 4 MHz ≤ 6 GHz		*Fig. 4* 31	dBm dBm
V_{ESD}	ESD voltage HBM[1]		500	V

Note: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42551 in the 20-lead 4x4x0.85 mm QFN package is MSL1.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Table 4. Operating Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Positive Power Supply Voltage	2.5	2.75	3.0	V
V_{DD} Negative Power Supply Voltage	-2.5	-2.75	-3.0	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		20		µA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V
RF Power In 50Ω: 9 kHz ≤ 4 MHz 4 MHz ≤ 6 GHz			*Fig. 4* 31	dBm dBm

Spurious Performance

The typical spurious performance of the PE42551 is -116 dBm when V_{SS} = 0V. If further improvement is desired, the internal negative voltage generator can be disabled by externally applying a negative voltage to the V_{SS} pin such that V_{SS} = -V_{DD}.

Figure 4. Power Handling vs Frequency and Vdd

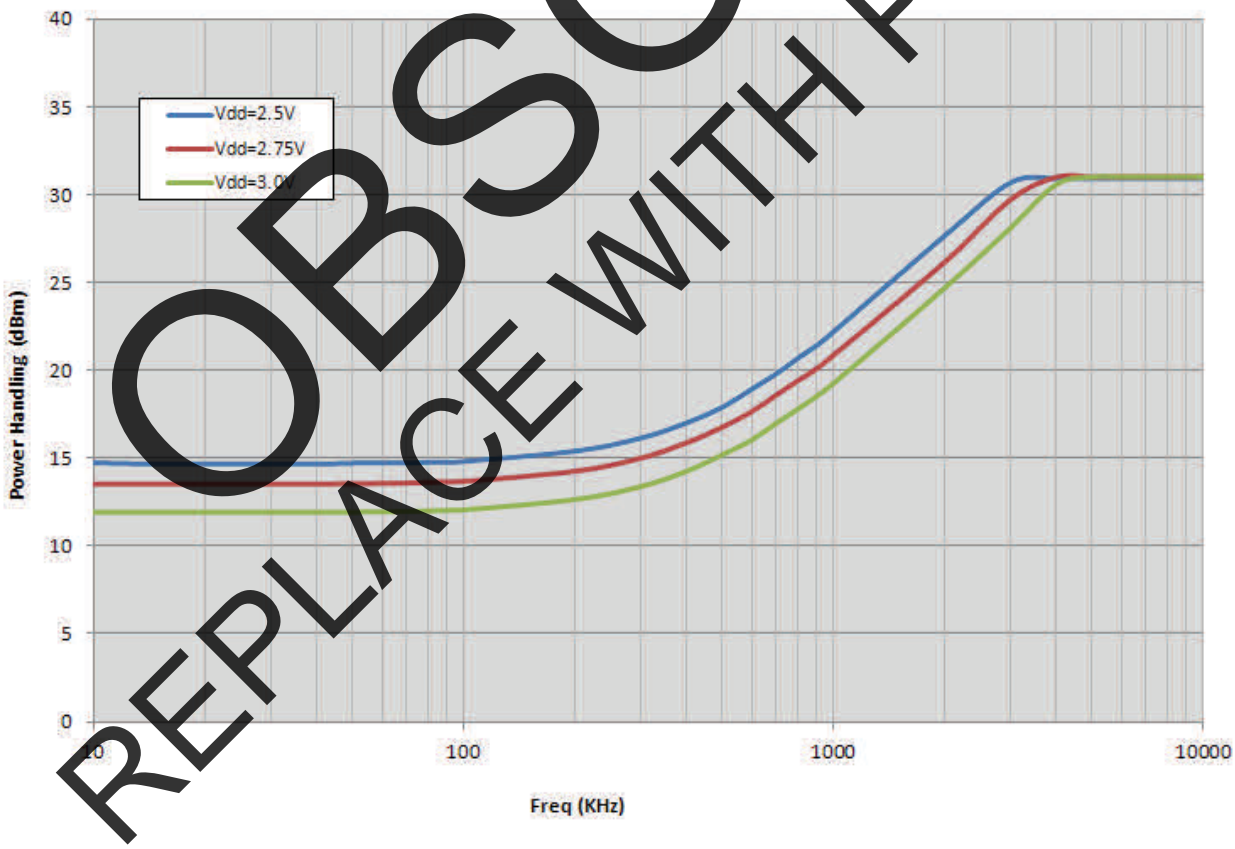


Table 5. Control Logic Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Logic Select (LS)

The Logic Select feature is used to determine the definition for the CTRL pin.

Switching Frequency

The PE42551 has a maximum 25 kHz switching rate when the internal negative voltage generator is used. In the event a customer applies V_{SS} external (-V_{DD}) to Pin 18, the Switching Rate is limited to the reciprocal of the Switching Time in *Table 1*.

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE42551 SPDT switch. The RF common port is connected through a 50 Ω transmission line to J2. Port 1 and Port 2 are connected through 50 Ω transmission lines to J1 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.032". The transmission lines were designed using a coplanar waveguide with ground plane (28 mil core, 47.6 mil width, 30 mil gap).

Good RF layout and prudent use of vias is critical for obtaining the specified isolation performance for the device shown in this datasheet.

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to V_{DD} for logic high. When the jumper is in place, 3 µA of current will flow through the 1MΩ pull up resistor. This extra current should not be attributed to the requirements of the device.

Figure 5. Evaluation Board Layouts

Peregrine Specification 101-0151

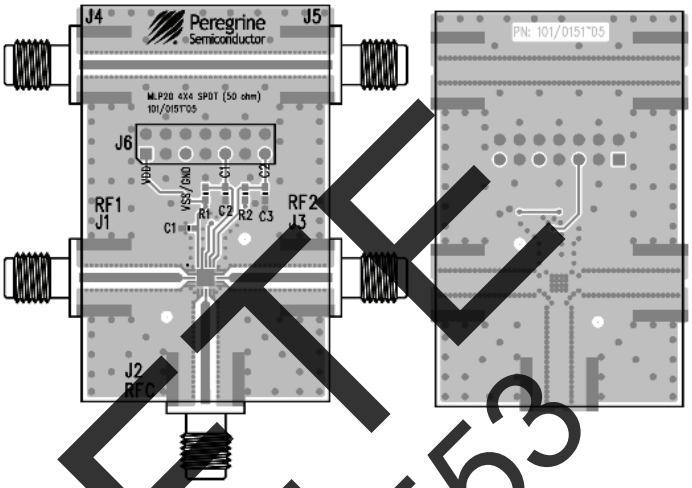
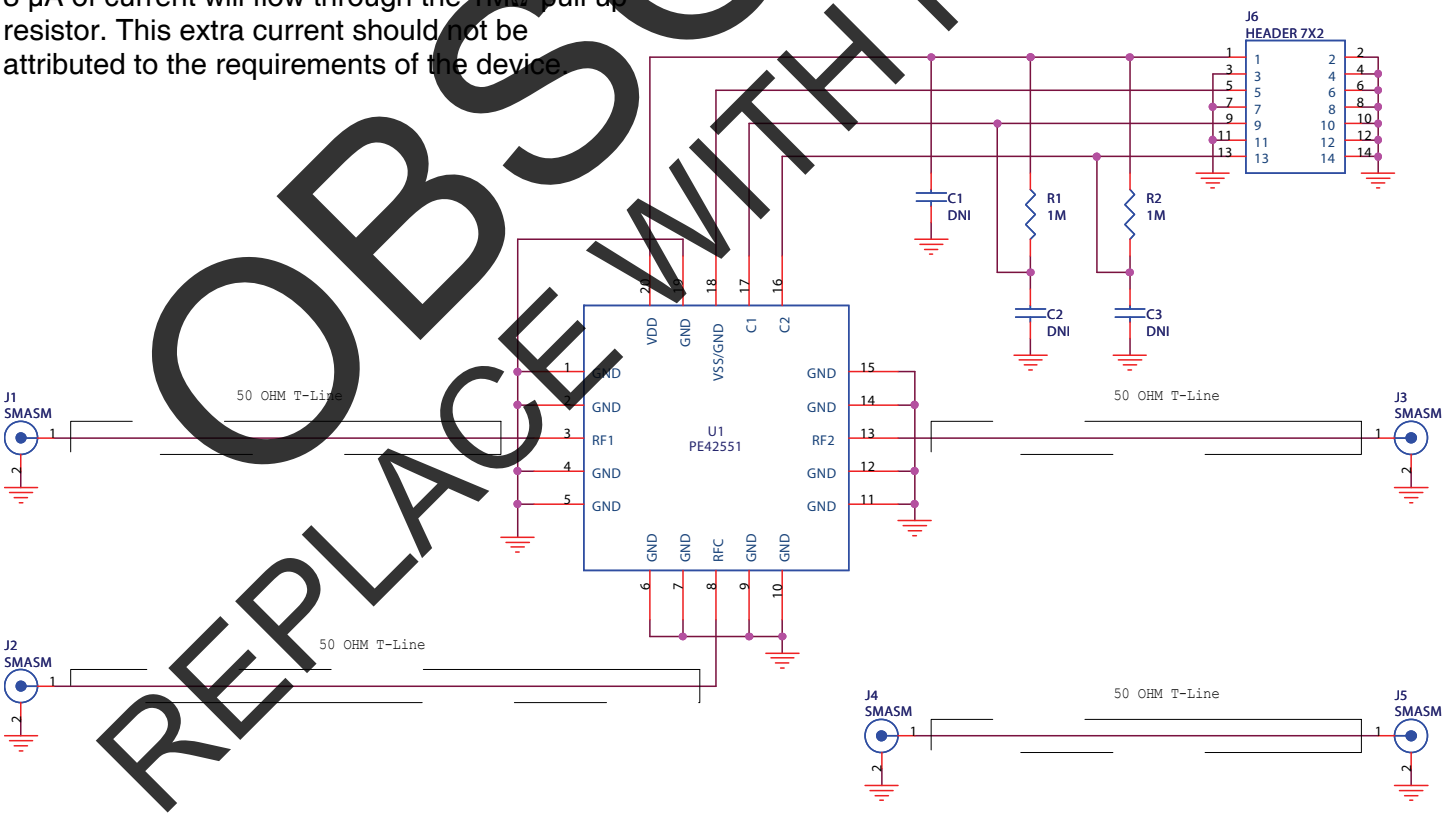


Figure 6. Evaluation Board Schematic

Peregrine Specification 102-0198



Typical Performance Data

Figure 7. Insertion Loss: RFC-RF1@ 25°C

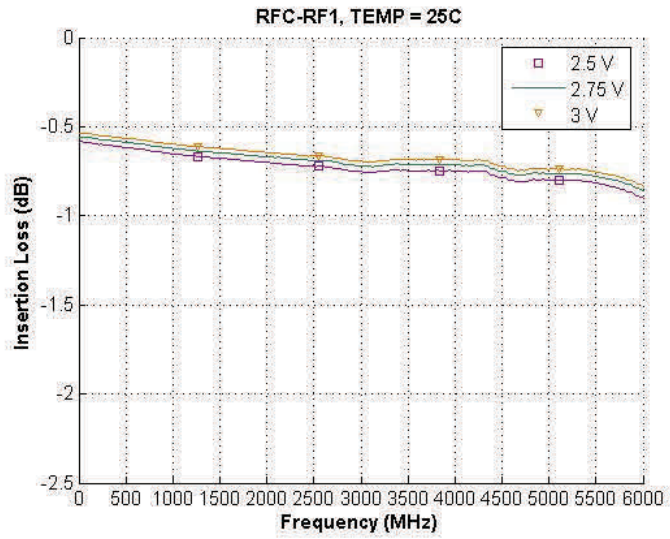


Figure 8. Insertion Loss: RFC-RF1@ 2.75V

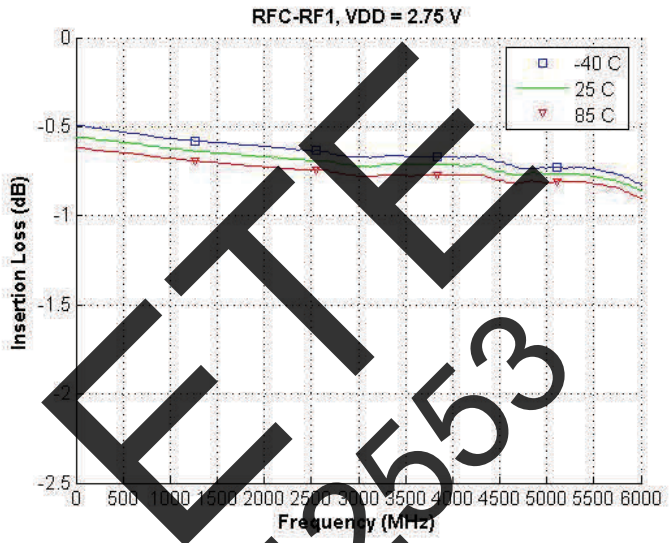


Figure 9. Insertion Loss: RFC-RF2 @ 25°C

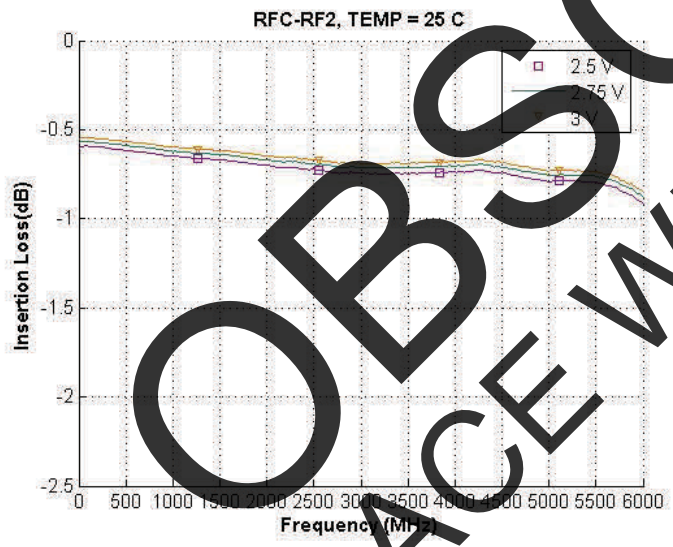
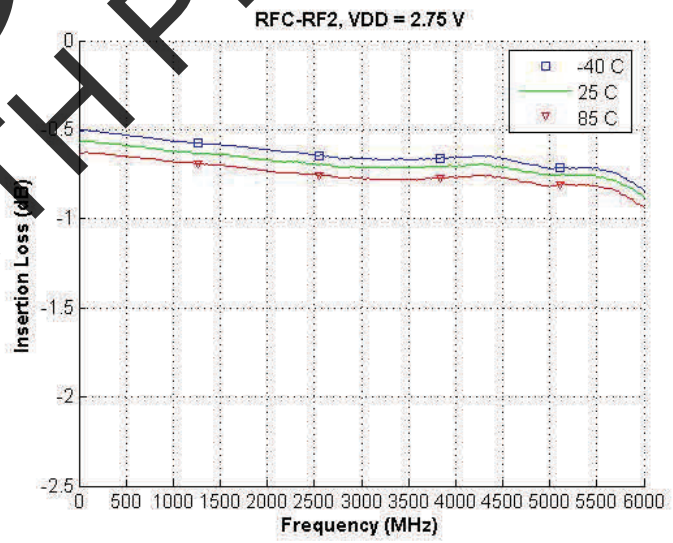


Figure 10. Insertion Loss: RFC-RF2 @ 2.75V



Typical Performance Data

Figure 11. Isolation: RFC-RF1@ 25°C

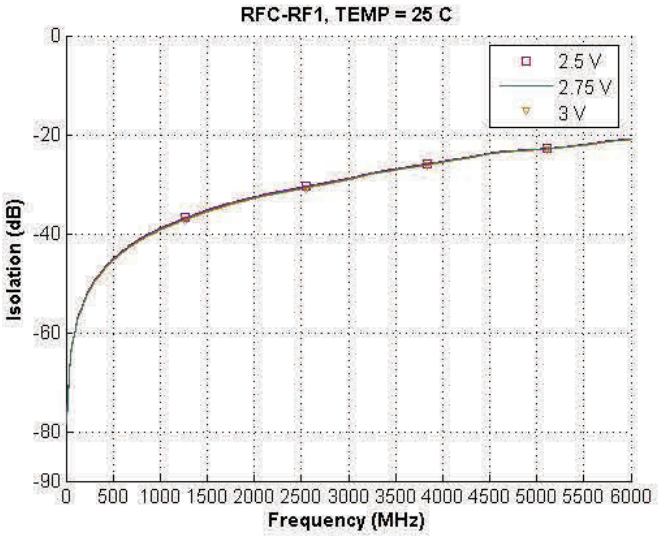


Figure 12. Isolation: RFC-RF1@ 2.75V

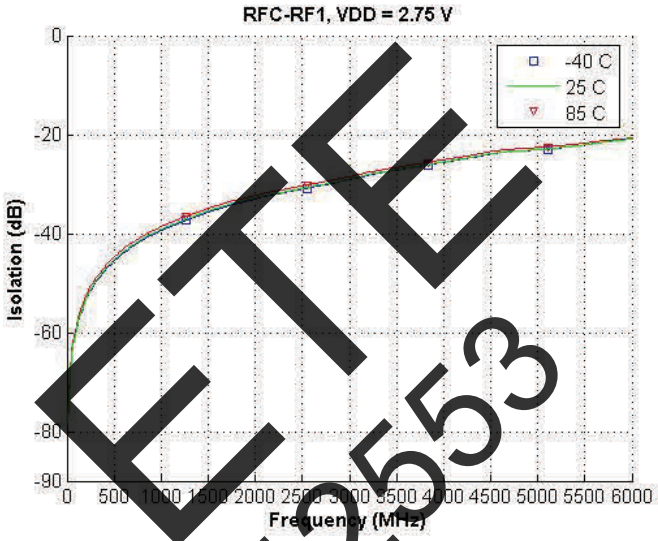


Figure 13. Isolation: RFC-RF2 @ 25°C

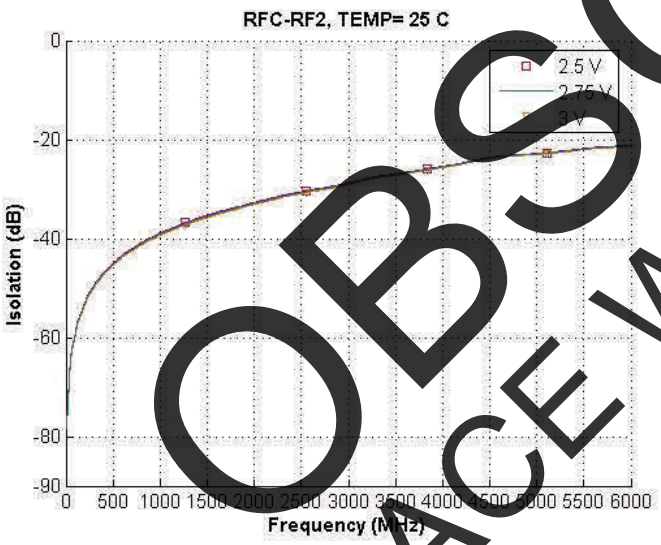
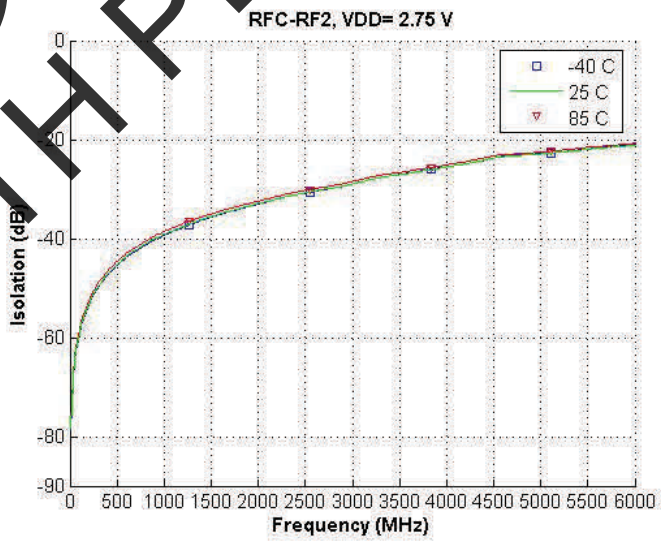


Figure 14. Isolation: RFC-RF2 @ 2.75V



Typical Performance Data

Figure 15. Return Loss: RF1 @ 25°C (RFC-RF1 Active Path)

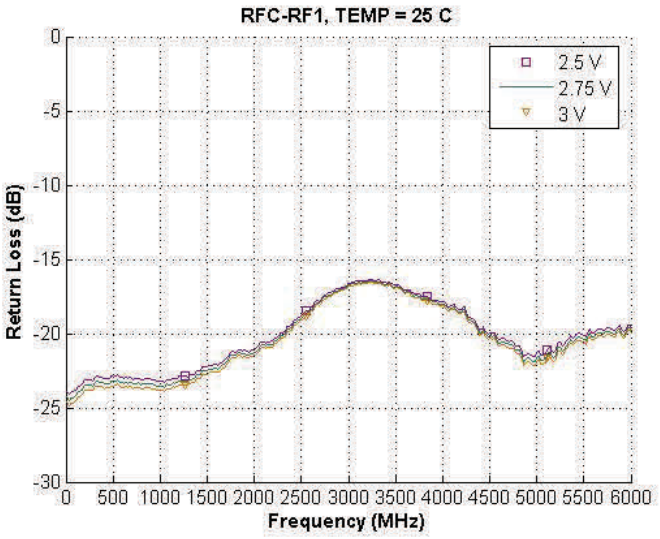


Figure 16. Return Loss: RF1 @ 2.75V (RFC-RF1 Active Path)

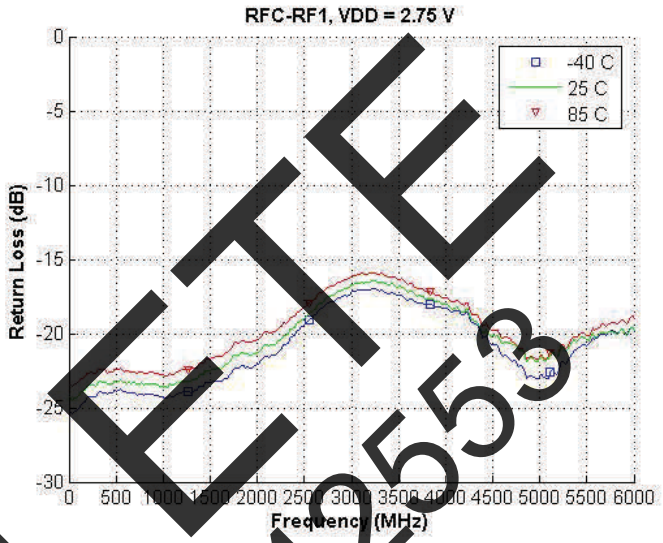


Figure 17. Return Loss: RF2 @ 25°C (RFC-RF2 Active Path)

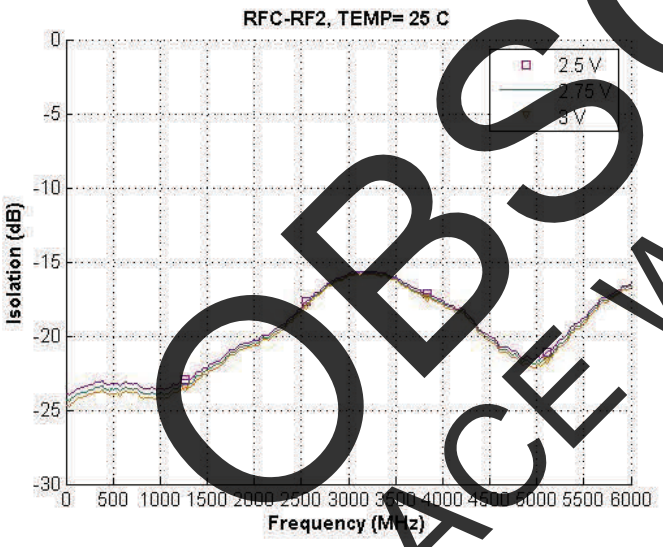


Figure 18. Return Loss: RF2 @ 2.75V (RFC-RF2 Active Path)

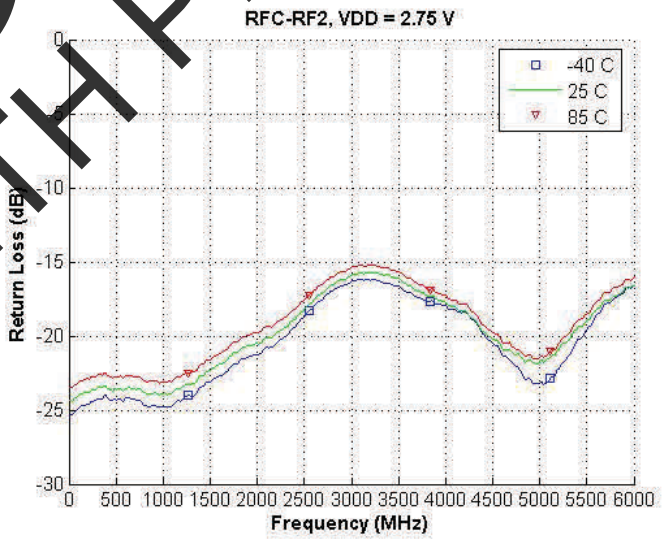


Figure 19. Package Drawing

20-lead 4x4x0.85 mm QFN
Peregrine Specification 19-0106

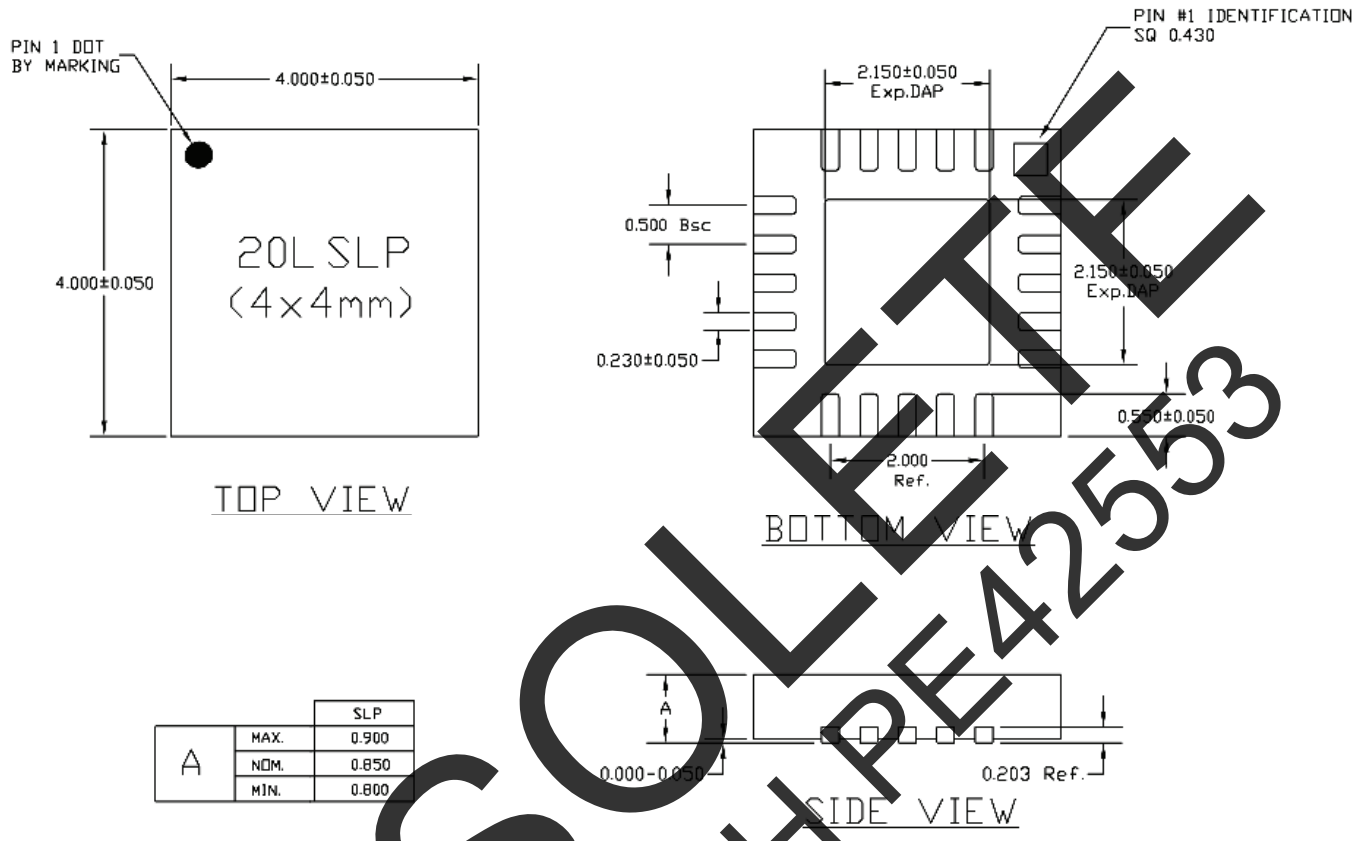
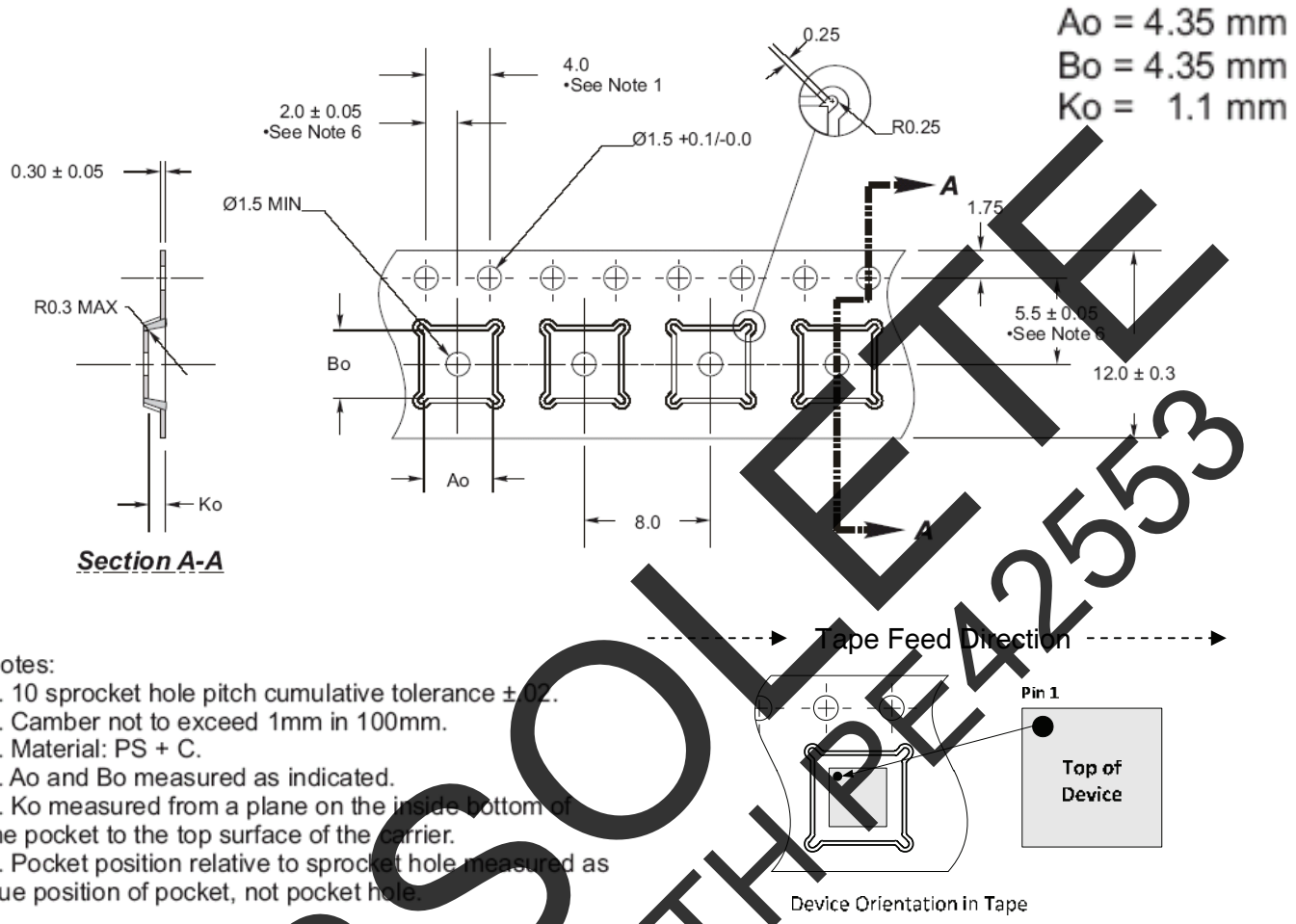


Figure 20. Marking Specifications

Peregrine Specification 17-0009

YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Figure 21. Tape and Reel Drawing



Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
42551-00	PE42551-EK	PE42551-20QFN 4x4 mm-EK	Evaluation Kit	1/Box
42551-51	42551	PE42551G-20QFN 4x4 mm	Green 20-lead 4x4 mm QFN	Cut Tape
42551-52	42551	PE42551G-20QFN 4x4 mm-3000C	Green 20-lead 4x4 mm QFN	3000 units/T&R

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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