Peregrine Semiconductor

Product Specification

PE4283

SPDT High Power UltraCMOS™
DC – 4.0 GHz RF Switch

Product Description

The PE4283 RF Switch is designed to cover a broad range of applications from DC through 4000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. The PE4283 operates using a +3 volt power supply.

The PE4283 SPDT High Power RF Switch is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Single-pin or complementary CMOS logic control inputs
- 1.5 kV ESD tolerance
- Low insertion loss: 0.65 dB at 1000 MHz, 0.70 dB at 2500 MHz
- RFC-RF1/RF2 isolation of 33.5 dB at 1000 MHz, 21.5 dB at 2500 MHz
- RF1-RF2 isolation of 37.5 dB at 1000 MHz, 22 dB at 2500 MHz
- Typical input 1 dB compression point of +32 dBm
- Ultra-small SC-70 package

Figure 1. Functional Diagram

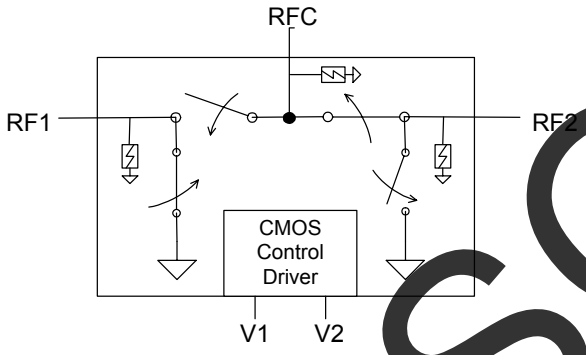


Figure 2. Package Type SC-70

6-lead SC-70

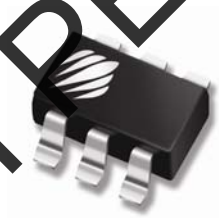


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V ($Z_S = Z_L = 50\ \Omega$)

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency[1]	DC - 4000	DC		4000	MHz
Insertion Loss	1000 MHz 2500 MHz		0.65 0.70	0.75 0.80	dB dB
Isolation: RFC - RF1/RF2	1000 MHz 2500 MHz	31.5 19.5	33.5 21.5		dB dB
Isolation: RF1 - RF2	1000 MHz 2500 MHz	35.5 20	37.5 22		dB dB
Return Loss	1000 MHz 2500 MHz		19 16		dB dB
'ON' Switching Time	50% CTRL to 0.1 dB of final value, 1 GHz		0.725	1.5	µs
'OFF' Switching Time	50% CTRL to 25 dB isolation, 1 GHz		0.625	1.3	µs
Input 1 dB Compression	1000 MHz	30	+32		dBm
Input IP3	1000 MHz, 20 dBm input power		+53		dBm

Note: 1. Device linearity will begin to degrade below 10 MHz.

Figure 3. Pin Configuration (Top View)

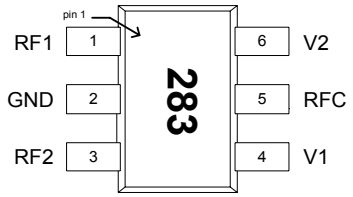


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1	RF Port1[2]
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2	RF Port2[2]
4	V1	Switch control input, CMOS logic level.
5	RFC	RF Common[2]
6	V2	This pin supports two interface options: *Single-pin control mode*. A nominal 3-volt supply connection is required. *Complementary-pin control mode*. A complementary CMOS control signal to V1 is supplied to this pin.

Note: 2. All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		+34	dBm
V_{ESD}	ESD Voltage (HBM, ML_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.0	3.0	3.3	V
I_{DD} Power Supply Current (V1 = 3V, V2 = 3V)		8	50	µA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

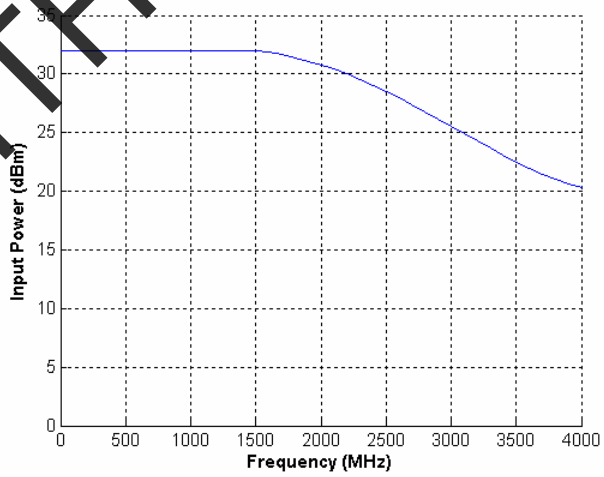
Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Figure 4. Maximum Operating Input Power[3]



Note: 3. Operating within DC limits (Table 4).

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V2) = V_{DD} Pin 4 (V1) = High	RFC to RF1
Pin 6 (V2) = V_{DD} Pin 4 (V1) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V2) = Low Pin 4 (V1) = High	RFC to RF1
Pin 6 (V2) = High Pin 4 (V1) = Low	RFC to RF2

Control Logic Input

The PE4283 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection (pin 6). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS µProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins V1 and V2 (pins 4 & 6), that can be directly driven by +3-volt CMOS logic or a suitable µProcessor I/O port. This enables the PE4283 to operate in positive control voltage mode within the PE4283 operating limits.

Evaluation Kit

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE4283. The RF common (RFC) port is connected through a 50 Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50 Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50 Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V2 input. J7-1 is connected to the device V1 input. Series resistors (R1 and R2) are provided to reduce the package resonance between RF and DC lines.

Figure 5. Evaluation Board Layouts
Peregrine Specification 101/0162

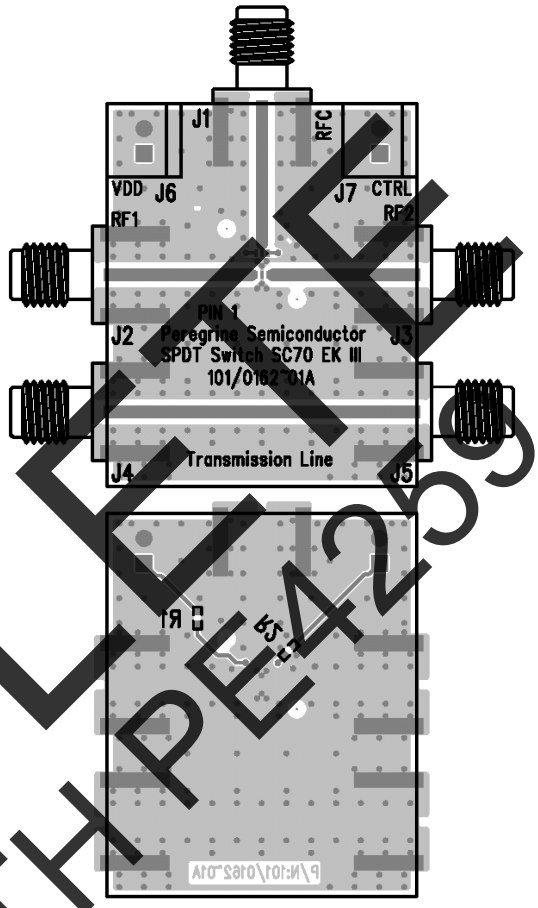
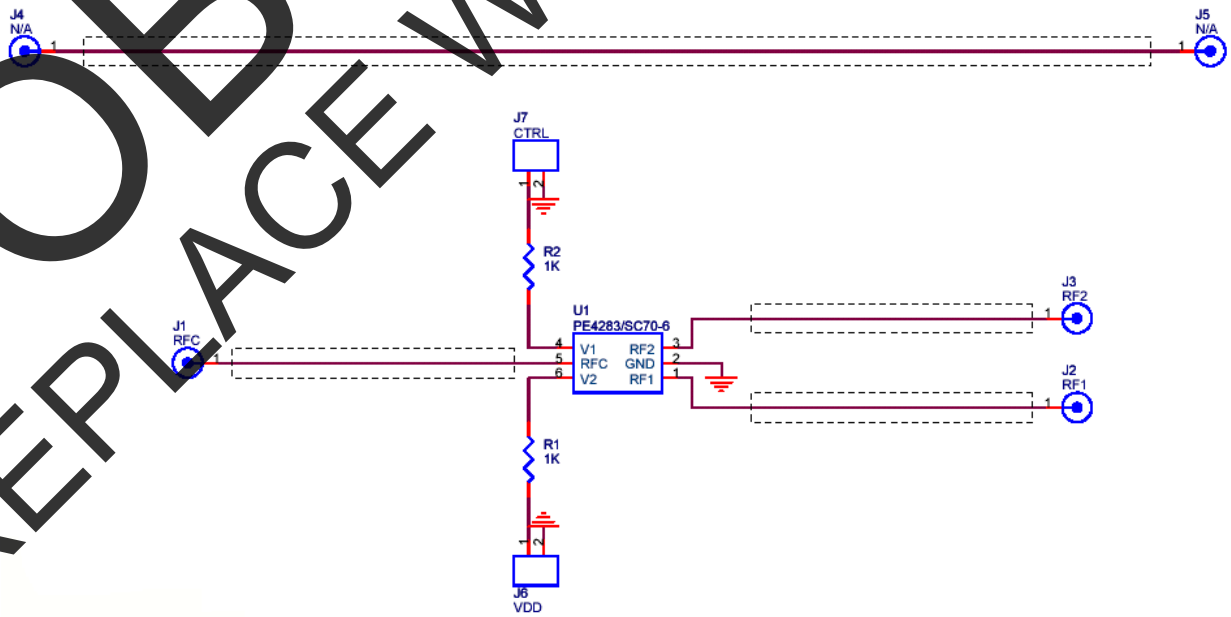


Figure 6. Evaluation Board Schematic
Peregrine Specification 102/0322



Typical Performance Data

Figure 7. Insertion Loss @ 25 °C

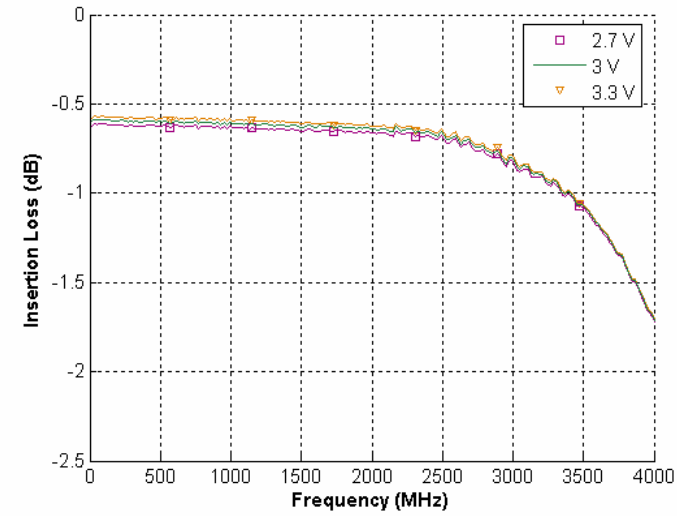


Figure 8. Insertion Loss @ 3 V

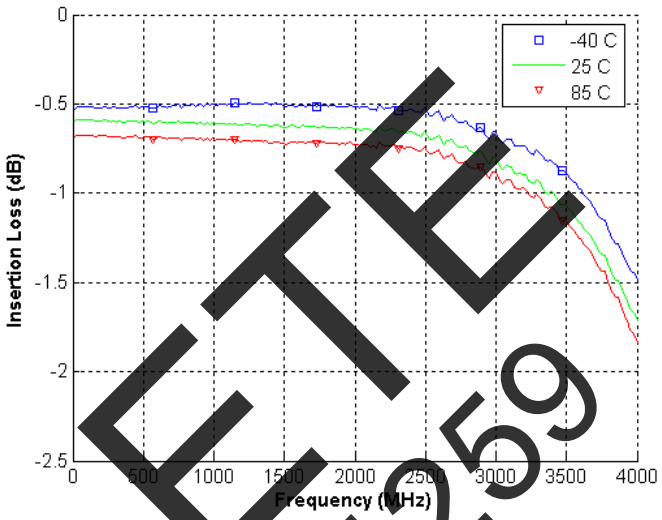


Figure 9. Isolation: RF1-RF2 @ 25 °C

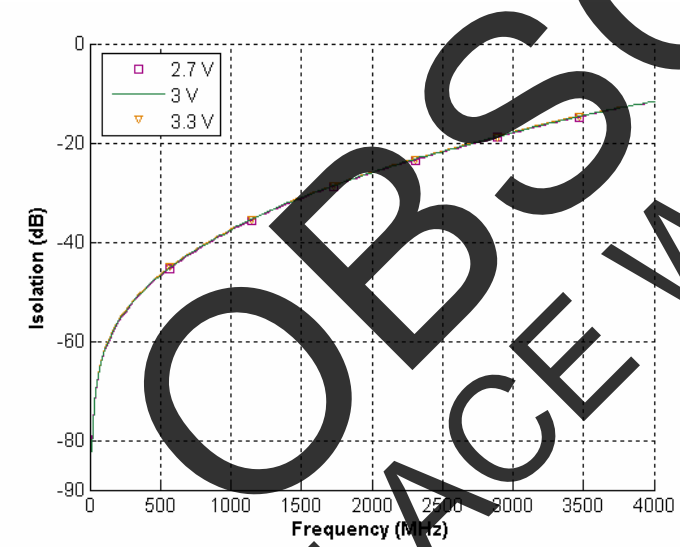
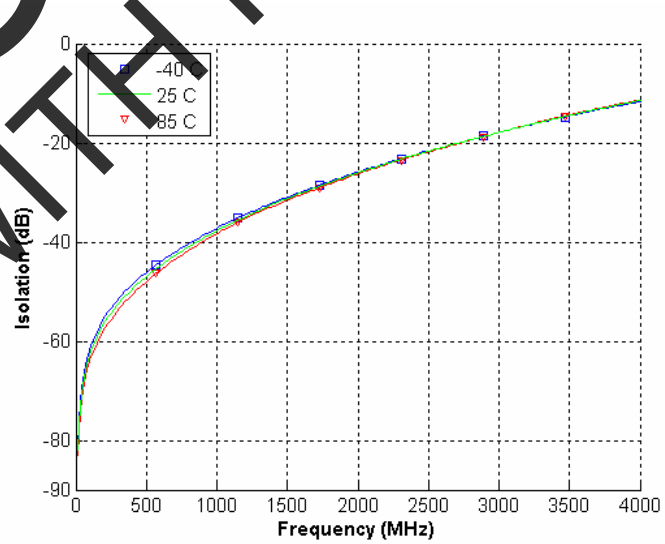


Figure 10. Isolation: RF1-RF2 @ 3 V



Typical Performance Data

Figure 11. Isolation: RFC-RF1/RF2 @ 25 °C

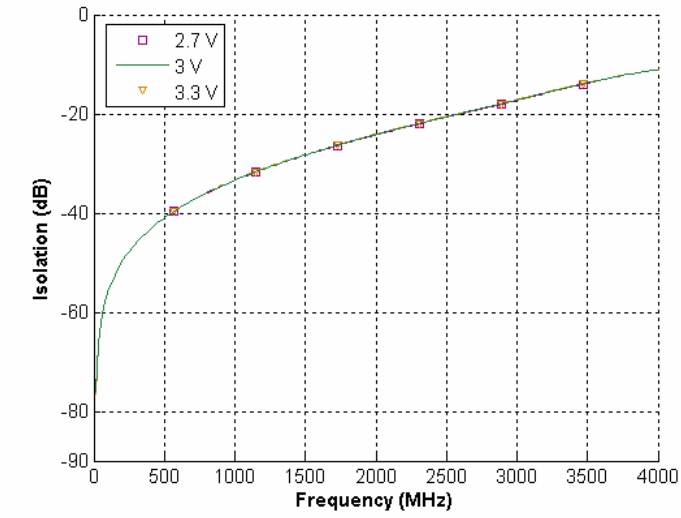


Figure 12. Isolation: RFC-RF1/RF2 @ 3 V

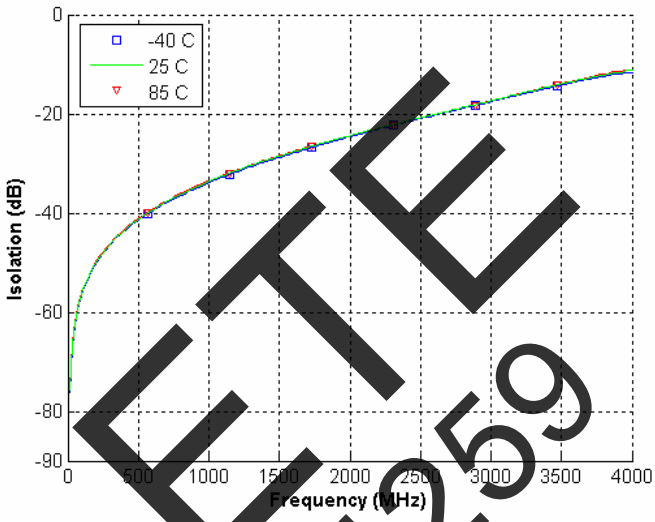


Figure 13. Return Loss: RF1-RF2 @ 25 °C

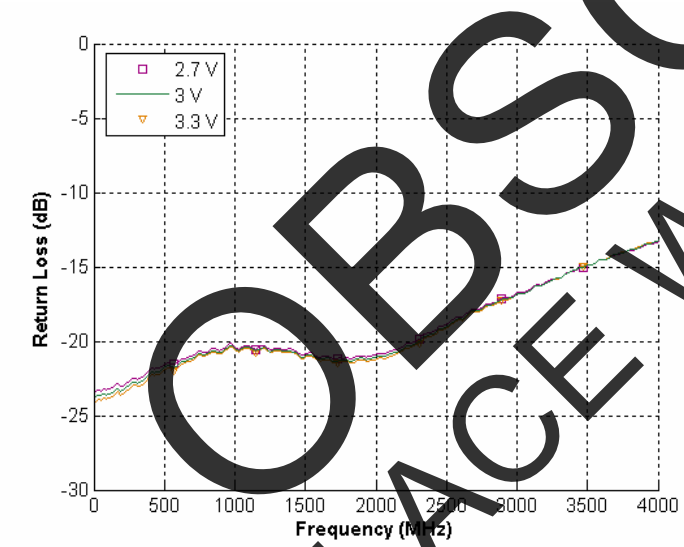
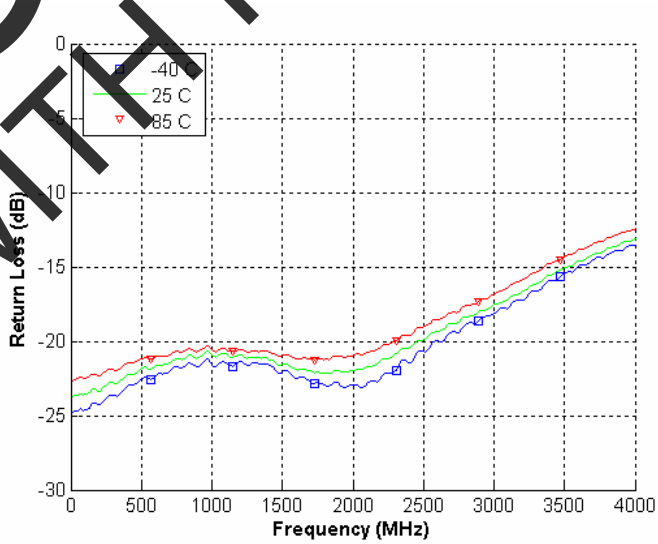


Figure 14. Return Loss: RF1-RF2 @ 3 V



Typical Performance Data

Figure 15. Return Loss: RFC-RF1 @ 25 °C

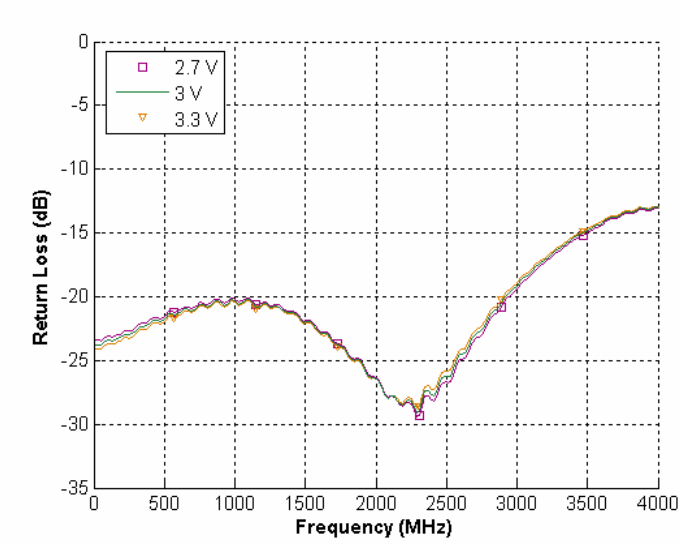


Figure 16. Return Loss RFC-RF1 @ 3 V

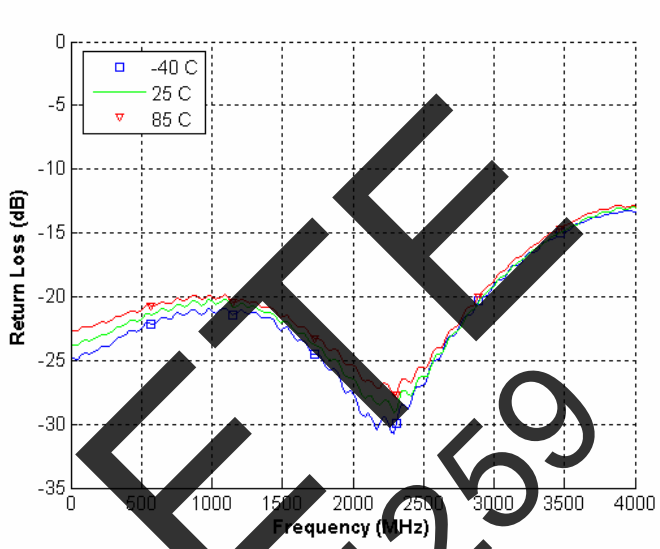


Figure 17. Return Loss: RFC-RF2 @ 25 °C

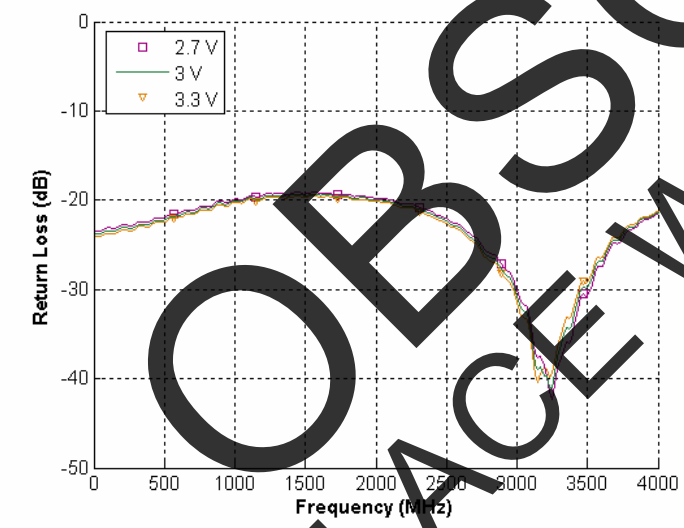
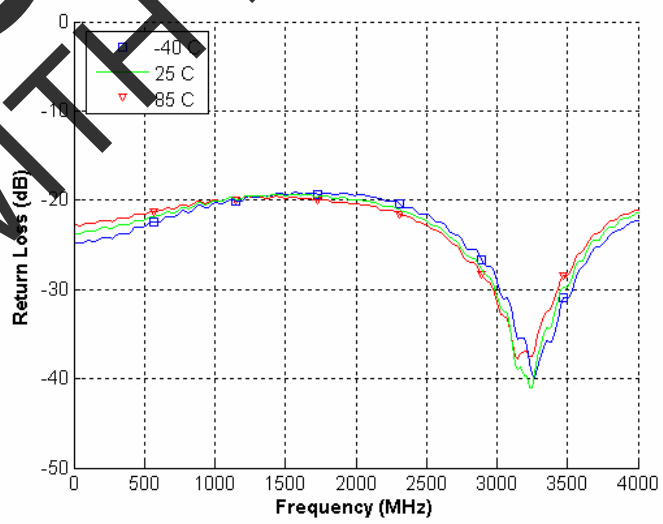


Figure 18. Return Loss: RFC-RF2 @ 3 V



Typical Performance Data

Figure 19. Input 1 dB Compression and IIP3

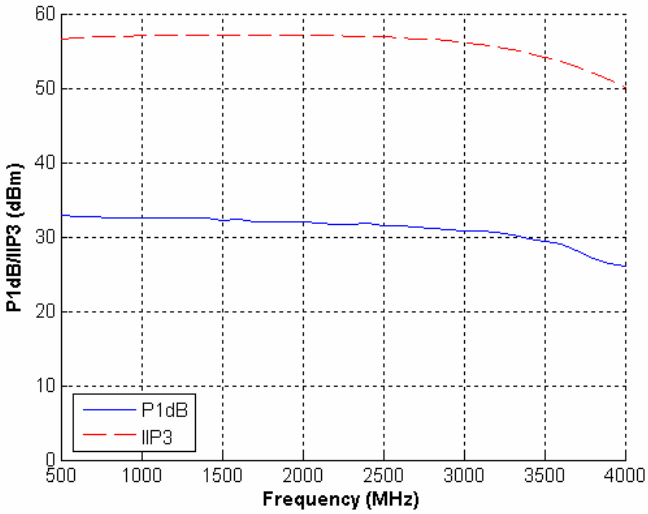


Figure 20. Package Drawing

6-lead SC-70

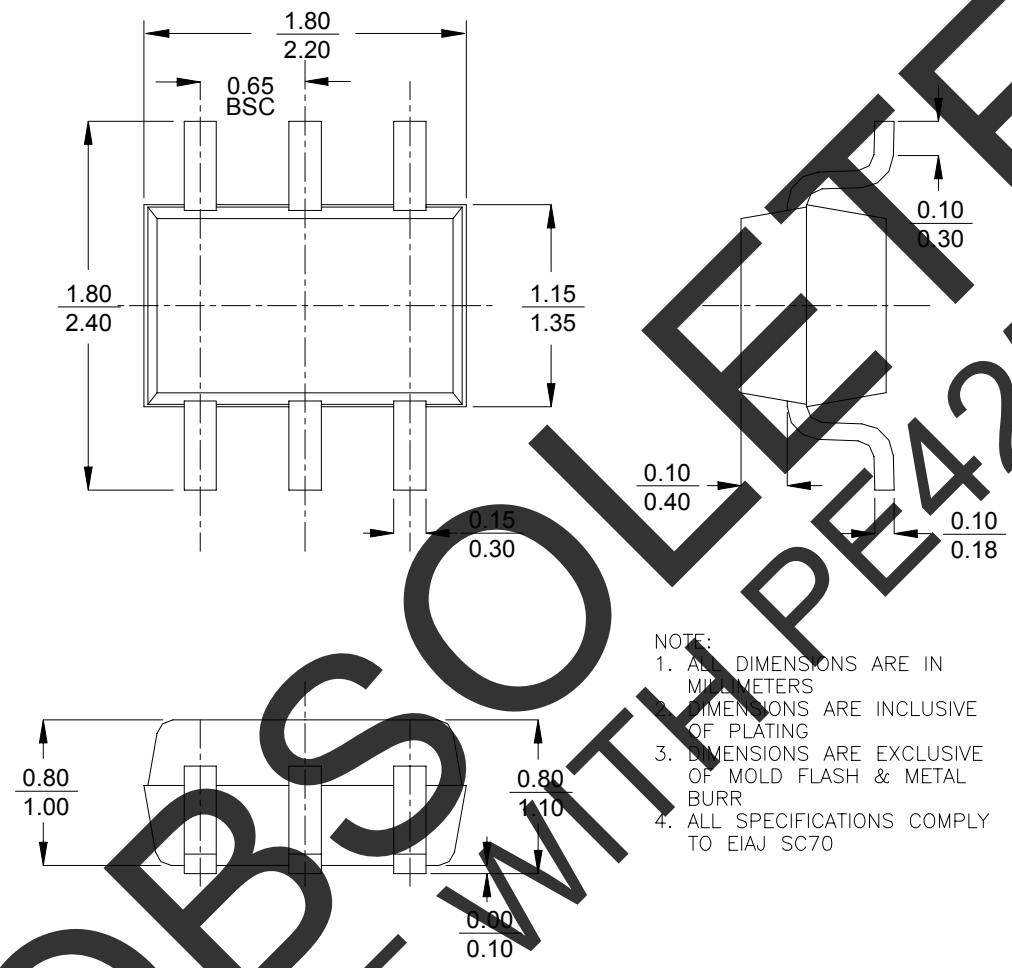
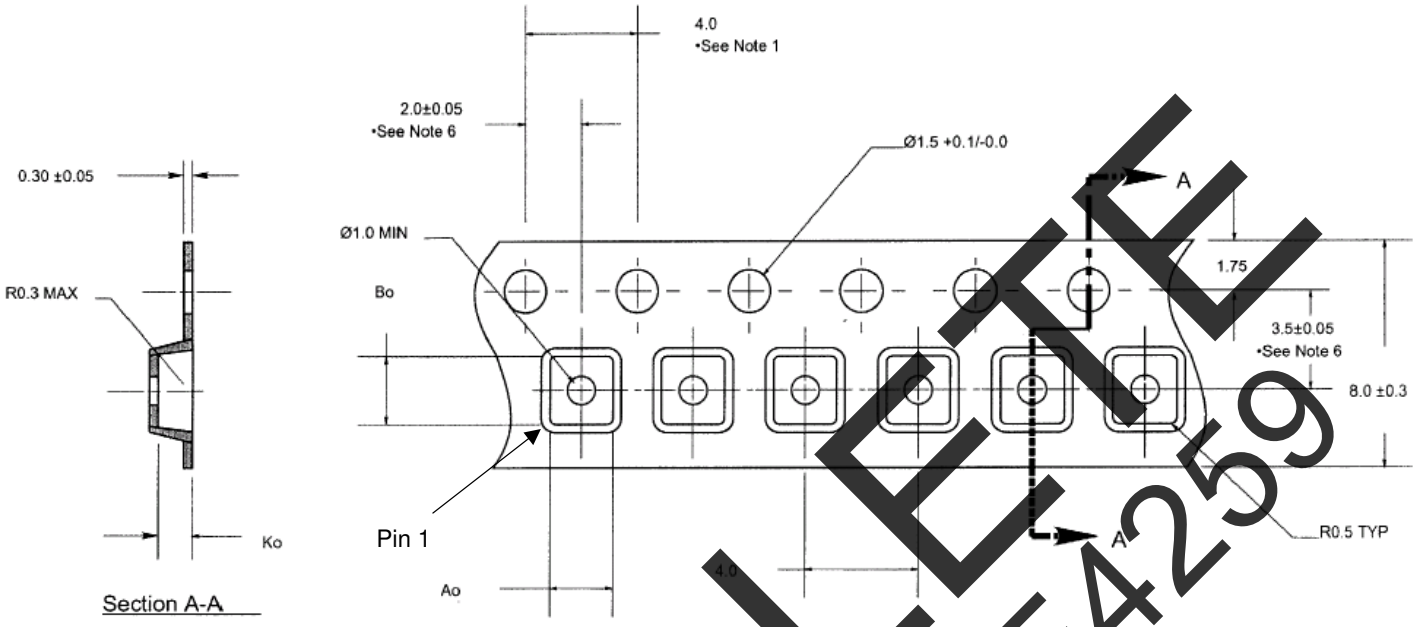


Figure 21. Tape and Reel Specifications



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 4.25 mm
Bo = 2.4 mm
Ko = 1.2 mm

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4283-00	PE4283-EK	PE4283-06SC70-EK	Evaluation Kit	1 / Box
4283-51	283	PE4283G-06SC70-7680A	Green 6-lead SC-70	7680 units / Canister
4283-52	283	PE4283G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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