Product Specification

PE45140

UltraCMOS® Power Limiter
20 MHz–2 GHz

Features

- Monolithic drop-in solution with no external components required
- Adjustable power limiting threshold from +12 dBm to +32 dBm
- Max power handling
  - +47 dBm Pulsed (50W)
  - +40 dBm CW (10W)
- Superior ESD rating and ESD protection
  - 8 kV HBM on RF pins to GND
  - 1 kV CDM on all pins
  - 200 V MM on all pins
- Unbiased power limiting operation
  - Fast response and recovery time of 1 ns
- Dual mode operation
  - Power limiting mode

Product Description

The PE45140 is a HaRP™ technology-enhanced RF power limiter designed for use in tactical and military communications receivers, land mobile radio and other high performance power limiting applications.

Unlike traditional PIN diode solutions the limiting threshold can be adjusted through a low current control voltage (V_{CTRL}), eliminating the need for external components such as DC blocking capacitors, RF choke inductors, and bias resistors.

This power limiter has symmetric RF ports that limit incident power up to 50W pulsed in both biased and unbiased conditions. It provides an extremely fast limiting response to undesired high power signals while delivering low insertion loss and high linearity under safe operating power levels.

The PE45140 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and

Figure 1. Functional Diagram

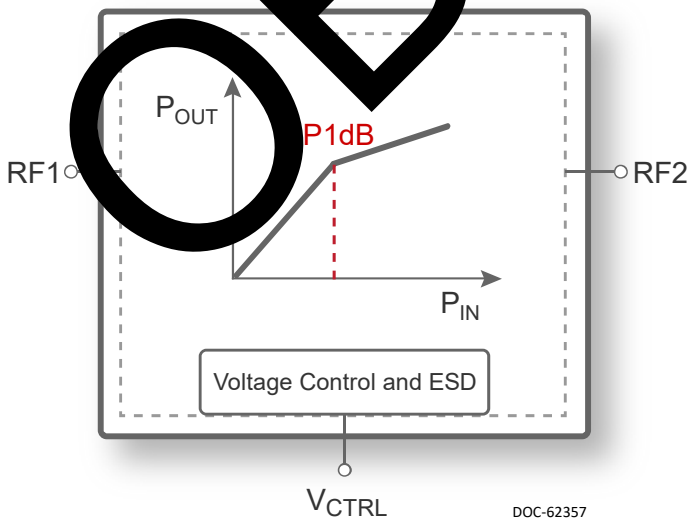


Figure 2. Package Type
12-lead 3x3 mm QFN

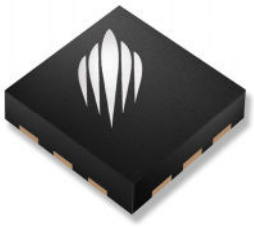


Table 1. Electrical Specifications @ +25°C (Z_S = Z_L = 50Ω), unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		20		2000	MHz
Power limiting mode					
Insertion loss	20 MHz–1 GHz 1–2 GHz		0.20 0.60	0.45 1.00	dB dB
Return loss	20 MHz–1 GHz 1–2 GHz		16 9		dB
P1dB / limiting threshold	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –0.5V @ 915 MHz		32 22		dBm dBm
Leakage power[1]	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –0.5V @ 915 MHz		25 21	34 31.5	dBm dBm
Leakage power slope	V_{CTRL} = –1.0V @ 915 MHz		0.4		dB/dB
Unbiased leakage power[1]	V_{CTRL} = 0V		23.5	27	dBm
Input IP2	V_{CTRL} = –2.5V @ 915 MHz		104		dBm
Input IP3	V_{CTRL} = –2.5V @ 915 MHz		54		dBm
Response / recovery time	1 GHz		1		ns
Power reflecting mode[2]					
Leakage power[1]	V_{CTRL} = +2.5V @ 915 MHz		–1	4.5	dBm
Switching time[3]	State change to 10% RF		390		µs

Notes: 1. Measured with +40 dBm CW applied at input.
2. This mode requires the control voltage to toggle between +2.5V and -2.5V. At +2.5V, the limiter shunt element circuit is a low impedance to ground, reflecting most of the incident power back to the source.
3. State change is V_{CTRL} toggle from –2.5V to +2.5V.

Figure 3. Pin Configuration (Top View)

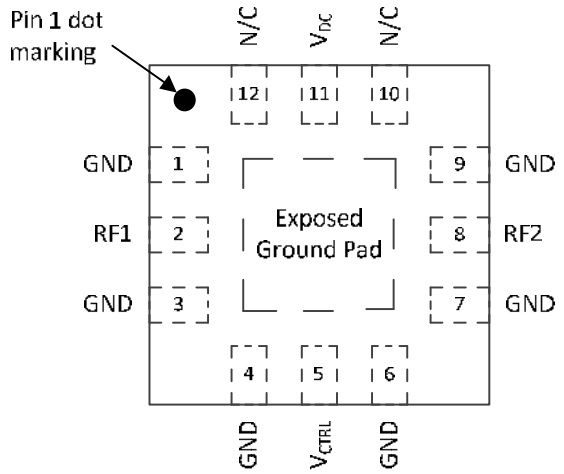


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1, 3, 4, 6, 7, 9	GND	Ground
2	RF1*	RF port 1
5	V_{CTRL}	Control
8	RF2*	RF port 2
10, 12	N/C	No connect
11	V_{DC}	DC voltage
Pad	GND	Exposed pad: Ground for proper operation

Note: * RF pins 2 and 8 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE45140 in the 12-lead 3x3 mm QFN package is MSL1.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
DC voltage	V_{DC}	2.5		3.3	V
Control voltage Power limiting mode Power reflecting mode	V_{CTRL}			–0.5 +2.5	V V
RF input power, CW[1]	P_{MAX}			40	dBm
RF input power, pulsed[2]	$P_{MAX,PULSED}$			47	dBm
RF input power, unbiased[2,3]	$P_{MAX,UNB}$				dBm
Operating temperature range	T_{OP}	–55		+85	°C
Operating junction temperature[1]	T_J			+270	°C

Notes: 1. [illegible], 100% duty cycle, in 10 min, 50Ω
2. [illegible]ulsed, 0.1% duty cycle of 1 µs pulse width in 10 min, 50Ω

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC voltage	V_{DC}	-0.3	3.6	V
Control voltage Power limiting mode Power reflecting mode	V_{CTRL}	–3.3	3.6	V
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM[1] All pins RF pins to GND	$V_{ESD,HBM}$		7000 8000	V V
ESD voltage MM[2], all pins	$V_{ESD,MM}$		200	V
ESD voltage CDM[3], all pins	$V_{ESD,CDM}$		1000	V

Notes: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)
2. Machine Model (JEDEC JESD22-A115)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the

ESD Protection Capability

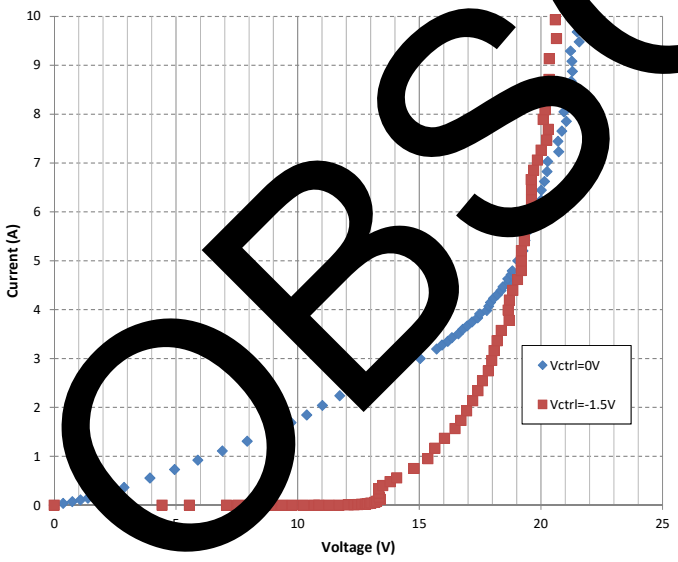
The PE45140 has the unique capability of being used as a voltage clamp in the event of an ESD strike. Clamping the output voltage can protect devices that follow from ESD damage and enable overall system ESD ratings to be increased.

The PE45140's ESD protection capability under biased and unbiased conditions is observed with a Transmission Line Pulse (TLP) measurement characterizing the product as an ESD clamp from each RF port to ground.

Table 5. Transmission Line Pulse Data vs. HBM

V_{CTRL}	HBM (V)	Max Current (A)	Voltage (V)
0	1000	0.7	4.5
–1.5	1000	0.7	14.5
0	2000	1.3	8
–1.5	2000	1.3	16
0	3000	2.0	11
–1.5	3000	2.0	

Figure 4. Transmission Line Pulse Measurement



Dual Mode Operation

Power Limiting Mode

The PE45140 performs as a linear power limiter with adjustable P1dB / limiting threshold. The P1dB / limiting threshold can be adjusted by changing the control voltage between –2.5V and –0.5V. If unbiased, or if V_{CTRL} = 0V, the PE45140 still offers power limiting protection.

Power Reflecting Mode

Power reflecting mode requires a power detector to sample the input power and a microcontroller to toggle the limiter control voltage between +2.5V and –2.5V based on the system protection requirements. At +2.5V, the limiter impedance to ground is less than 1Ω and most of the incident power will be reflected back to the source. At –2.5V, the device operates as in power limiting mode.

Thermal Data

When limiting high power RF signals, the junction temperature of the power limiter can rise significantly.

Special consideration needs to be made in the design of the PCB to properly dissipate the heat away from the part and maintain the +270°C maximum junction temperature.

It is recommended to use best design practices for high power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Special care also needs to be made to alleviate solder voiding under the part.

Table 5. Theta JC

Parameter	Min	Typ	Max	Unit
Theta JC		16		°C/W

Typical Performance Data @ +25°C (Z_S = Z_L = 50Ω), unless otherwise noted

Figure 5. Insertion Loss vs. Temperature

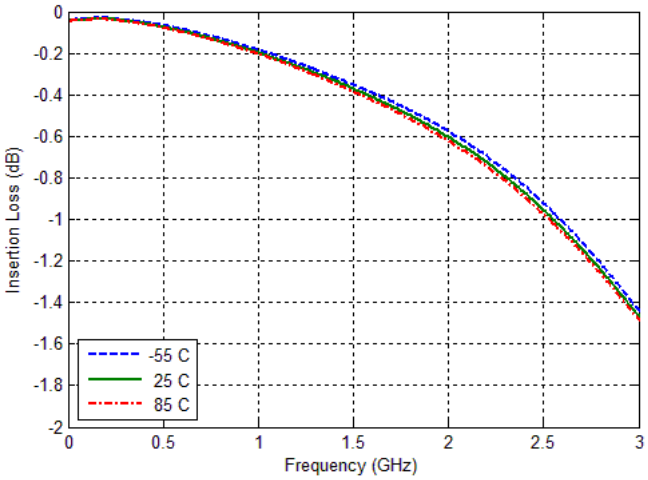
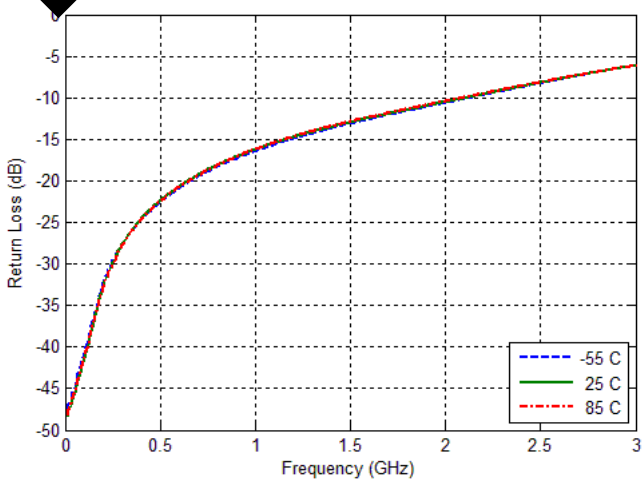


Figure 6. Input Return Loss vs. Temperature

Figure 7. Output Return Loss vs. Temperature



Typical Performance Data @ +25°C, 915 MHz ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 8. P_{OUT} vs. P_{IN} Over V_{CTRL}

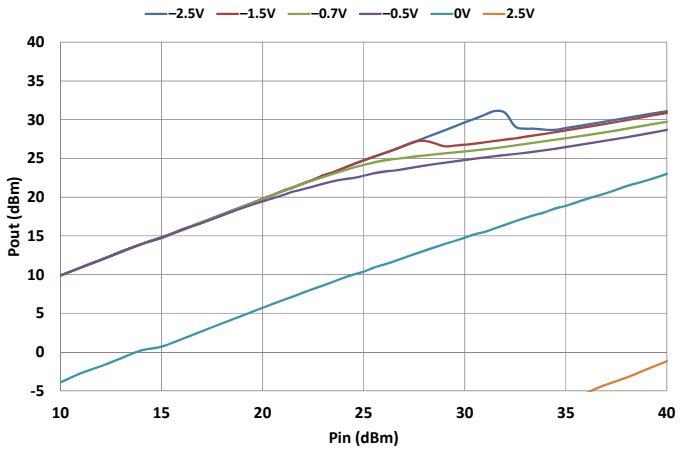


Figure 9. P_{OUT} vs. P_{IN} Over Frequency @ V_{CTRL} = –0.7V

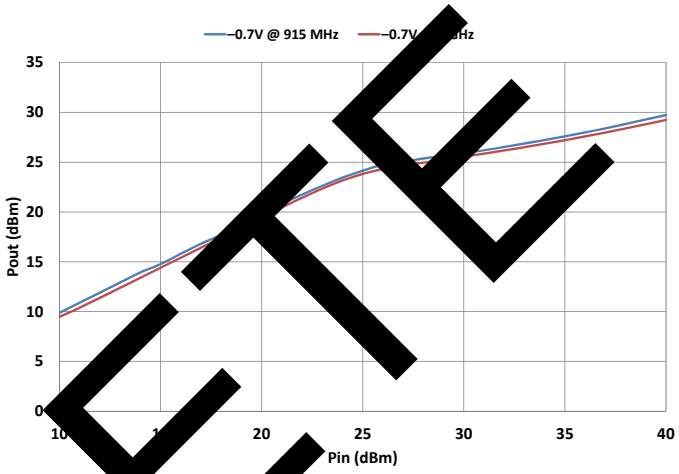
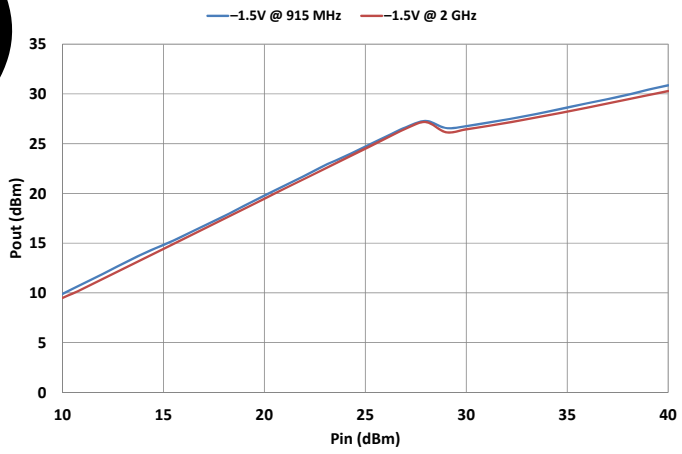


Figure 10. P1dB vs. V_{CTRL} Over Temperature

Figure 11. P_{OUT} vs. P_{IN} Over Frequency @ V_{CTRL} = –1.5V



Typical Performance Data @ +25°C, 915 MHz ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 12. IIP3 / IIP2 vs. V_{CTRL} Over Temperature

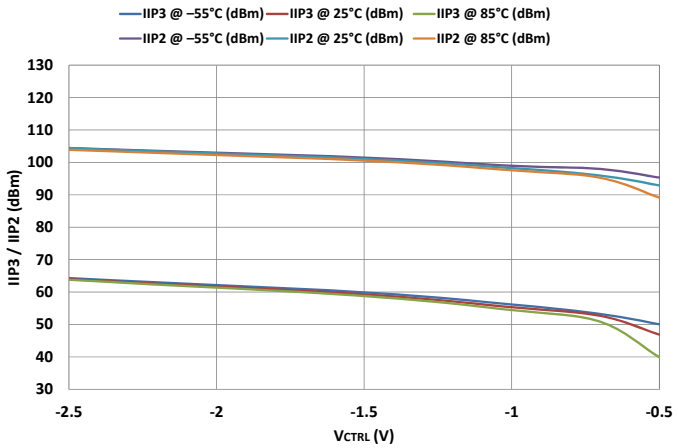


Figure 13. IIP3 / IIP2 vs. P_{IN} Over V_{CTRL}

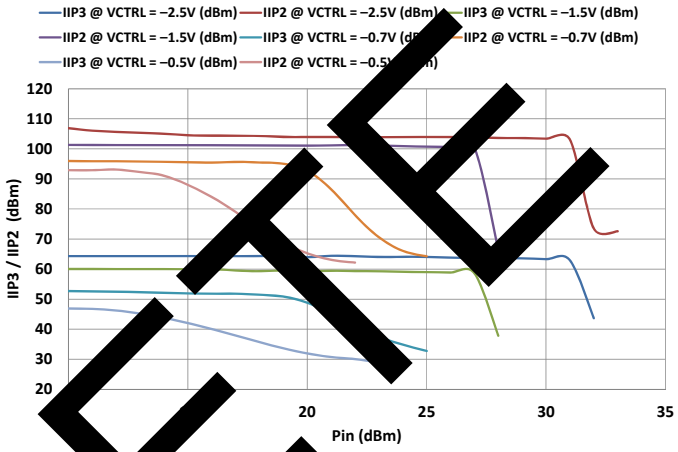


Figure 14. Leakage Power @ P_{MAX} vs. V_{CTRL} Over Temperature

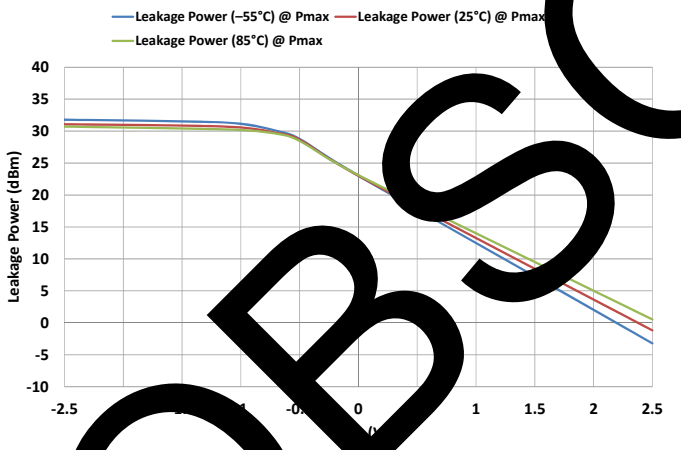
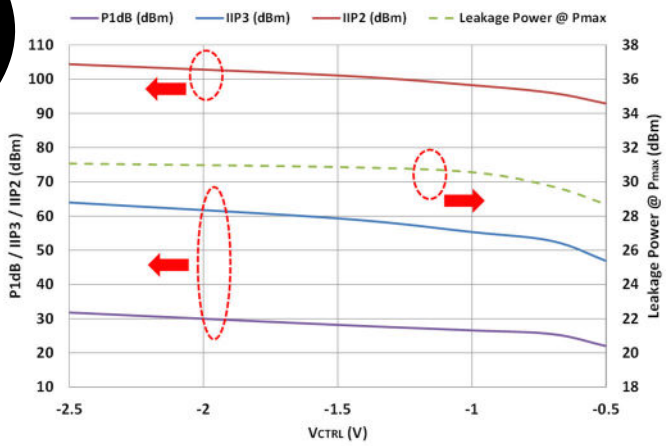


Figure 15. P1dB, IIP3, IIP2, Leakage Power @ P_{MAX} vs. V_{CTRL}



Evaluation Kit

The power limiter EVK board was designed to ease customer evaluation of Peregrine's PE45140. The bi-directional RF input and output are connected to RF1 and RF2 port through a 50Ω transmission line via SMA connectors J2 and J3. A through 50Ω transmission line is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. The 2-pin connectors J1 and J4 are connected to the external DC voltage V_{DC} and V_{CTRL}, respectively.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers RO4350B material with a 6.6 mil RF core and Er = 3.66. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 13.5 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

Figure 16. Evaluation Board Layout

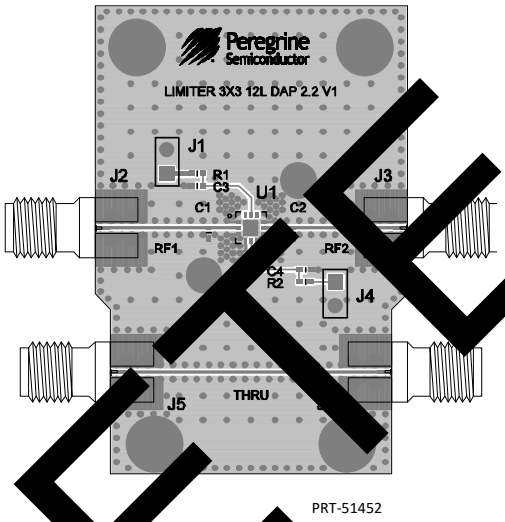
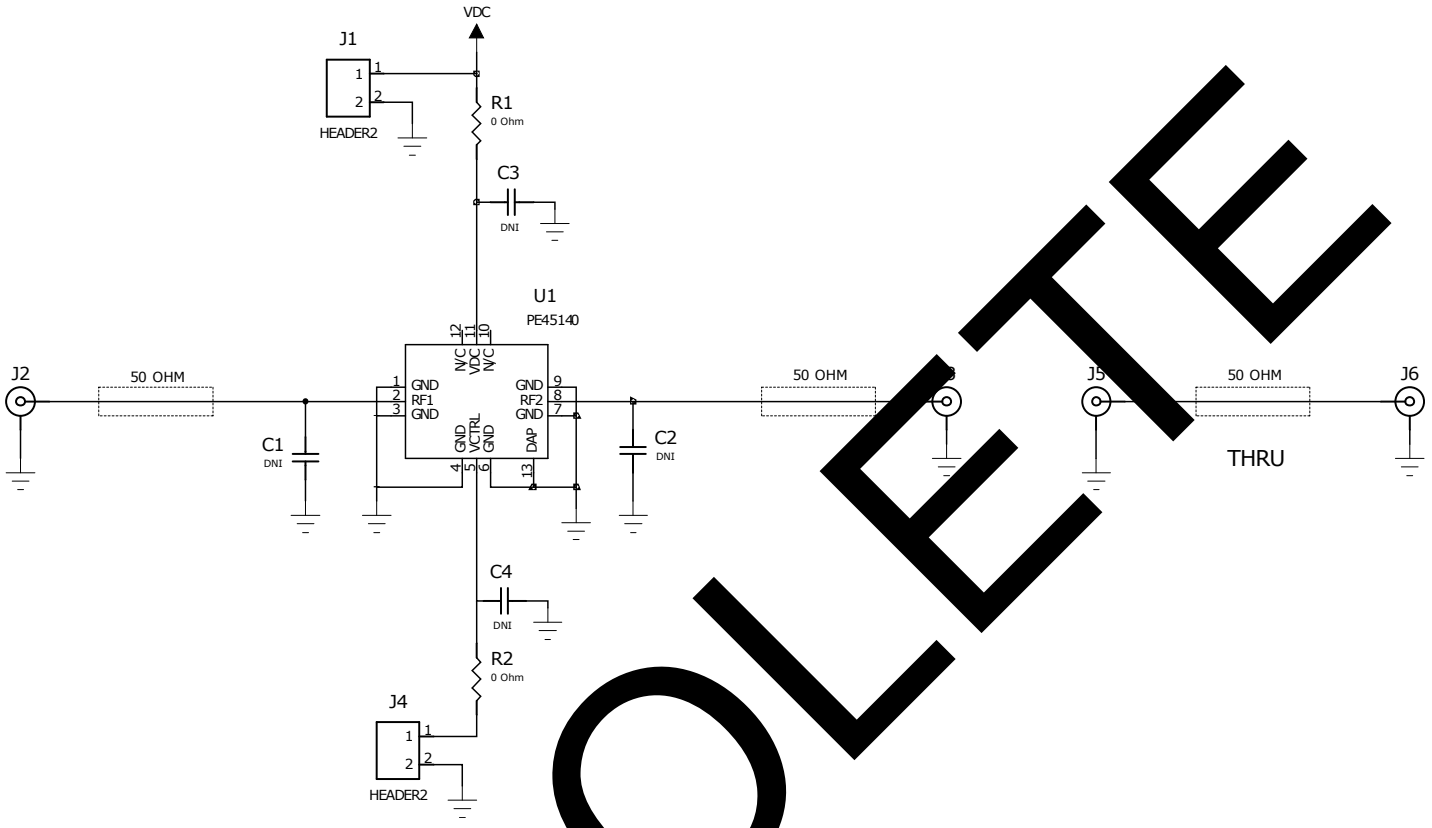


Figure 17. Evaluation Board Schematic



Caution: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)

DOC-44027

Figure 18. Package Drawing

12-lead 3x3 mm QFN

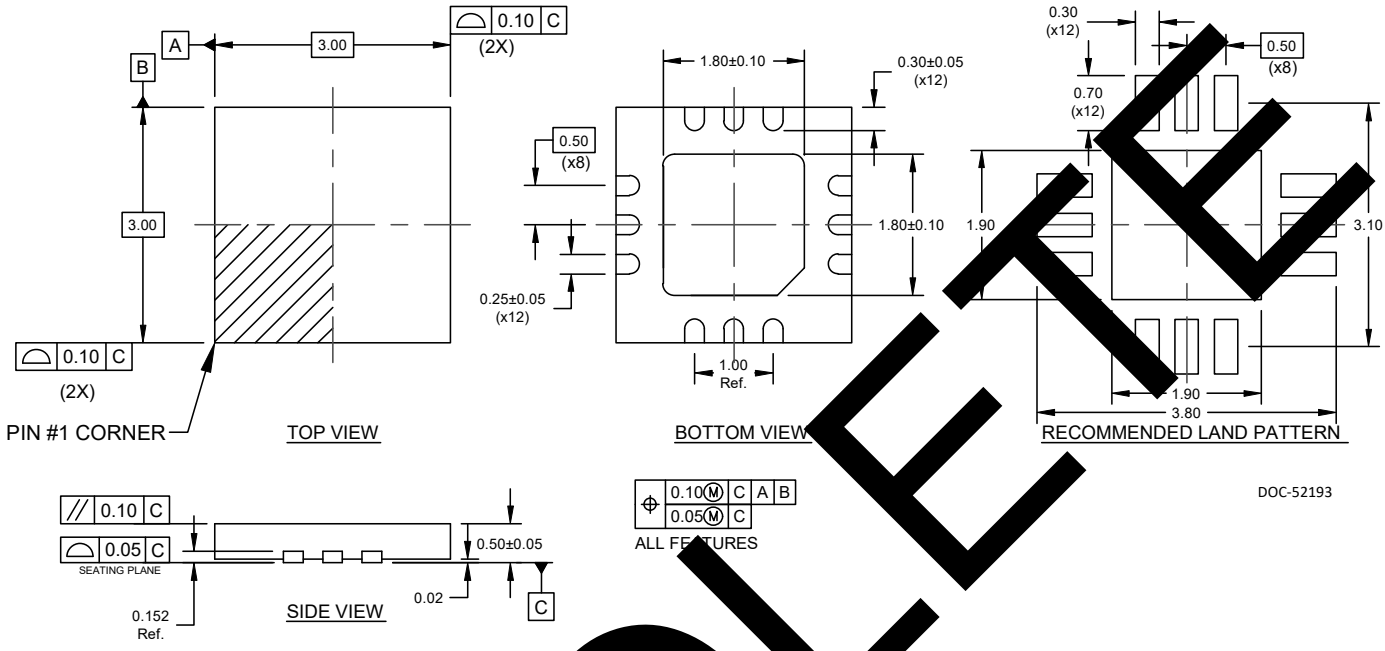
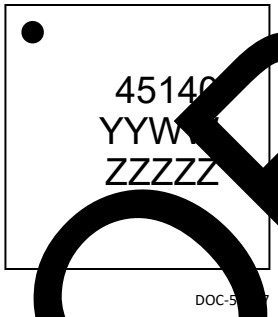


Figure 19. Top Marking Specifications



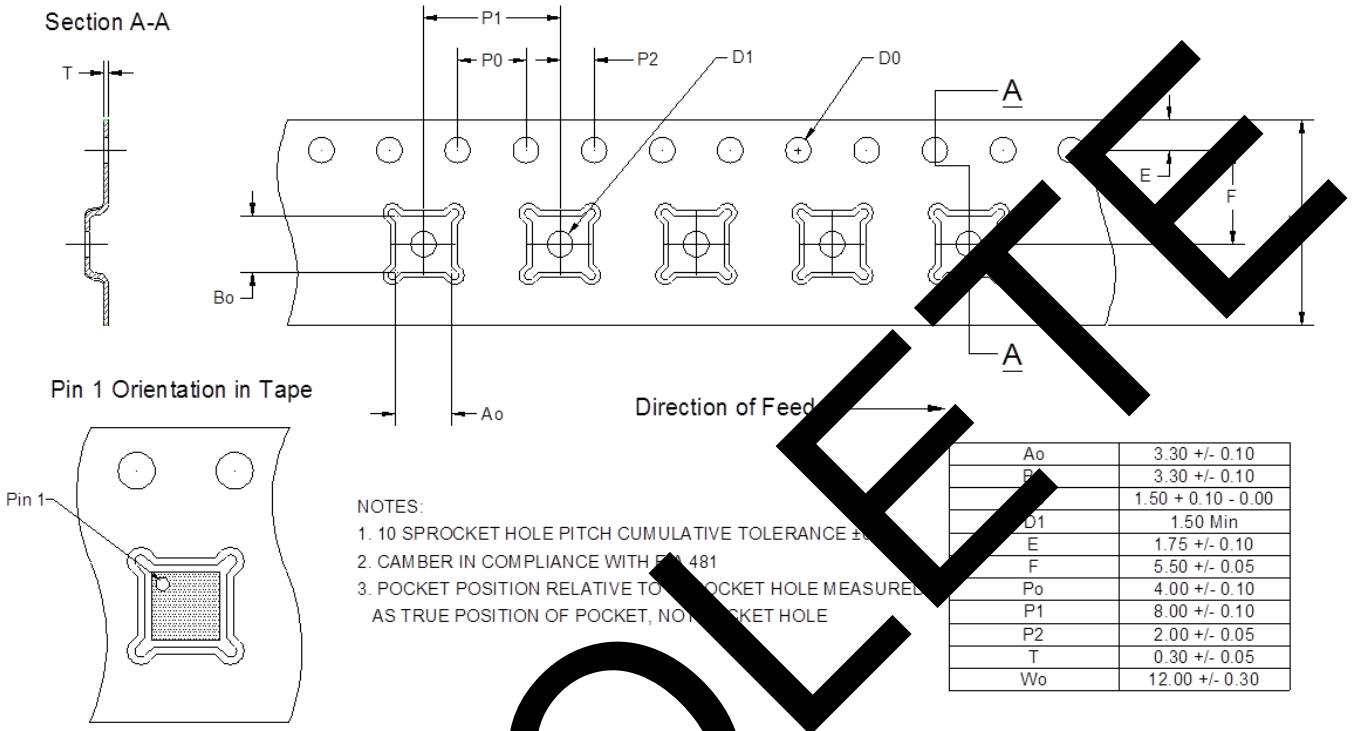
= Pin 1 designator

5140 = Five digit part number

YWW = Date code, last two digits of the year and work week

ZZZZZ = Five digits of the lot number

Figure 20. Tape and Reel Drawing



Ao	3.30 +/- 0.10
B	3.30 +/- 0.10
	1.50 + 0.10 - 0.00
D1	1.50 Min
E	1.75 +/- 0.10
F	5.50 +/- 0.05
Po	4.00 +/- 0.10
P1	8.00 +/- 0.10
P2	2.00 +/- 0.05
T	0.30 +/- 0.05
Wo	12.00 +/- 0.30

Table 6. Ordering Infor

Order Code	Description	Package	Shipping Method
PE45140A-X	PE 40 Power limiter	Green 12-lead 3x3 mm QFN	500 units / T&R
EK451	5140 Evaluation kit	Evaluation kit	1 / box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.