# Product Specification

# PE621020

**UltraCMOS® Digitally Tunable Capacitor (DTC) Optimized for 2G/3G/4G Impedance Tuning Applications, 100-3000 MHz**

## Product Description

PE621020 is a DuNE™-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine's UltraCMOS® technology. This highly versatile product supports a wide variety of tuning circuit topologies in series or shunt configurations. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications.

PE621010 offers high RF power handling and ruggedness while meeting challenging harmonic and linearity requirements enabled by Peregrine's HaRP™ technology. The device is controlled through the widely supported 3-wire (SPI compatible) 8-bit serial interface. All decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

DuNE™ devices feature ease of use while delivering superior RF performance in the form of tuning accuracy, monotonicity, tuning ratio, power handling, size, and quality factor. With built-in bias voltage generation and ESD protection, DTC products provide a monolithically integrated tuning solution for demanding RF applications.

## Features

- 5-bit 32-state Digitally Tunable Capacitor
- C = 1.88 - 14.0 pF (7.4:1 tuning ratio) in discrete 391 fF steps
- RF power handling (up to +26 dBm, 6 $V_{PK}$ RF) and high linearity for diversity applications
- Wide power supply range (2.3 to 3.1V) and low current consumption (typ. $I_{DD}$ = 30 µA @ 2.8V)
- 2 x 2 x 0.55 mm QFN package
- High ESD tolerance of 2kV HBM on all pins
- Applications include:
  - Antenna tuning
  - Tunable filters
  - Impedance matching

**Figure 1. Functional Block Diagram**

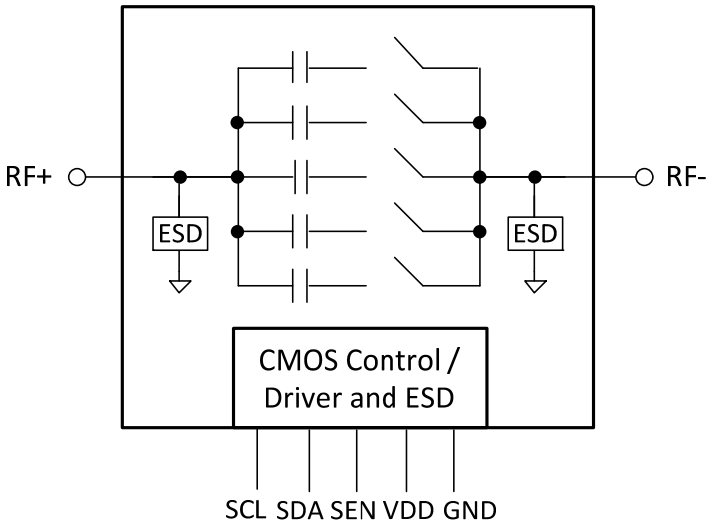
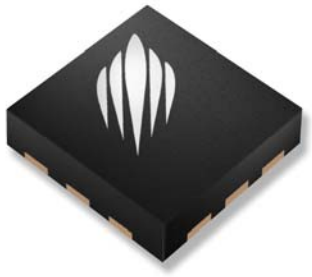



**Figure 2. Package Type**
12-lead 2 x 2 x 0.55 mm QFN package

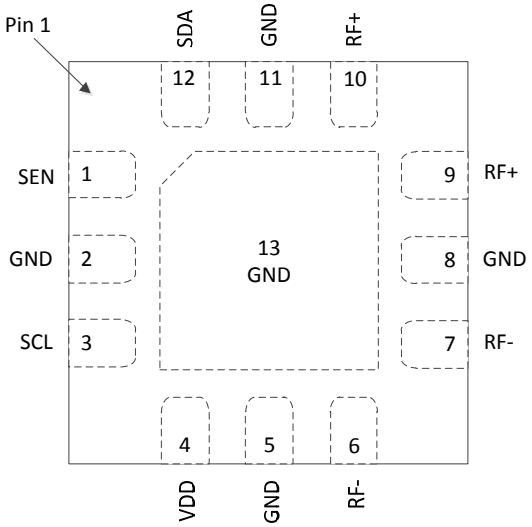


## Table 1. Electrical Specifications @ 25 °C, $V_{DD}$ = 2.8V (In shunt configuration between 50 Ω ports, RF- connected to GND)

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Frequency Range | | 100 | | 3000 | MHz |
| Minimum Capacitance | State 00000, 100 MHz (RF+ to Grounded RF-) | -10% | 1.88 | +10% | pF |
| Maximum Capacitance | State 11111, 100 MHz (RF+ to Grounded RF-) | -10% | 14.0 | +10% | pF |
| Tuning Ratio | $C_{max}/C_{min}$, 100 MHz | | 7.4:1 | | |
| Step Size | 5 bits (32 states), constant step size (100 MHz) | | 0.391 | | pF |
| Quality Factor ($C_{min}$)[1] | 698 - 960 MHz, with $L_s$ removed<br>1710 - 2170 MHz, with $L_s$ removed | | 50<br>28 | | |
| Quality Factor ($C_{max}$)[1] | 698 - 960 MHz, with $L_s$ removed<br>1710 - 2170 MHz, with $L_s$ removed | | 25<br>5 | | |
| Self Resonant Frequency | State 00000<br>State 11111 | | 4.7<br>1.6 | | GHz |
| Harmonics[4] | 2fo, 3fo: 698 to 915 MHz, Pin +26 dBm, 50 Ω<br>2fo, 3fo: 1710 to 1910 MHz, Pin +26 dBm, 50 Ω | | | -36<br>-36 | dBm<br>dBm |
| IMD3 | Bands I,II,V/VIII, +20 dBm CW @ TX freq,<br>-15 dBm CW @ 2Tx-Rx freq, 50 Ω | | -111 | -105 | dBm |
| Switching Time[2,3] | State change to 10/90% delta capacitance between any two states | | | 10 | µs |
| Start-up Time[2] | Time from $V_{DD}$ within specification to all performances within specification | | | 100 | µs |
| Wake-up Time[2,3] | State change from standby mode to RF state to all performances within specification | | | 100 | µs |

Note: 1. Q for a Shunt DTC based on a Series RLC equivalent circuit
$Q = X_C / R = (X-X_L)/R$, where $X = X_L + X_C$, $X_L = 2*pi*f*L$, $X_C = -1 / (2*pi*f*C)$, which is equal to removing the effect of parasitic inductance $L_S$
2. DC path to ground at RF+ and RF– must be provided to achieve specified performance
3. State change activated on falling edge of SEN following data word
4. Between 50 Ω ports in series or shunt configuration using a pulsed RF input with 4620 vs period, 50% duty cycle, measured per 3GPPTS45.005

## Figure 3. Pin Configuration (Top View)




## Table 2. Pin Descriptions

| Pin # | Pin Name | Description |
|---|---|---|
| 1 | SEN | Serial Enable (Active High) |
| 2 | GND | Digital and RF Ground |
| 3 | SCL | Serial Interface Clock Input |
| 4 | VDD | Supply |
| 5 | GND | Digital and RF Ground |
| 6 | RF- | Negative RF Port [1] |
| 7 | RF- | Negative RF Port [1] |
| 8 | GND | Digital and RF Ground [3] |
| 9 | RF+ | Positive RF Port [2] |
| 10 | RF+ | Positive RF Port [2] |
| 11 | GND | Digital and RF Ground |
| 12 | SDA | Serial Interface Data Input |
| 13 | GND | Digital and RF Ground [3] |

Notes: 1. Pins 6 and 7 must be tied together on PCB board to reduce inductance
2. Pins 9 and 10 must be tied together on PCB board to reduce inductance
3. Pin 2, 5, 8, 11 and 13 must be connected together on PCB

### Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE621020 in the 12-lead 2 x 2 QFN package is MSL1.

### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

## Table 3. Operating Ranges[1]

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ Supply Voltage | 2.3 | 2.8 | 3.1 | V |
| $I_{DD}$ Power Supply Current[5] | | 30 | 75 | µA |
| $I_{DD}$ Standby Current[5] | | 20 | 45 | µA |
| Control Voltage High | 1.2 | | 3.1 | V |
| Control Voltage Low | 0 | | 0.2 | V |
| Peak Operating RF Voltage[4]<br>$V_P$ to $V_M$<br>$V_P$ to RFGND<br>$V_M$ to RFGND | | | <br>6<br>6<br>6 | <br>$V_{PK}$<br>$V_{PK}$<br>$V_{PK}$ |
| RF Input Power (50Ω)[3,4]<br>Shunt | | | <br>+26 | <br>dBm |
| Input Control Current | | 1 | 10 | µA |
| Operating Temperature Range | -40 | +25 | +85 | °C |
| Storage Temperature Range | -65 | +25 | +150 | °C |

Notes: 1. Operation should be restricted to the limits in the Operating Ranges table
2. The DTC is active when STBY is low (set to 0) and in low-current stand-by mode when high (set to 1)
3. Maximum CW power available from a 50Ω source in shunt configuration
4. RF+ to RF- and RF+ and/or RF- to ground. Cannot exceed 6 $V_{PK}$ or max RF input power (whichever occurs first)
5. $I_{DD}$ current typical value is based on $V_{DD}$ = 2.8V. Max $I_{DD}$ is based on $V_{DD}$ = 3.1V

## Table 4. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Unit |
|---|---|---|---|---|
| $V_{ESD}$ | ESD Voltage (HBM, MIL_STD 883 Method 3015.7) | | 2000 | V |

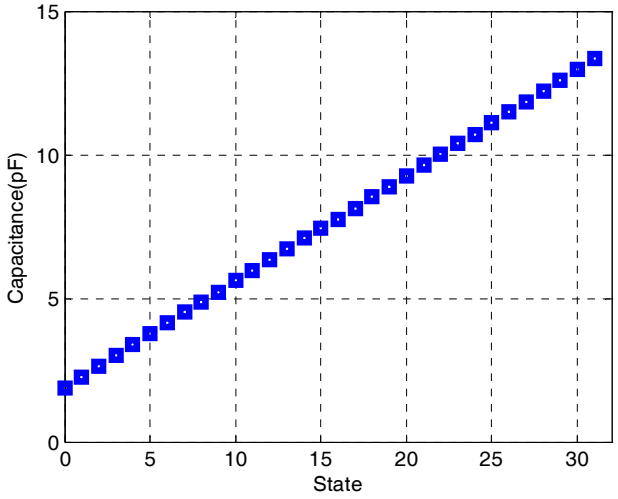
Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

### Electrostatic Discharge (ESD) Precautions

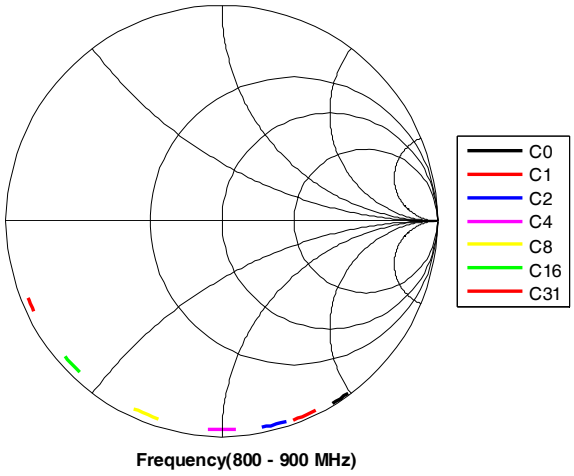
When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

## Performance Plots @ 25°C and 2.8V unless otherwise specified

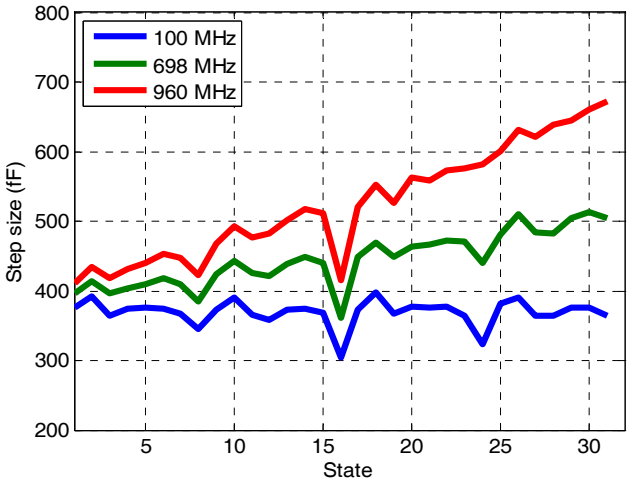
### Figure 4. Measured Shunt C (@ 100 MHz) vs State (temperature)



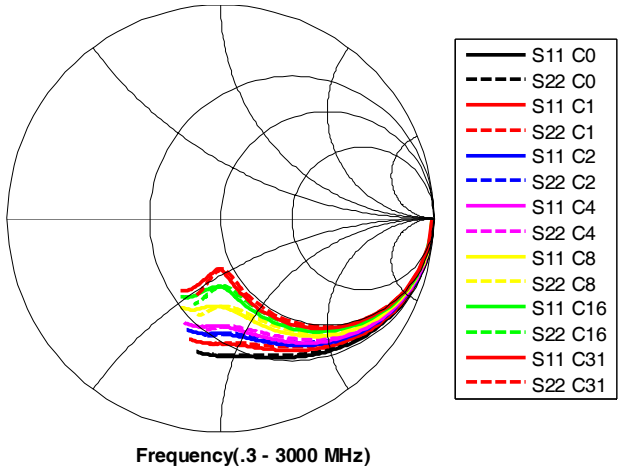

### Figure 5. Measured Shunt $S_{11}$ (major states)



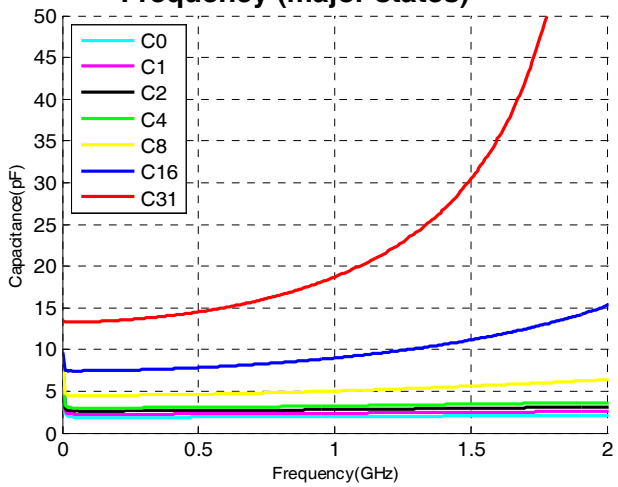

### Figure 6. Measured Step Size vs State (frequency)




### Figure 7. Measured Series $S_{11}/S_{22}$ (major states)




### Figure 8. Measured Shunt C vs Frequency (major states)




### Figure 9. Measured Series $S_{21}$ vs Frequency (major states)

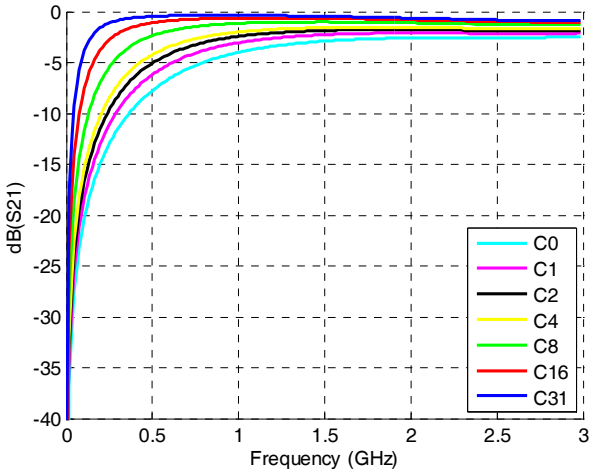


**Figure 10. Measured Shunt Q vs Frequency (major states)**

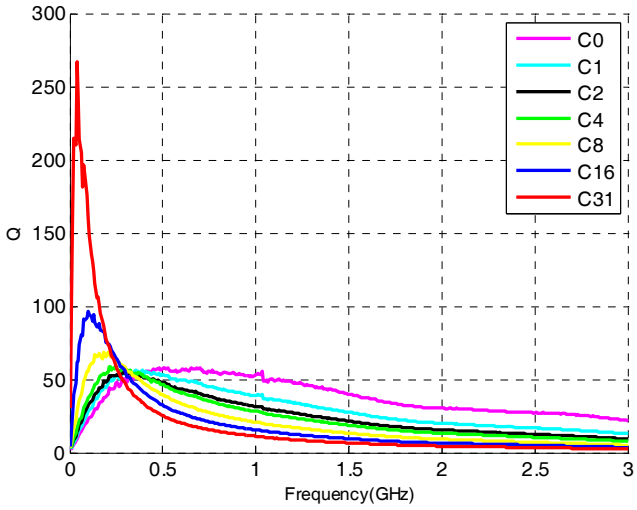



**Figure 11. Measured 2-Port Shunt S21 vs Frequency (major states)**

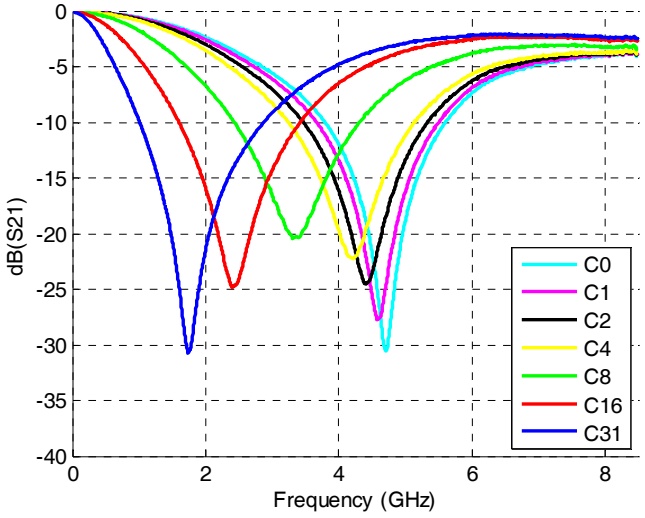



**Figure 12. Measured Self Resonance Frequency vs State**

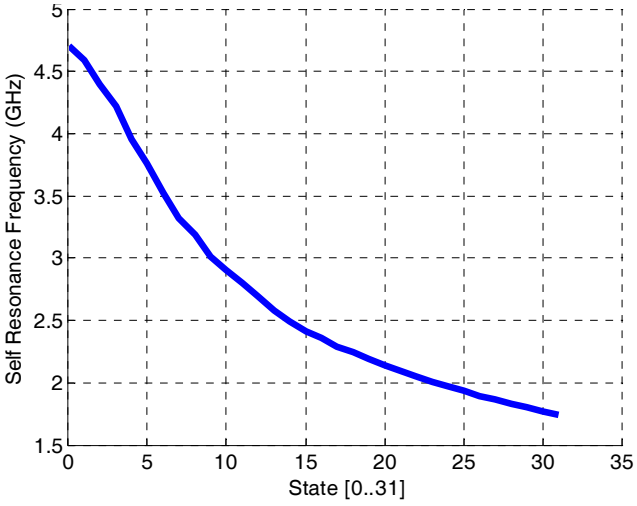
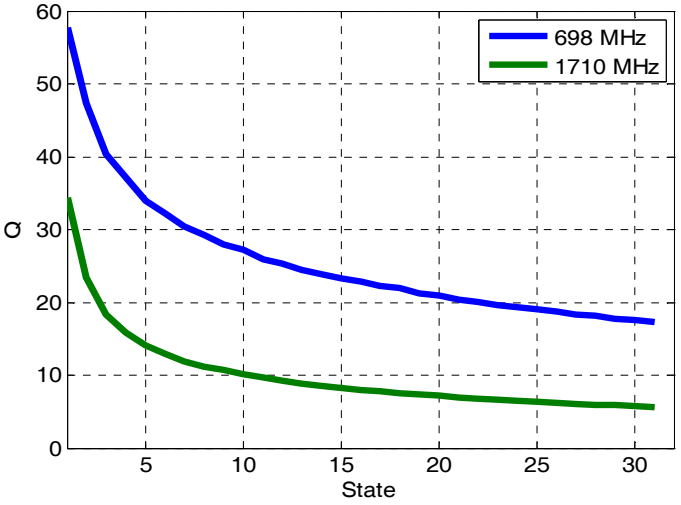



**Figure 13. Measured Shunt Q vs State**



## Serial Interface Operation and Sharing

The PE621020 is controlled by a three wire SPI-compatible interface with enable active high. As shown in *Figure 14*, the serial master initiates the start of a telegram by driving the SEN (Serial Enable) line high. Each bit of the 8-bit telegram (MSB first in) is clocked in on the rising edge of SCL (Serial Clock), as shown in *Table 5* and *Figure 14*. Transitions on SDA (Serial Data) are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last 8 bits it received.

More than 1 DTC can be controlled by one interface by utilizing a dedicated enable (SEN) line for each DTC. SDA, SCL, and $V_{DD}$ lines may be shared as shown in *Figure 15*. Dedicated SEN lines act as a chip select such that each DTC will only respond to serial transactions intended for them. This makes each DTC change states sequentially as they are programmed.

Alternatively, a dedicated SDA line with common SEN can be used. This allows all DTCs to change states simultaneously, but requires all DTCs to be programmed even if the state is not changed.

**Figure 14. Serial Interface Timing Diagram**

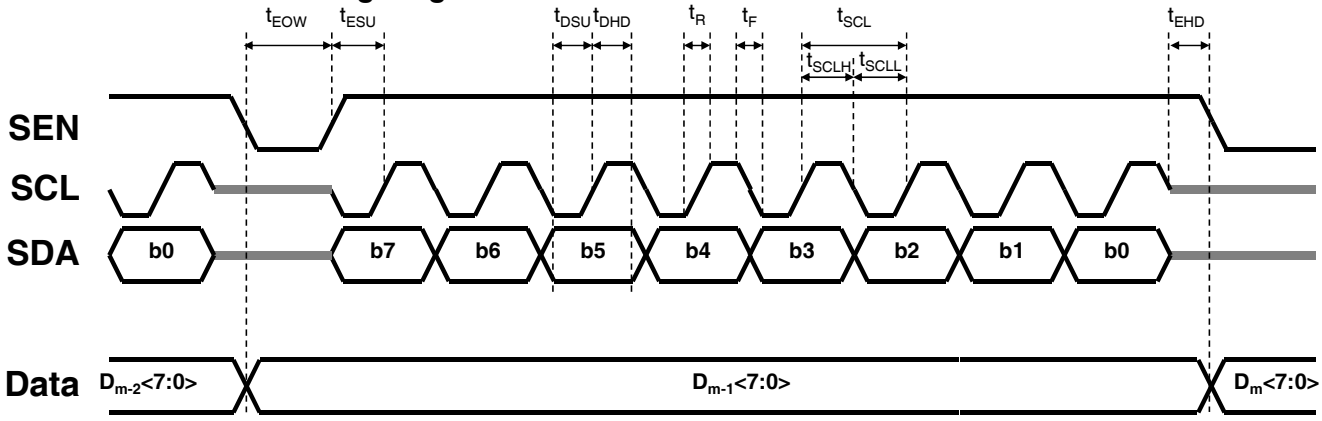



**Table 5. 8-Bit Serial Programming Register Map**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| 0[1] | 0[1] | STB[2] | d4 | d3 | d2 | d1 | d0 |

MSB (first in) LSB (last in)

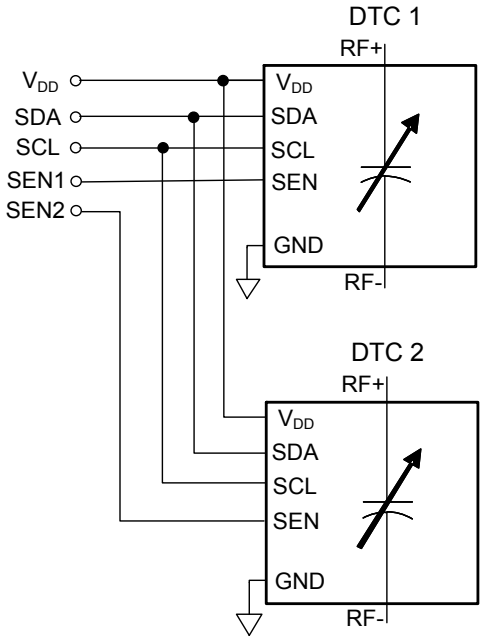
Note: 1. These bits are reserved and must be written to 0 for proper operation
2. The DTC is active when low (set to 0) and in low-current stand-by mode when high (set to 1)

**Table 6. Serial Interface AC Characteristics**

2.3V < $V_{DD}$ < 3.1V, -40 °C < $T_A$ < +85 °C, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SCL}$ | Serial Clock Period | 38.4 | | ns |
| $t_{SCLL}$ | SCL Low Time | 13.2 | | ns |
| $t_{SCLH}$ | SCL High Time | 13.2 | | ns |
| $t_R$ | SCL, SDA, SEN Rise Time | | 6.5 | ns |
| $t_F$ | SCL, SDA, SEN Fall Time | | 6.5 | ns |
| $t_{ESU}$ | SEN rising edge to SCL rising edge | 19.2 | | ns |
| $t_{EHD}$ | SCL falling edge to SEN falling edge | 19.2 | | ns |
| $t_{DSU}$ | SDA valid to SCL rising edge | 13.2 | | ns |
| $t_{DHD}$ | SDA valid after SCL rising edge | 13.2 | | ns |
| $t_{EOW}$ | SEN falling edge to SEN rising edge | 38.4 | | ns |

**Figure 15. Recommended Bus Sharing**



## Equivalent Circuit Model Description

The DTC Equivalent Circuit Model includes all parasitic elements and is accurate in both Series and Shunt configurations, reflecting physical circuit behavior accurately and providing very close correlation to measured data. It can easily be used in circuit simulation programs. Simple equations are provided for the state dependent parameters.

The Tuning Core capacitance $C_S$ represents capacitance between RF+ and RF- ports. It is linearly proportional to state (0 to 31 in decimal) in a discrete fashion. The Series Tuning Ratio is defined as $C_{Smax}/C_{Smin}$.

$C_{P1}$ and $C_{P2}$ represent the circuit and package parasitics from RF ports to GND. In shunt configuration the total capacitance of the DTC is higher due to parallel combination of $C_P$ and $C_S$. The capacitance seen looking into RF+ is $C_S$+$C_{P1}$ (when RF- is grounded) and $C_S$+$C_{P2}$ for RF-, respectively. In Series configuration, $C_S$ and $C_P$ do not add in parallel and the DTC appears as an impedance transformation network.

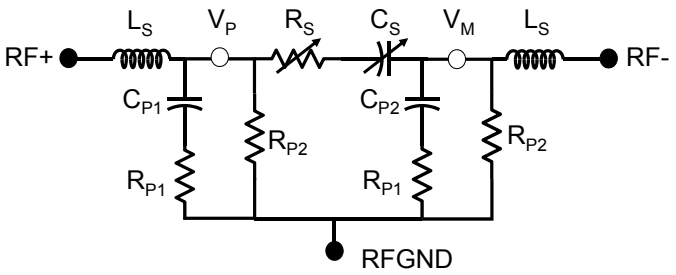
Parasitic inductance due to circuit and package is modeled as $L_S$ and causes the apparent capacitance of the DTC to increase with frequency until it reaches Self Resonant Frequency (SRF). The value of SRF depends on state and is approximately inversely proportional to the square root of capacitance.

The overall dissipative losses of the DTC are modeled by $R_S$, $R_{P1}$ and $R_{P2}$ resistors. The parameter $R_S$ represents the Equivalent Series Resistance (ESR) of the tuning core and is dependent on state. $R_{P1}$ and $R_{P2}$ represent losses due to the parasitic and biasing networks.

### Table 7. Maximum Operating RF Voltage

| Condition | Limit |
|---|---|
| $V_P$ to $V_M$ | 6 $V_{PK}$ |
| $V_P$ to RFGND | 6 $V_{PK}$ |
| $V_M$ to RFGND | 6 $V_{PK}$ |

### Figure 16. Equivalent Circuit Model Schematic




### Table 8. Equivalent Circuit Model Parameters

| Variable | **Equation** (state = 0, 1, 2…31) | Unit |
|---|---|---|
| $C_S$ | 0.394*state + 1.456 | pF |
| $R_S$ | 15/(state+15/(state+0.4)) + 0.4 | Ω |
| $C_{P1}$ | -0.0026*state + 0.4155 | pF |
| $C_{P2}$ | 0.0029*state + 0.4914 | pF |
| $R_{P1}$ | 4 | Ω |
| $R_{P2}$ | 22000 + 6*(state)^3 | Ω |
| $L_S$ | 0.4 | nH |

### Table 9. Equivalent Circuit Data

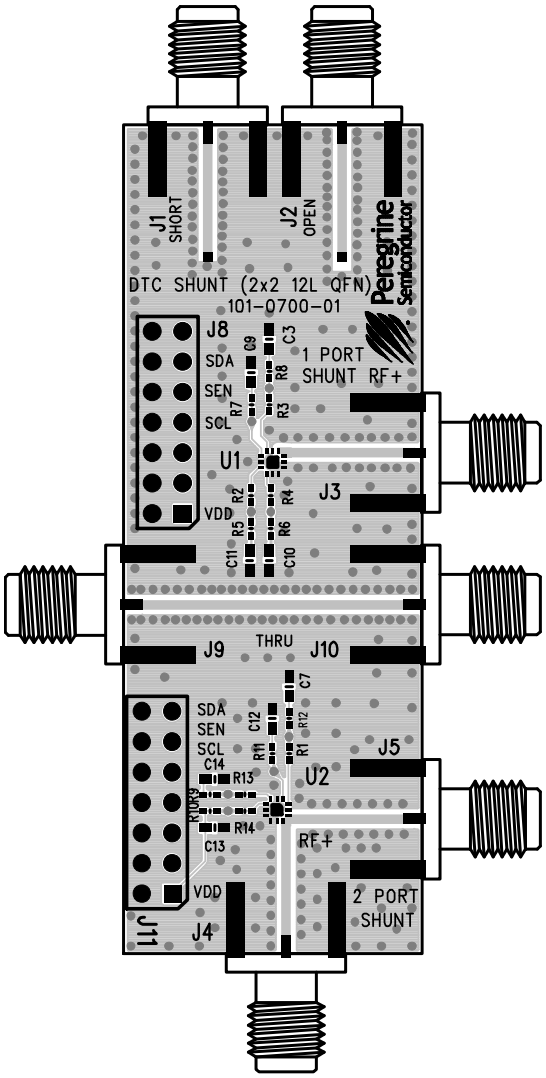
| State | | | DTC Core | | Parasitic Elements | | |
|---|---|---|---|---|---|---|---|
| Hex | Bin | Dec | Cs [pF] | Rs [Ω] | Cp1 [pF] | Cp2 [pF] | Rp2 [kΩ] |
| 0x00 | 00000 | 0 | 1.40 | 0.80 | 0.42 | 0.49 | 22.0 |
| 0x01 | 00001 | 1 | 1.79 | 1.68 | 0.41 | 0.49 | 22.0 |
| 0x02 | 00010 | 2 | 2.19 | 2.22 | 0.41 | 0.50 | 22.0 |
| 0x03 | 00011 | 3 | 2.58 | 2.42 | 0.41 | 0.50 | 22.2 |
| 0x04 | 00100 | 4 | 2.98 | 2.42 | 0.41 | 0.50 | 22.4 |
| 0x05 | 00101 | 5 | 3.37 | 2.33 | 0.40 | 0.51 | 22.8 |
| 0x06 | 00110 | 6 | 3.76 | 2.20 | 0.40 | 0.51 | 23.3 |
| 0x07 | 00111 | 7 | 4.16 | 2.06 | 0.40 | 0.51 | 24.1 |
| 0x08 | 01000 | 8 | 4.55 | 1.93 | 0.39 | 0.51 | 25.1 |
| 0x09 | 01001 | 9 | 4.95 | 1.82 | 0.39 | 0.52 | 26.4 |
| 0x0A | 01010 | 10 | 5.34 | 1.71 | 0.39 | 0.52 | 28.0 |
| 0x0B | 01011 | 11 | 5.73 | 1.62 | 0.39 | 0.52 | 30.0 |
| 0x0C | 01100 | 12 | 6.13 | 1.54 | 0.38 | 0.53 | 32.4 |
| 0x0D | 01101 | 13 | 6.52 | 1.46 | 0.38 | 0.53 | 35.2 |
| 0x0E | 01110 | 14 | 6.92 | 1.40 | 0.38 | 0.53 | 38.5 |
| 0x0F | 01111 | 15 | 7.31 | 1.34 | 0.38 | 0.53 | 42.3 |
| 0x10 | 10000 | 16 | 7.70 | 1.29 | 0.37 | 0.54 | 46.6 |
| 0x11 | 10001 | 17 | 8.10 | 1.24 | 0.37 | 0.54 | 51.5 |
| 0x12 | 10010 | 18 | 8.49 | 1.20 | 0.37 | 0.54 | 55.0 |
| 0x13 | 10011 | 19 | 8.89 | 1.16 | 0.37 | 0.55 | 63.2 |
| 0x14 | 10100 | 20 | 9.28 | 1.12 | 0.36 | 0.55 | 70.0 |
| 0x15 | 10101 | 21 | 9.67 | 1.09 | 0.36 | 0.55 | 77.6 |
| 0x16 | 10110 | 22 | 10.07 | 1.06 | 0.36 | 0.56 | 85.9 |
| 0x17 | 10111 | 23 | 10.46 | 1.03 | 0.36 | 0.56 | 95.0 |
| 0x18 | 11000 | 24 | 10.86 | 1.01 | 0.35 | 0.56 | 104.9 |
| 0x19 | 11001 | 25 | 11.25 | 0.99 | 0.35 | 0.56 | 115.8 |
| 0x1A | 11010 | 26 | 11.64 | 0.96 | 0.35 | 0.57 | 127.5 |
| 0x1B | 11011 | 27 | 12.04 | 0.94 | 0.35 | 0.57 | 140.1 |
| 0x1C | 11100 | 28 | 12.43 | 0.93 | 0.34 | 0.57 | 153.7 |
| 0x1D | 11101 | 29 | 12.83 | 0.91 | 0.34 | 0.58 | 168.3 |
| 0x1E | 11110 | 30 | 13.22 | 0.89 | 0.34 | 0.58 | 184.0 |
| 0x1F | 11111 | 31 | 13.61 | 0.88 | 0.33 | 0.58 | 200.7 |

## Evaluation Board

The 101-0700 Evaluation Board (EVB) was designed for accurate measurement of the DTC impedance and loss. Two configurations are available: 1 Port Shunt (J3) and 2 Port Shunt (J4, J5). Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used for performing port extensions and accounting for electrical length and transmission line loss. The Thru (J9, J10) standard can be used to estimate PCB transmission line losses for scalar de-embedding of the 2 Port Shunt configuration (J4, J5).

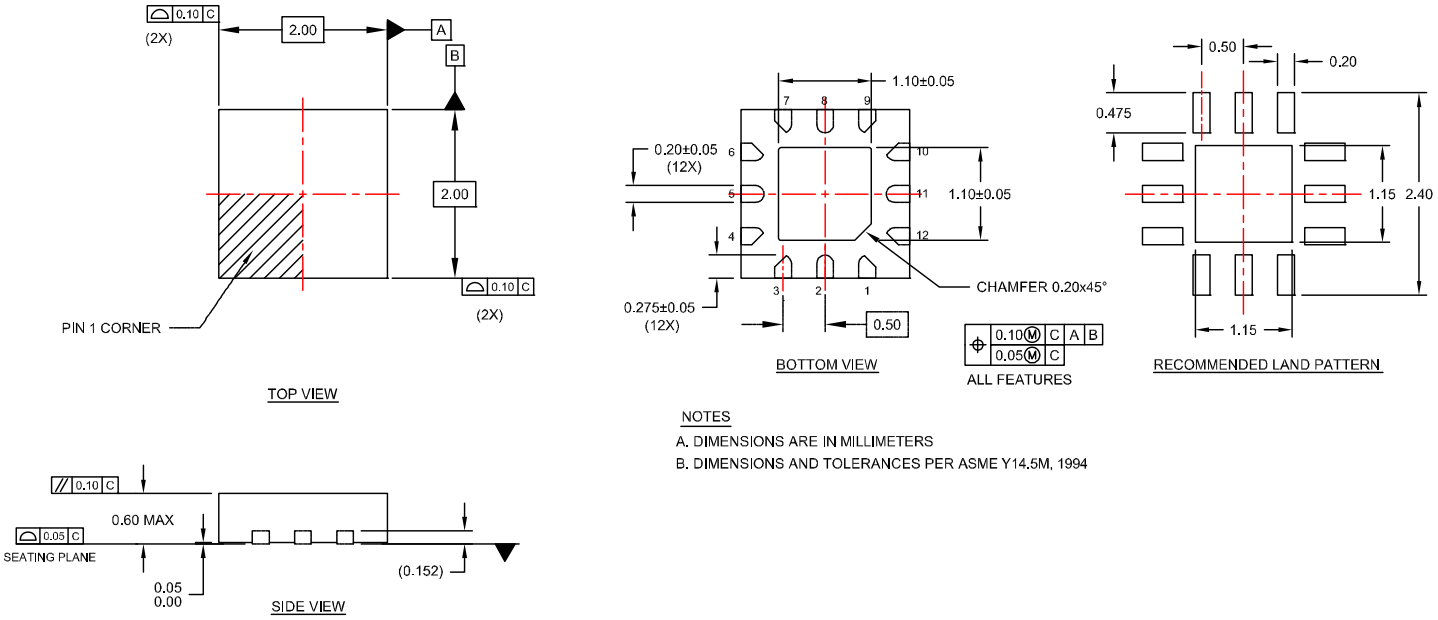
The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B ($\varepsilon_r$ = 3.48) and 2 inner layers of FR4 ($\varepsilon_r$ = 4.80). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.036 mm).

**Figure 17. Evaluation Board Layout**



## Figure 18. Package Drawing

12-lead 2 x 2 x 0.55 mm QFN

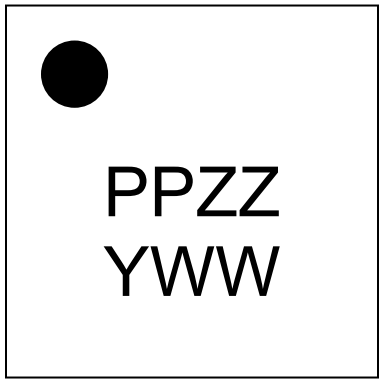



NOTES

A. DIMENSIONS ARE IN MILLIMETERS

B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

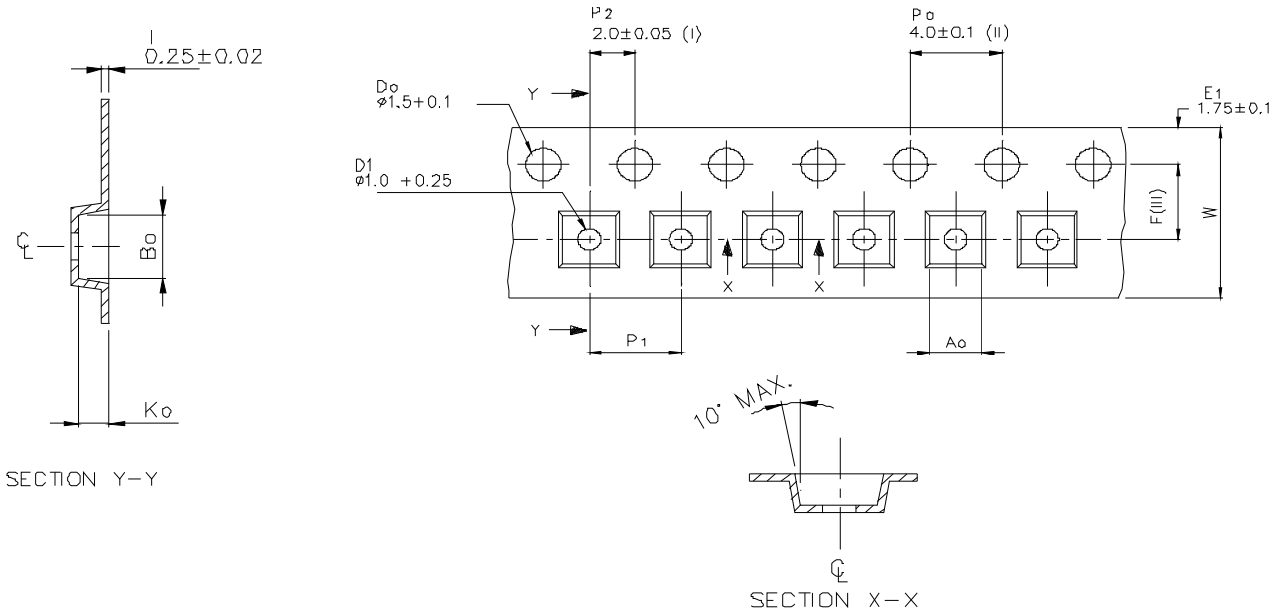
## Figure 19. Top Marking Specifications

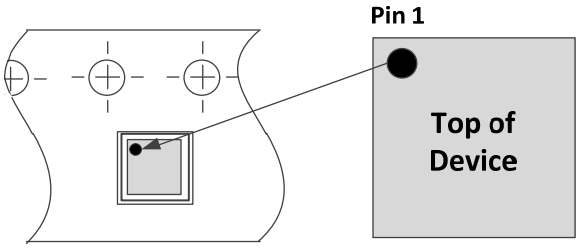



17-0112

| Marking Spec Symbol | Package Marking | Definition |
|---|---|---|
| **PP** | CP | Part number marking for PE621020 |
| **ZZ** | 00-99 | Last two digits of lot code |
| **Y** | 0-9 | Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc) |
| **WW** | 01-53 | Work week |

**Figure 20. Tape and Reel Specifications**
12-lead 2 x 2 x 0.55 mm QFN




Device Orientation in Tape

## Table 10. Ordering Information

| Order Code | Package | Description | Shipping Method |
|---|---|---|---|
| PE621020MLAA-Z | 12-lead 2 x 2 x 0.55 mm QFN | Package Part in Tape and Reel | 3,000 units / T&R |
| EK621020-11 | Evaluation Kit | Evaluation Kit | 1 set / box |

## Sales Contact and Information

For sales and contact information please visit www.psemi.com.