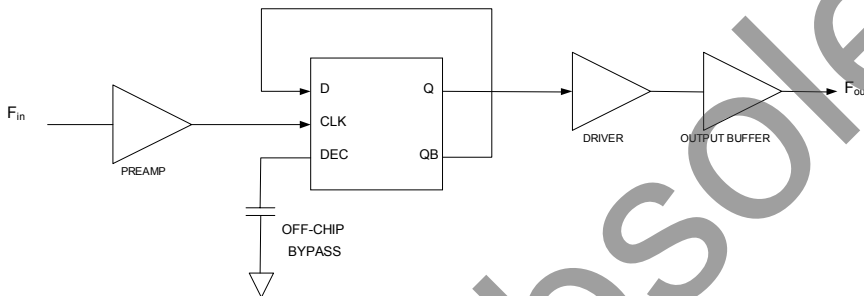


Product Description

The PE83501 is a high-performance dynamic UltraCMOS™ prescaler with a fixed divide ratio of 2. Its operating frequency range is 400 MHz to 3.5 GHz. The PE83501 operates on a nominal 3 V supply and draws only 12 mA. It is packaged in a small 8-lead MSOP and is ideal for frequency scaling and microwave PLL synthesis solutions.

The PE83501 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram



**3.5 GHz Low Power UltraCMOS™
Divide-by-2 Prescaler
Military Operating Temperature Range**

Features

- High-frequency operation: 400 MHz to 3.5 GHz
- Fixed divide ratio of 2
- Low-power operation: 12 mA typical @ 3 V
- Small package: 8-lead MSOP
- Low cost

Figure 2. Package Type

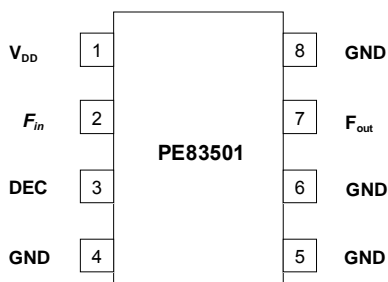
8-lead MSOP



Table 1. Electrical Specifications ($Z_S = Z_L = 50 \Omega$)

$2.85V \leq V_{DD} \leq 3.15 V$; $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			13	18	mA
Input Frequency (F_{in})		400		3500	MHz
Input Power (P_{in})	$400 \text{ MHz} \leq F_{in} \leq 2.0 \text{ GHz}$	-10		+10	dBm
	$2.0 \text{ GHz} < F_{in} \leq 2.8 \text{ GHz}$	0		+10	dBm
	$2.8 \text{ GHz} < F_{in} \leq 3.5 \text{ GHz}$	+5		+10	dBm
Output Power (P_{out})	$400 \text{ MHz} \leq F_{in} \leq 3.5 \text{ GHz}$	-15			dBm

Figure 3. Pin Configuration (Top View)

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Power supply pin. Bypassing is required.
2	F_{in}	Input signal pin. DC blocking capacitor required (15 pF typical)
3	DEC	Power supply decoupling pin. Place a capacitor as close as possible and connect directly to the ground plane.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	GND	Ground pin.
7	F_{out}	Divided frequency output pin. DC blocking capacitor required (47 pF typical)
8	GND	Ground pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		4.0	V
P_{in}	Input Power		15	dBm
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-55	125	°C
V_{ESD}	ESD voltage (Human Body Model)	250		V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The PE83501 divides a 400 MHz to 3.5 GHz input signal by two, producing a 200 MHz to 1.75 GHz output signal. To work properly, pin 3 must be supplied with a bypass capacitor to ground. In addition, the input and output signals (pins 2 & 7) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 4.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 9 for a layout example.

Figure 4. Test Circuit Block Diagram

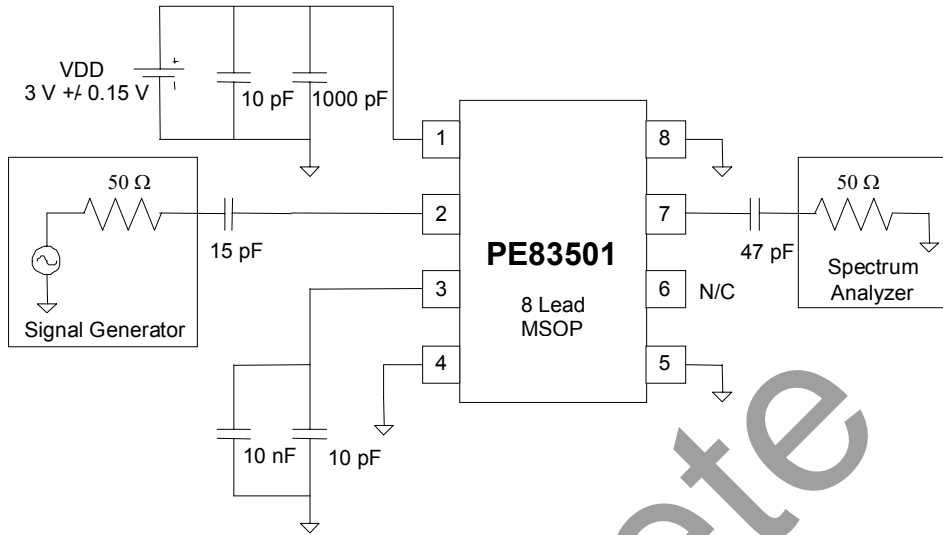
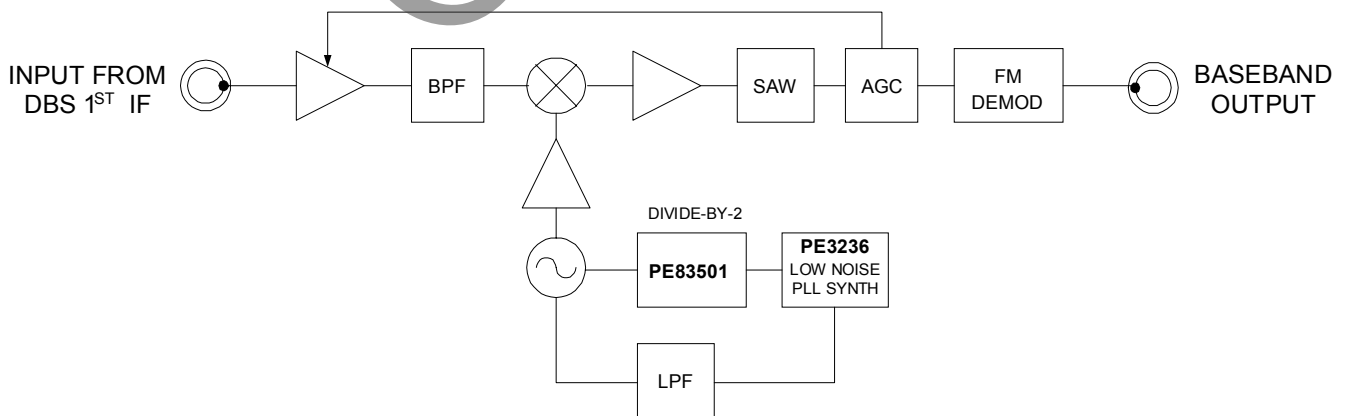


Figure 5. High Frequency System Application

The wideband frequency of operation of the *PE83501* makes it an ideal part for use in a DBS downconverter system.



Typical Performance Data: $V_{DD} = 3.0\text{ V}$

Figure 6. Input Sensitivity

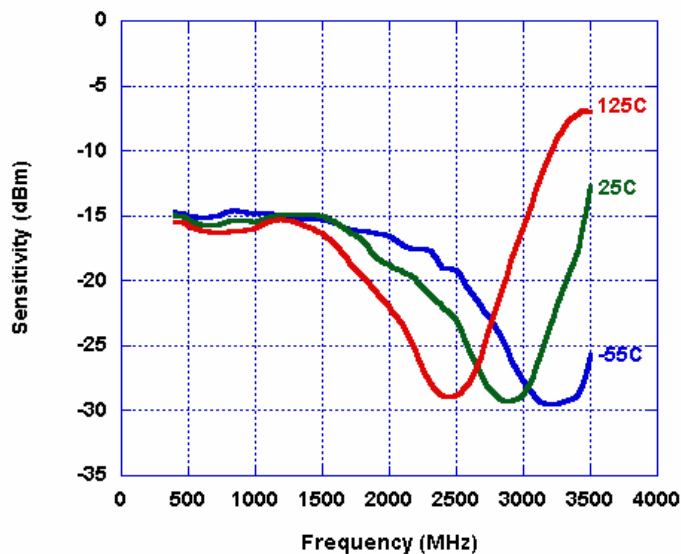


Figure 7. Device Current

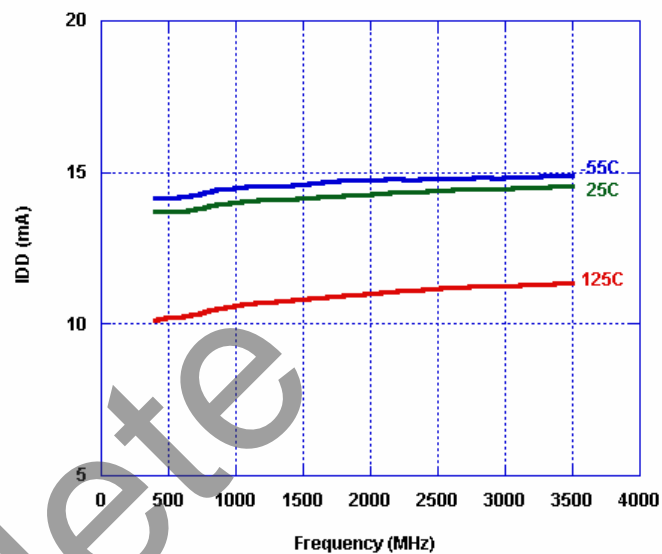
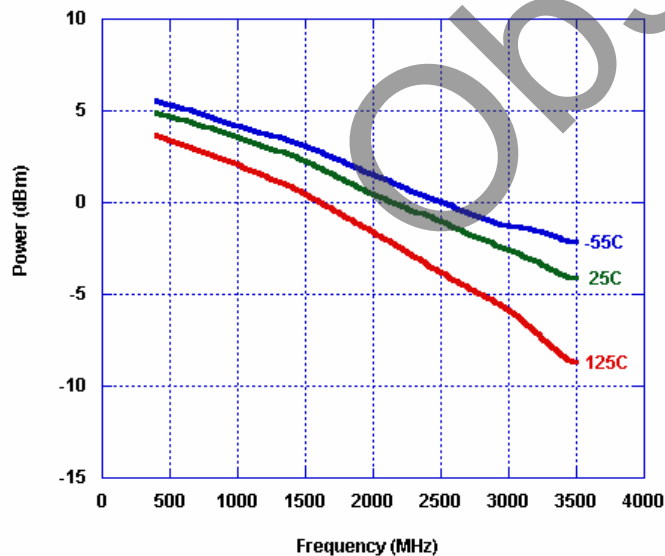


Figure 8. Output Power



Evaluation Kit

Evaluation Kit Operation

The MSOP Prescaler Evaluation Board was designed to help customers evaluate the *PE83501* Divide-by-2 Prescaler. On this board, the device input (pin 2) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. It is important to note that the value of this capacitance will impact the performance of the device. A value of 15 pF was found to be optimal for this board layout; other applications may require a different value.

The device output (pin 7) is connected to connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. Note that this capacitor must be chosen to have a low impedance at the desired output frequency of the device. The value of 47 pF was chosen to provide a wide operating range for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ϵ_r of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide.

J2 provides DC power to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device VDD pin (1). Two decoupling capacitors (10 pF, 1000 pF) are included on this trace.

It is the responsibility of the customer to determine proper supply decoupling for their design application.

The DEC pin (3) must be connected to a low impedance AC ground for proper device operation. On the board, two decoupling capacitors (C6 = 10 nF, C4 = 10 pF), located on the back of the board, perform this function.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 731-9400 and ask for applications support. You may also contact us by fax or e-mail:

Fax: (858) 731-9499

E-Mail: help@psemi.com

Figure 9. Evaluation Board Layouts

Peregrine Specification 101/0035

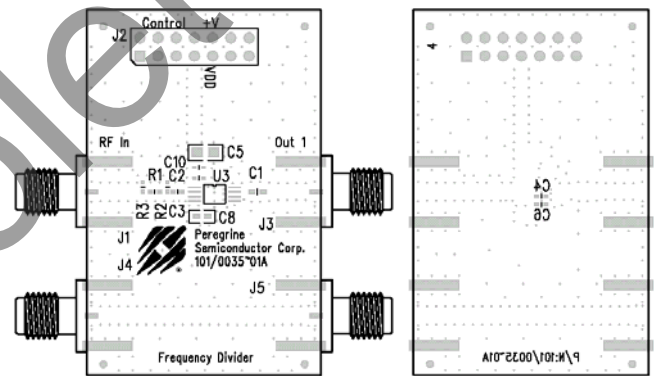


Figure 10. Evaluation Board Schematic

Peregrine Specification 102/0200

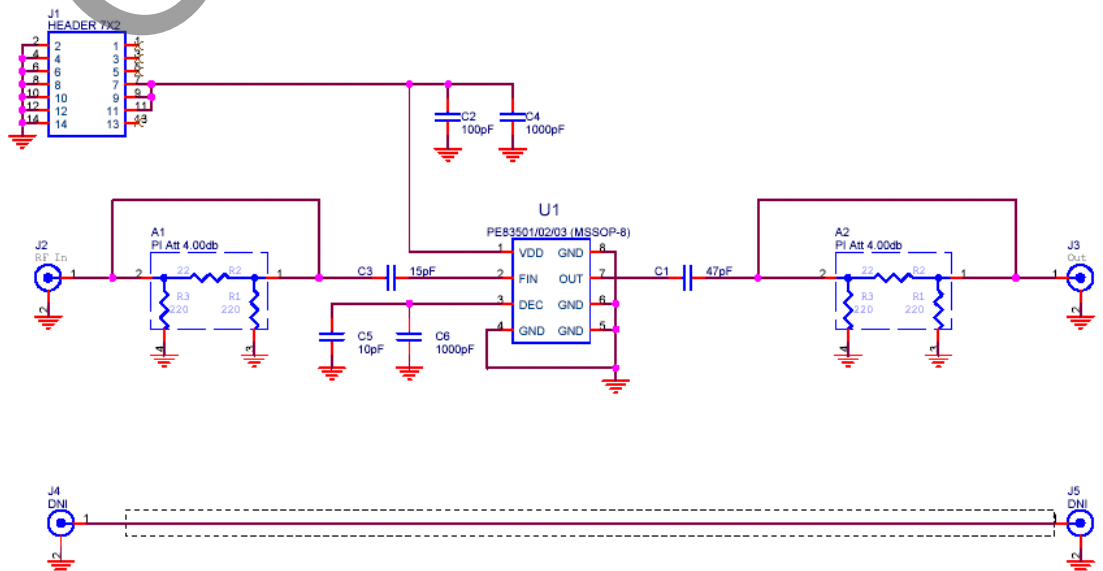


Figure 11. Package Drawing

8-lead MSOP

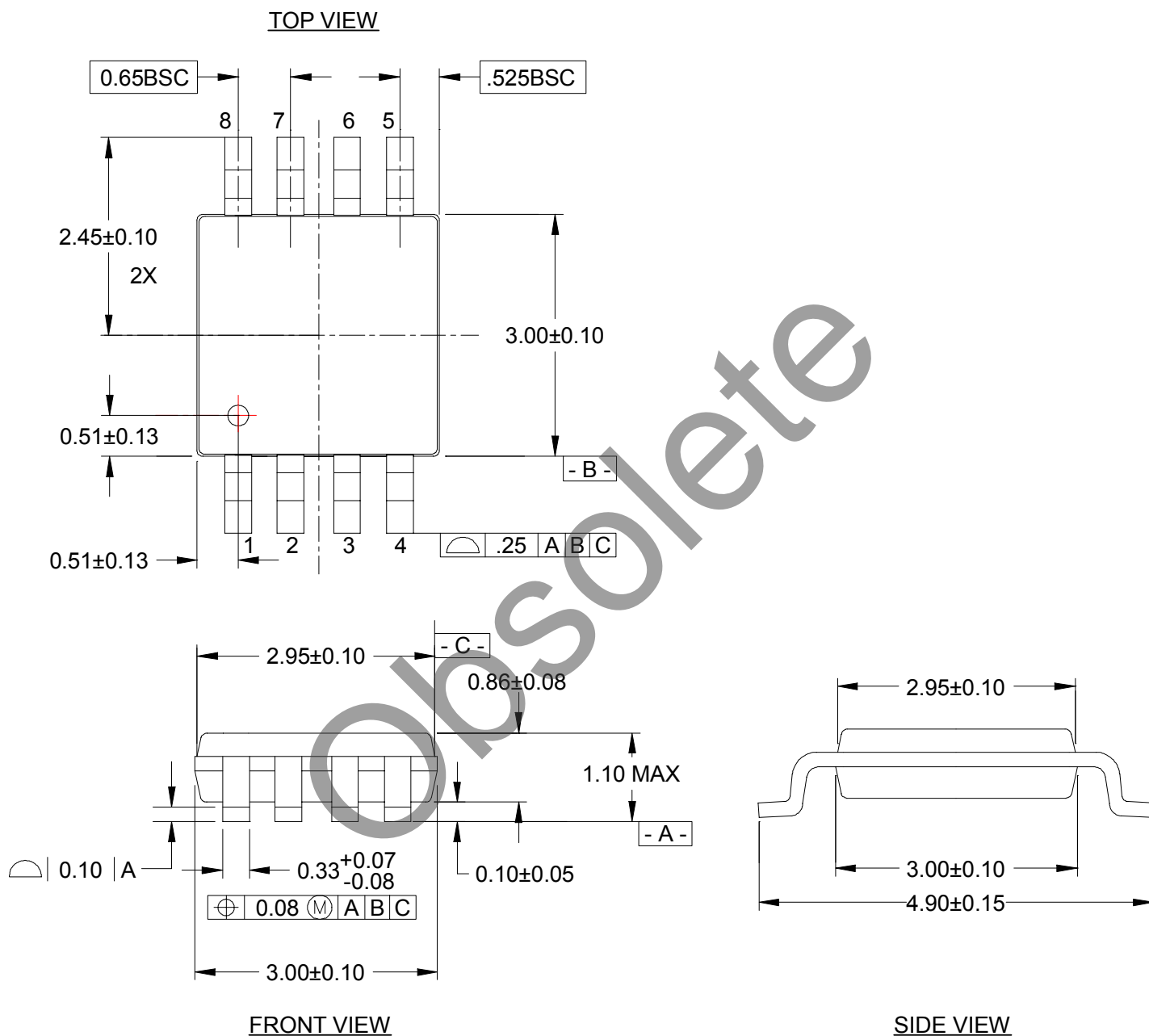
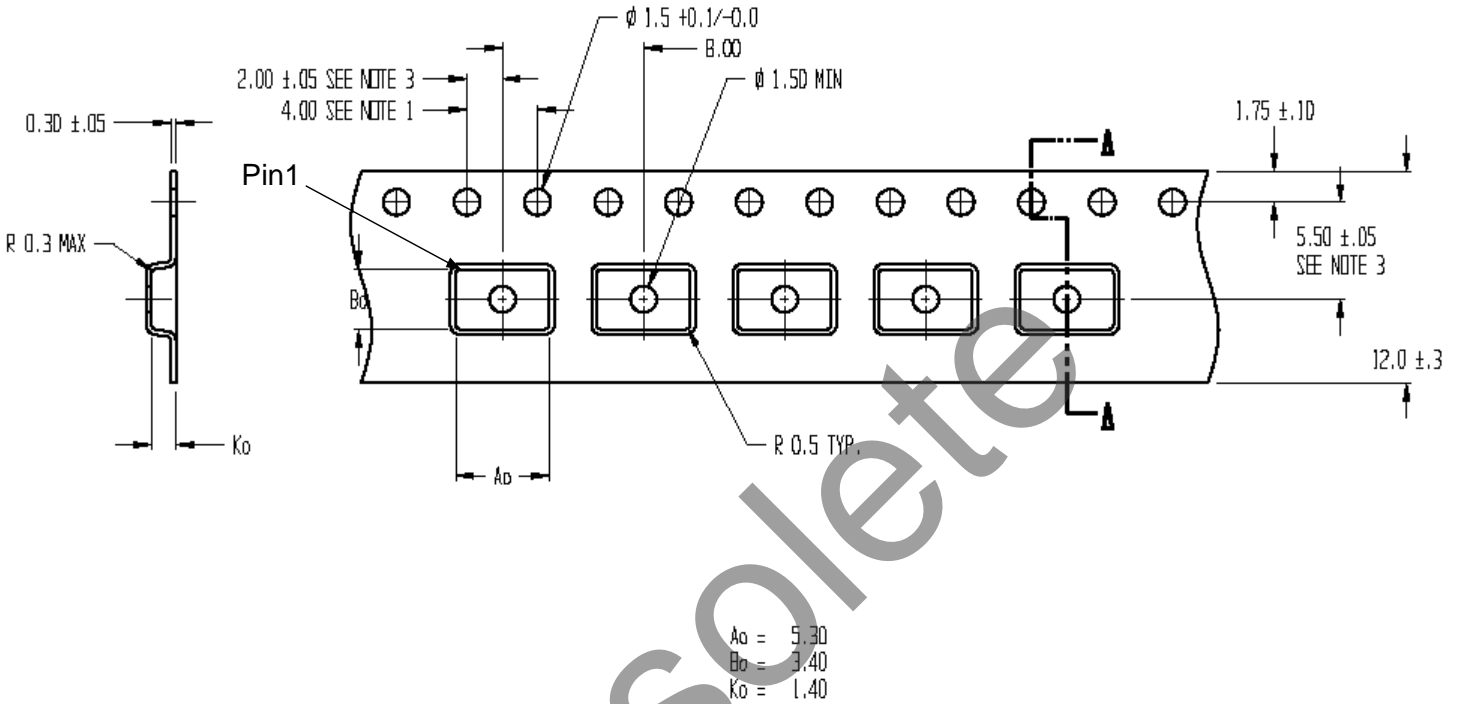


Figure 12. Tape and Reel Specifications

8-lead MSOP



NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
83501-11	PE83501	PE83501-08MSOP-100A	8-lead MSOP	50 pcs. / Tube
83501-12	PE83501	PE83501-08MSOP-2000C	8-lead MSOP	2000 pcs. / T&R
83501-00	PE83501-EK	PE83501-08MSOP-EK	Evaluation Board	1 / Box

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