Product Specification

PE83503

3.5 GHz Low Power UltraCMOS™ Divide-by-8 Prescaler
Military Operating Temperature Range

Product Description

The PE83503 is a high-performance monolithic UltraCMOS™ prescaler with a fixed divide ratio of 8. Its operating frequency range is 1.5 GHz to 3.5 GHz. The PE83503 operates on a nominal 3 V supply and draws only 12 mA. It is packaged in a small 8-lead MSOP and is ideal for microwave PLL synthesis solutions.

The PE83503 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- High-frequency operation: 1.5 GHz to 3.5 GHz
- Fixed divide ratio of 8
- Low-power operation: 12 mA typical @ 3 V across frequency
- Small package: 8-lead MSOP
- Low Cost

Figure 1. Functional Schematic Diagram

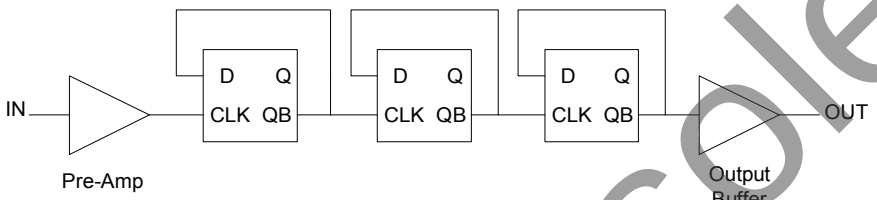


Figure 2. Package Type
8-lead MSOP

Table 1. Electrical Specifications ($Z_S = Z_L = 50\ \Omega$)

2.85 V ≤ V_{DD} ≤ 3.15 V; -55° C ≤ T_A ≤ 125° C, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			13	19	mA
Input Frequency (F_{IN})		1.5		3.5	GHz
Input Power (P_{IN})	1500 MHz ≤ F_{in} ≤ 2800 MHz	-5		+10	dBm
	2800 MHz < F_{in} ≤ 3500 MHz	0		+10	dBm
Output Power		0			dBm

Figure 3. Pin Configuration (Top View)

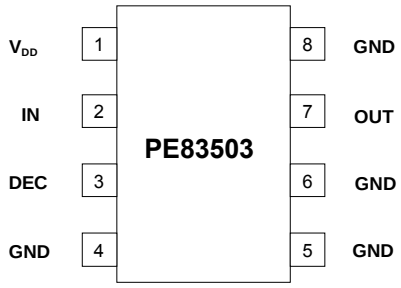


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Power supply pin. Bypassing is required.
2	IN	Input signal pin. Should be coupled with a capacitor (eg 15pF)
3	DEC	Power supply decoupling pin. Place a capacitor as close as possible and connect directly to the ground plane (eg 10 nF and 10 pF).
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	GND	Ground pin.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 100 pF).
8	GND	Ground pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		4.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-55	125	°C
V_{ESD}	ESD voltage (Human Body Model)		250	V
P_{INMAX}	Maximum input power		15	dBm

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The *PE83503* takes an input signal frequency from 1.5 GHz to 3.5 GHz and produces an output signal frequency one-eighth that of the supplied input. In order for the prescaler to work properly, several conditions need to be adhered to. It is crucial that pin 3 be supplied with a bypass capacitor to ground. In addition, the input and output signals (pins 2 & 7, respectively) need to be AC coupled via an external capacitor as shown in the test circuit in Figure 7.

The ground pattern on the board should be made as wide as possible to minimize ground impedance.

Figure 4. Test Circuit Block Diagram

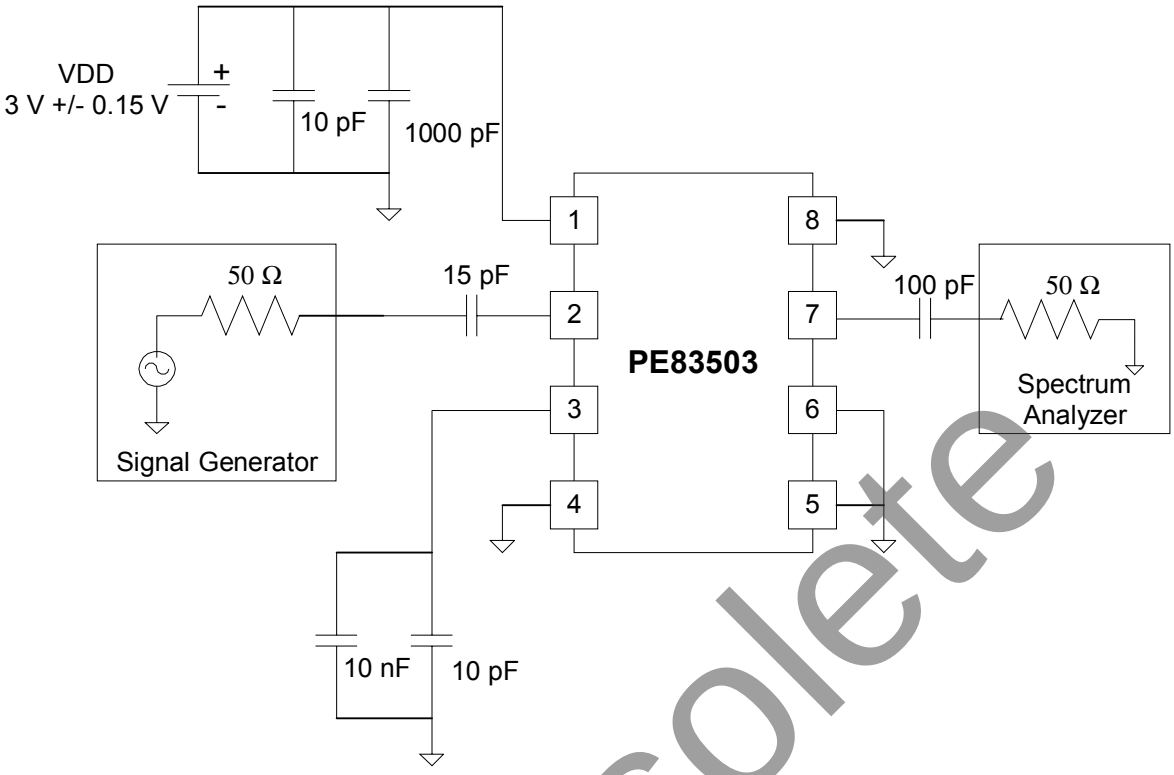
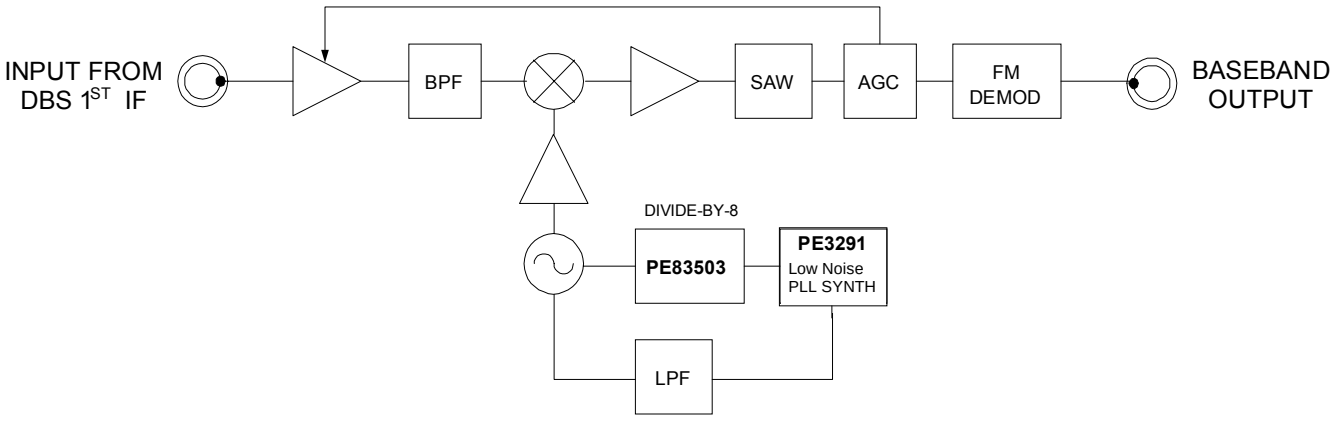


Figure 5. High Frequency System Application

The wideband frequency of operation of the *PE83503* makes it an ideal part for use in a DBS downconverter system.



Typical Performance Data: V_{DD} = 3.0 V

Figure 6. Input Sensitivity

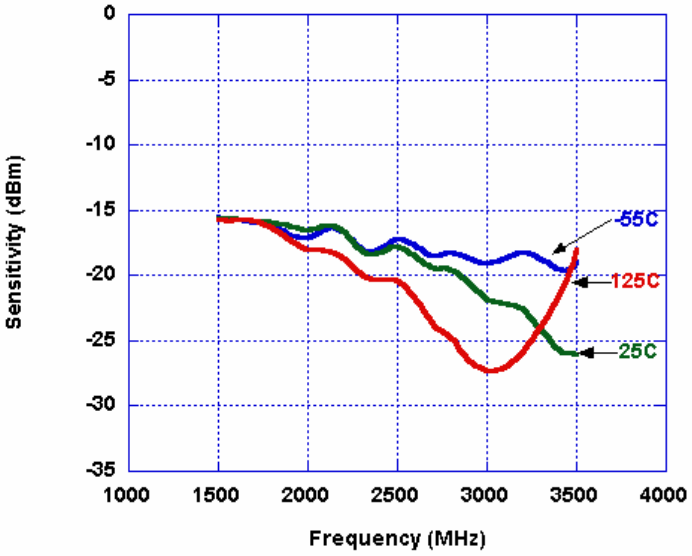


Figure 7. Device Current

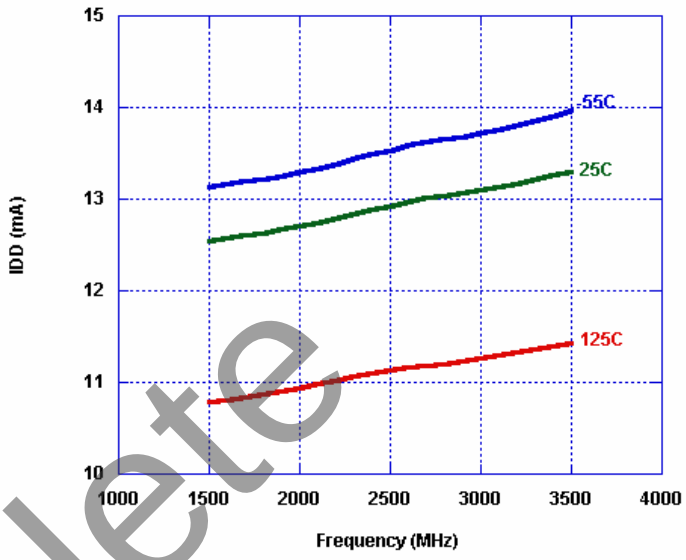
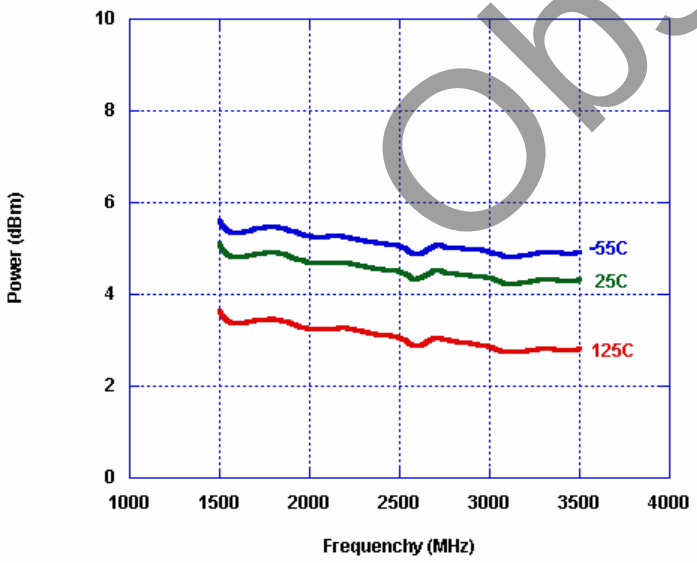


Figure 8. Output Power



Evaluation Kit

Evaluation Kit Operation

The MSOP Prescaler Evaluation Board was designed to help customers evaluate the *PE83503* Divide-by-8 Prescaler. On this board, the device input (pin 2) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. It is important to note that the value of this capacitance will impact the performance of the device. A value of 15pF was found to be optimal for this board layout; other applications may require a different value.

The device output (pin 7) is connected to connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. Note that this capacitor must be chosen to have a low impedance at the desired output frequency the device. The value of 100pF was chosen to provide a wide operating range for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ε_r of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide.

J2 provides DC power to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device VDD pin (1). Two decoupling capacitors (10 pF, 1000 pF) are included on this trace.

It is the responsibility of the customer to determine proper supply decoupling for their design application.

The DEC pin (3) must be connected to a low impedance AC ground for proper device operation. On the board, two decoupling capacitors (C6 = 10 nF, C4 = 10 pF), located on the back of the board, perform this function.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 731-9400 and ask for applications support. You may also contact us by fax or e-mail:
Fax: (858) 731-9499
E-Mail: help@psemi.com

Figure 9. Evaluation Board Layouts
Peregrine Specification 101/0035

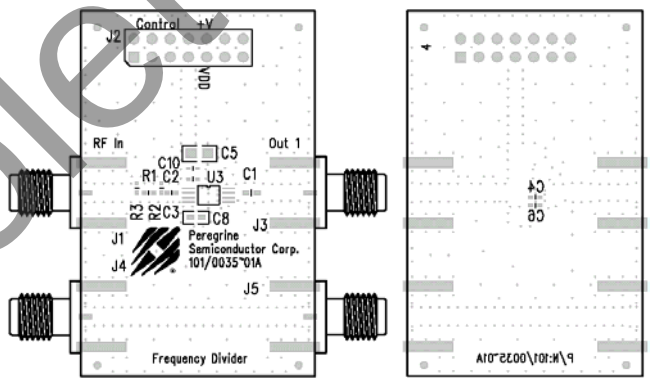


Figure 10. Evaluation Board Schematic
Peregrine Specification 102/0200

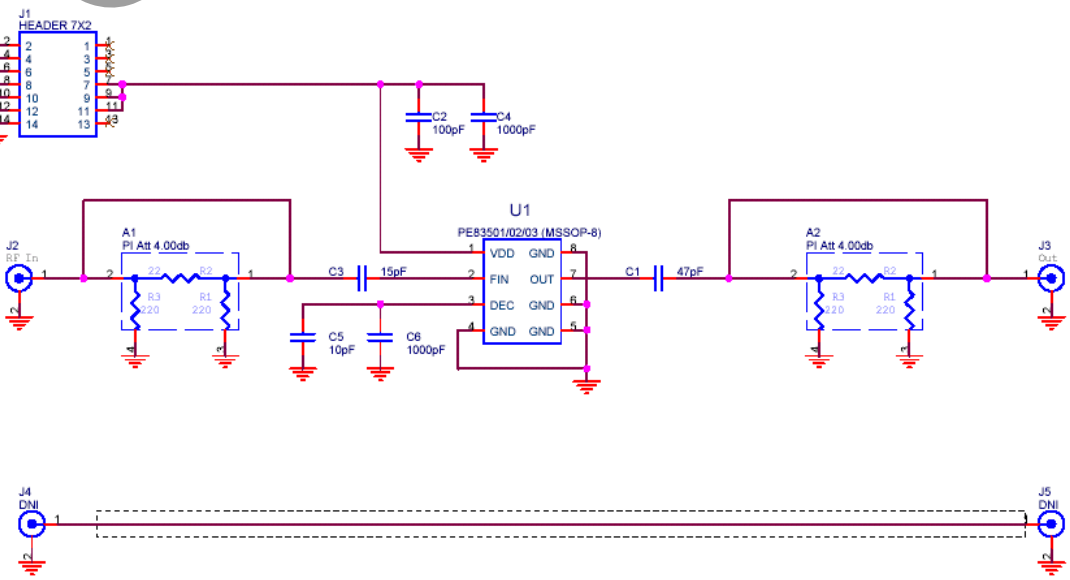


Figure 11. Package Drawing

8-lead MSOP

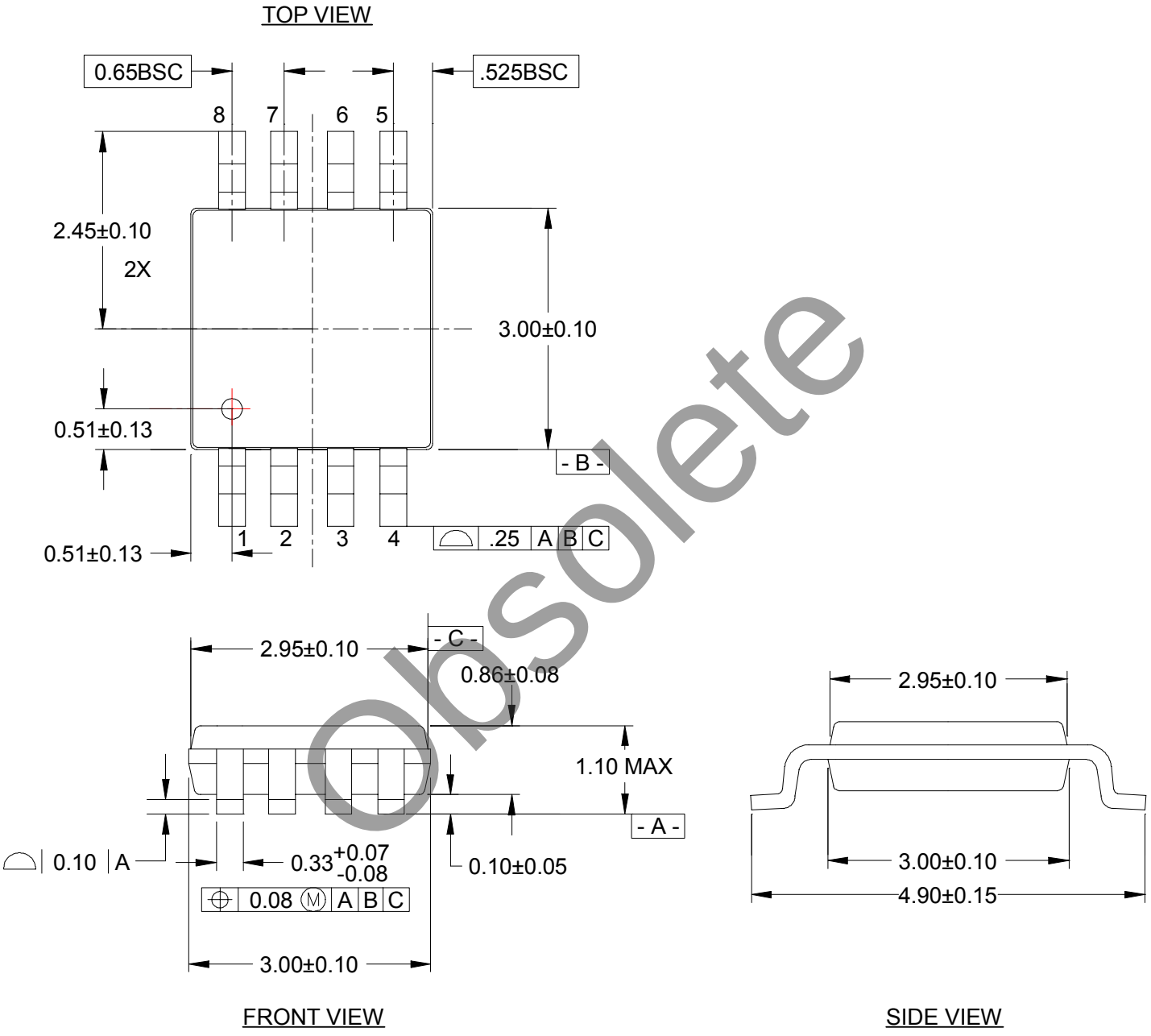
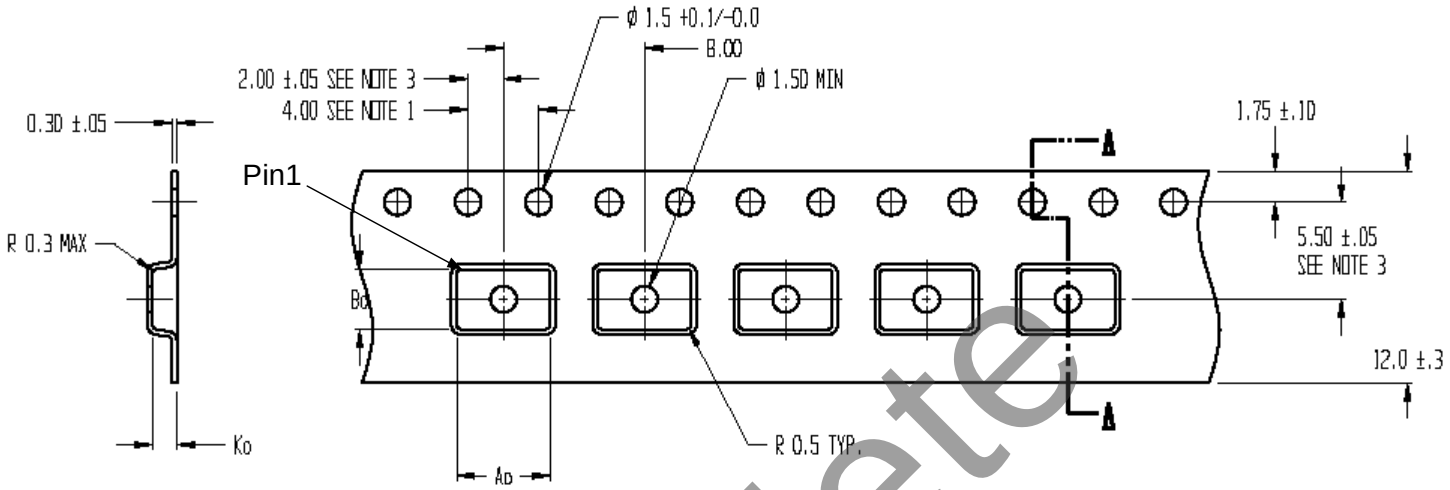


Figure 12. Tape and Reel Specifications

8-lead MSOP



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
83503-21	83503	PE83503-08MSOP-100A	8-lead MSOP	50 pcs. / Tube
83503-22	83503	PE83503-08MSOP-2000C	8-lead MSOP	2000 pcs. / T&R
83503-00	PE83503-EK	PE83503-08MSOP-EK	Evaluation Board	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation
9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

North Asia Pacific

Peregrine Semiconductor K.K.
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

Peregrine Semiconductor, Korea
#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

South Asia Pacific

Peregrine Semiconductor, China
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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